

Service Manual

DVCPRO

DVCPRO Studio VTR

AJ-D750_{E/EN}

COMPONENT SERIAL I/F BOARD

AJ-YA750_P

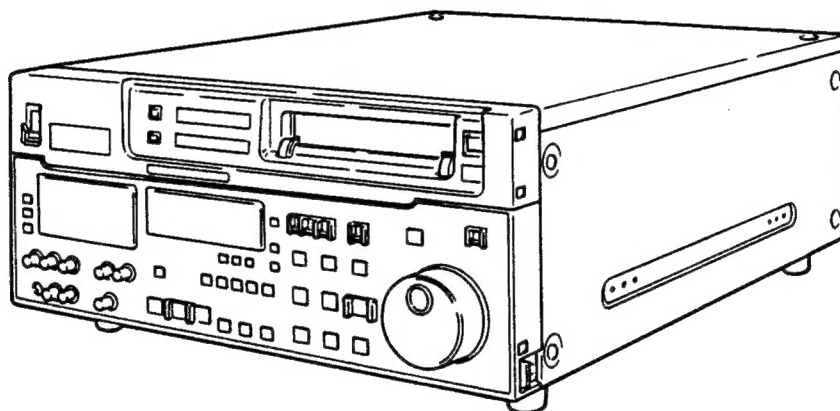
Vol. 2

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Panasonic

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INTRODUCTION

This service manual contains technical information which allow service personnel to understand and service the DVCPRÖ Studio VTR AJ-D750E/EN

Specifications

GENERAL

Power supply:	AC 220 – 240 V±10%, 50 – 60 Hz
Power consumption:	165 W

Operating ambient temperature:	5°C to 40°C (41°F to 104°F)
Operating ambient humidity:	10% to 90% (no condensation)
Weight:	18 kg
Dimensions (W×H×D):	424×175×415 mm
Recording format:	DVCPRÖ format
Recording tracks:	Digital video Time code Recorded in sub-code area Digital audio 2channels Cue Track 1 track Control (CTL) 1 track
Tape speed:	33.854 mm/sec
Recording time:	General purpose cassette; Max. 123 minutes News-gathering cassette; Max. 63 minutes
Tape:	1/4-inch thin magnetic layer metal tape
FF/REW time:	Less than 3 min (with general purpose cassette) Less than 2 min (with news-gathering cassette)
Editing accuracy:	±0 frame (using time code)
Tape timer accuracy:	±1 frame (using continuous CTL signal)
Servo lock time:	Less than 0.5 sec. (colour framing/standby ON)

VIDEO

(Digital video)

Sampling frequencies:	Y: 13.5 MHz/Pb, Pr: 3.375 MHz
Quantizing:	8 bits
Error correction:	Reed-Solomon product code

(Digital IN/analogue component OUT)

Video bandwidth:	Y: 25 Hz to 5.5 MHz (±0.5 dB) 5.75 MHz (–2 dB) Pb, Pr: 25 Hz to 1.3 MHz (±0.5 dB) 1.5 MHz (–5 dB) typ.
S/N ratio:	Better than 60 dB
K factor:	Less than 1%

(Analogue component IN/component OUT)

Video bandwidth:	Y: 25 Hz to 5.5 MHz (±1 dB) 5.75 MHz (–3 dB) Pb, Pr: 25 Hz to 1.3 MHz (±1 dB) 1.5 MHz (–6 dB) typ.
S/N ratio:	Better than 55 dB
K factor:	Less than 1%

(Analogue composite IN/composite OUT)

Video bandwidth:	Y: 25 to 5.5 MHz (±1 dB)
S/N ratio:	Better than 20 ns
K factor:	Less than 2%

(Video input connector)

Analogue component input:	BNC×3 (Y, Pb, Pr) Y: 1.0 Vp-p, 75Ω Pb, Pr: 0.7 Vp-p, 75Ω (100% colour bar, 0% setup)
Analogue composite input:	BNC×2, loop-through, 75Ω on/off
Reference input:	Analogue composite
Serial digital component input (option):	BNC×2, loop-through, 75Ω on/off Complies with EBU Tech. 3267-E standard, BNC×2, active through

(Video output connector)

Analogue component output:	BNC×3 (Y, Pb, Pr) Y: 1.0 Vp-p, 75Ω Pb, Pr: 0.7 Vp-p, 75Ω (100% colour bar, 0% setup)
Analogue composite output:	BNC×3 Video1/video2/video3 (superimpose on/off)
Serial digital component output (option):	Complies with EBU Tech. 3267-E standard, BNC×3

(Video signals adjustment)

Composite video input signal:	±3 dB
Video output gain:	±3 dB
Video output chroma gain:	±3 dB
Video output chroma phase:	±30°
Video output black level:	±100 mV
Video output sync phase:	±6 μs
Video output SC phase:	±180°
Video output Y/C delay:	±300 ns

AUDIO

(Digital audio)

Sampling frequencies:	48 kHz
Quantizing:	16 bits
Frequency response:	20 Hz to 20 kHz ±1 dB
Dynamic range:	Better than 90 dB (1 kHz, emphasis OFF, "A" weighted)
Distortion:	Less than 0.05% (1 kHz, emphasis OFF, standard level)
Crosstalk:	Less than –80 dB (1 kHz, between 2 channels)
Wow & flutter:	Below measurable limit
Headroom:	18 dB
Emphasis:	T1=50μs/T2=15μs (on/off selectable)

(Cue track)

Frequency response:	300 Hz to 6 kHz ±3 dB
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(Audio input connector)

Analogue input (CH1/CH2):	XLR×2, 600Ω/high impedance selectable, +4/0/–20 dBu
Digital input (CH1/CH2):	XLR×1, AES/EBU format
Serial digital input (option):	Complies with EBU Tech. 3267-E standard (BNC)
Cue track input:	XLR×1, 600Ω/high impedance selectable, +4/0/–20/–60 dBu

(Audio output connector)

Analogue output (CH1/CH2):	XLR×2, low impedance, +4/0/–20 dBu
Digital output (CH1/CH2):	XLR×1, AES/EBU format
Serial digital output (option):	Complies with EBU Tech. 3267-E standard (BNC)
Cue track output:	XLR×1, low impedance, +4/0/–20 dBu
Monitor output:	XLR×2, low impedance, +4/0/–20 dBu
Headphones:	Variable level, mini-jack, 8Ω

Other input/output connector

Time code input:	XLR×1, 0.5 to 8 Vp-p
Time code output:	XLR×1, 2.0 Vp-p
RS-422A input/output:	D-sub 9-pin, RS-422A interface
RS-422A output:	D-sub 9-pin, RS-422A interface
RS-232C:	D-sub 25-pin, RS-232C interface
Parallel input/output:	D-sub 25-pin
Encoder remote:	D-sub 15-pin

Weight and dimensions when shown are approximately. Specifications are subject to change without notice.

SAFETY PRECAUTIONS

GENERAL GUIDELINES

1. When servicing, observe the original lead dress. If a short circuit is found, replace all parts which have been overheated or damaged by the short circuit.
2. After servicing, see to it that all the protective devices such as insulation barriers, insulation papers shields are properly installed.
3. After servicing make the following leakage current checks to prevent the customer from being exposed to shock hazards.

LEAKAGE CURRENT COLD CHECK

1. Unplug the AC cord and connect a jumper between the two prongs on the plug.
2. Measure the resistance value, with an ohm meter, between the jumpered AC plug and each exposed metallic cabinet part on the equipment such as screwheads, connectors, control shafts, etc. When the exposed metallic part has a return path to the chassis, the reading should be between $1\text{ M}\Omega$ and $5.2\text{ M}\Omega$. When the exposed metal does not have a return path to the chassis, the reading must be ∞ .

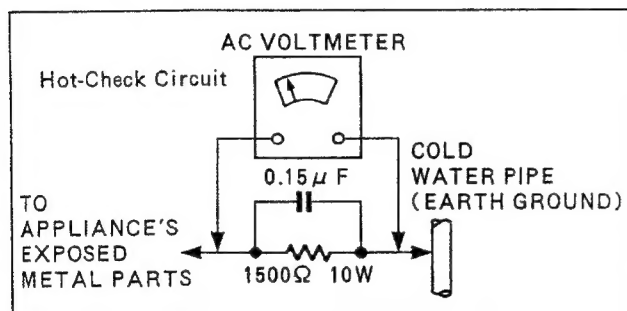


Figure 1

LEAKAGE CURRENT HOT CHECK (See Figure 1)

1. Plug the AC cord directly into the AC outlet. Do not use an isolation transformer for this check.
2. Connect a $1.5\text{ K}\Omega$, 10W resistor, in parallel with $0.15\mu\text{F}$ capacitor, between each exposed metallic part on the set and a good earth ground such as a water pipe, as shown in Figure 1.
3. Use an AC voltmeter, with 1000 ohms/volt or more sensitivity, to measure the potential across the resistor.
4. Check each exposed metallic part, and measure the voltage at each point.
5. Reverse the AC plug in the AC outlet repeat each of the above measurements.
6. The potential at any point should not exceed 0.75 volts RMS . A leakage current tester (Simpson Model 229 equivalent) may be used to make the hot checks, leakage current must not exceed $1\frac{1}{2}$ milliamp. In case a measurement is outside of the limits specified, there is a possibility of a shock hazard, and the equipment should be repaired and rechecked before it is returned to the customer.

ELECTROSTATICALLY SENSITIVE (ES) DEVICES

Some semiconductor (solid state) devices can be damaged easily by static electricity. Such components commonly are called Electrostatically sensitive (ES) Devices. Examples of typical ES devices are integrated circuits and some field-effect transistors and semiconductor "chip" components. The following techniques should be used to help reduce the incidence of component damage caused by static electricity.

1. Immediately before handling any semiconductor component or semiconductor-equipped assembly, drain off any electrostatic charge on your body by touching a known earth ground. Alternatively, obtain and wear a commercially available discharging wrist strap device, which should be removed for potential shock reasons prior to applying power to the unit under test.
2. After removing an electrical assembly equipped with ES devices, place the assembly on a conductive surface such as aluminum foil, to prevent electrostatic charge buildup or exposure of the assembly.
3. Use only a grounded tip soldering iron to solder or unsolder ES devices.
4. Use only an anti-static solder removal device classified as "anti-static" can generate electrical charges sufficient to damage ES devices.
5. Do not use freon-propelled chemicals. These can generate electrical charges sufficient to damage ES devices.
6. Do not remove a replacement ES device from its protective package until immediately before you are ready to install it. (most replacement ES devices are packaged with leads electrically shorted together by conductive foam, aluminum foil or comparable conductive material).
7. Immediately before removing the protective material from the leads of replacement ES device, touch the protective material to the chassis or circuit assembly into which the device will be installed.
CAUTION: Be sure no power is applied to the chassis or circuit, and observe all other safety precautions.
8. Minimize bodily motions when handling unpackaged replacement ES devices. (Otherwise harmless motion such as the brushing together of your clothes fabric or the lifting of your foot from a carpeted floor can generate static electricity sufficient to damage an ES device).

X-RADIATION

WARNING

1. The potential source of X-Radiation in EVF sets is the High Voltage section and the picture tube.
2. When using a picture tube test jig for service, ensure that jig is capable of handling 10 kV without causing X-Radiation.
NOTE: It is important to use an accurate periodically calibrated high voltage meter.
3. Measure the High Voltage. The meter (electric type) reading should indicate 2.5 kV , $\pm 0.15\text{ kV}$. If the meter indication is out of tolerance, immediate service and correction is required to prevent the possibility of premature component failure. To prevent an X-Radiation possibility, it is essential to use the specified picture tube.

IMPORTANT

"Unauthorized recording of copyrighted television programs, video tapes and other materials may infringe the right of copyright owners and be contrary to copyright laws."

■ THIS APPARATUS MUST BE EARTHED

To ensure safe operation the three-pin plug must be inserted only into a standard three-pin power point which is effectively earthed through the normal house-hold wiring.

Extension cords used with the equipment must be three-core and be correctly wired to provide connection to earth. Wrongly wired extension cords are a major cause of fatalities.

The fact that the equipment operates satisfactorily does not imply that the power point is earthed and that the installation is completely safe. For your safety, if in any doubt about the effective earthing of the power point, consult a qualified electrician.

■ DO NOT REMOVE PANEL COVER BY UN-SCREWING

To reduce the risk of electric shock, do not remove cover. No user serviceable parts inside. And do not insert fingers or any other objects into the video cassette holder.

WARNING:

TO REDUCE THE RISK OF FIRE OR SHOCK HAZARD, DO NOT EXPOSE THIS EQUIPMENT TO RAIN OR MOISTURE.

CAUTION:

TO REDUCE THE RISK OF FIRE OR SHOCK HAZARD, AND ANNOYING INTERFERENCE, USE THE RECOMMENDED ACCESSOIRES ONLY.

CAUTION:

To reduce the risk of fire or shock hazard, refer change of switch setting inside the unit to qualified service personnel.

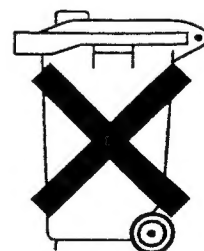
Operating precaution

Operation near any appliance which generates strong magnetic fields may give rise to noise in the video and audio signals. If this should be the case, deal with the situation by, for instance, moving the source of the magnetic fields away from the unit before operation.

☐ is the safety information.

Attention/Attentie

- This apparatus contains a lithium battery for memory back-up.
- For the removal of the battery at the moment of the disposal at the end of the service life please consult your dealer.
- Do not throw away the battery. Instead, hand it in as hazardous waste.
- Dit apparaat bevat een lithiumbatterij voor memory back-up.
- Raadpleeg uw leverancier over de verwijdering van de batterij op het moment dat u het apparaat bij einde levensduur afdankt.
- Gooi de batterij niet weg, maar lever hem in als KCA.



SECTION 1

BLOCK DIAGRAMS

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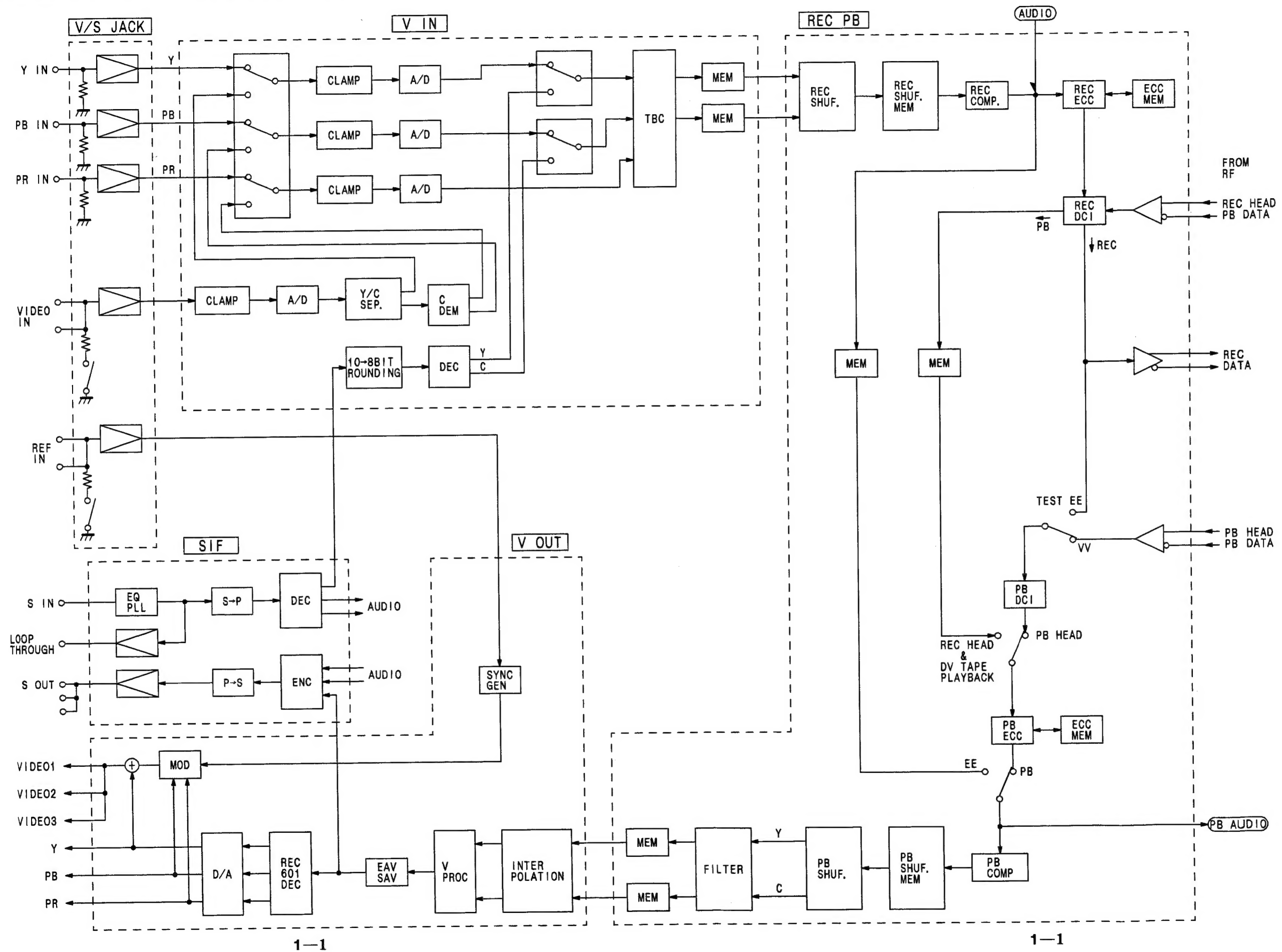
Section 2. Schematic Diagrams

Section 3. Circuit Board Diagrams

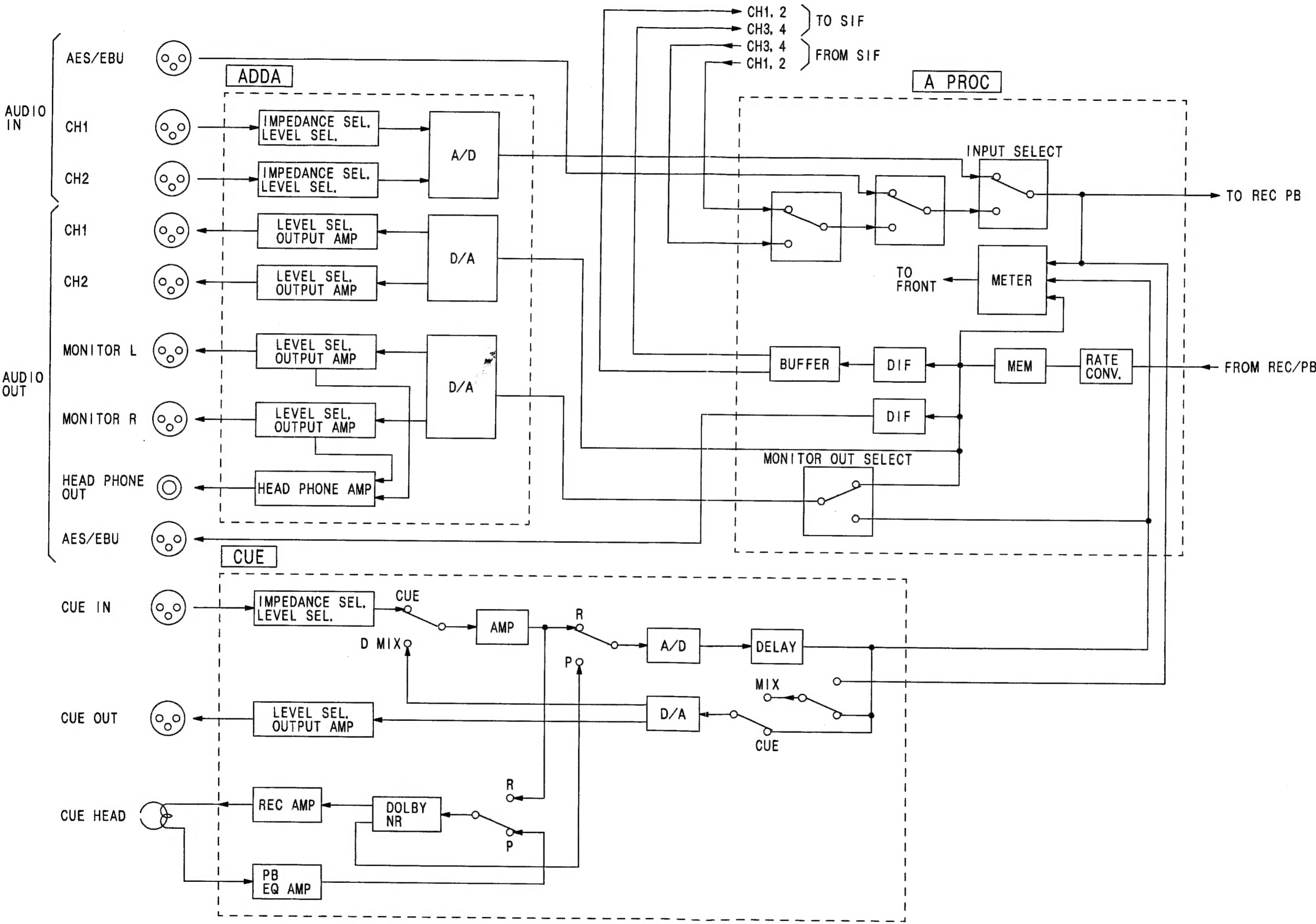
This section includes TP & VR location.

Section 4. IC Information

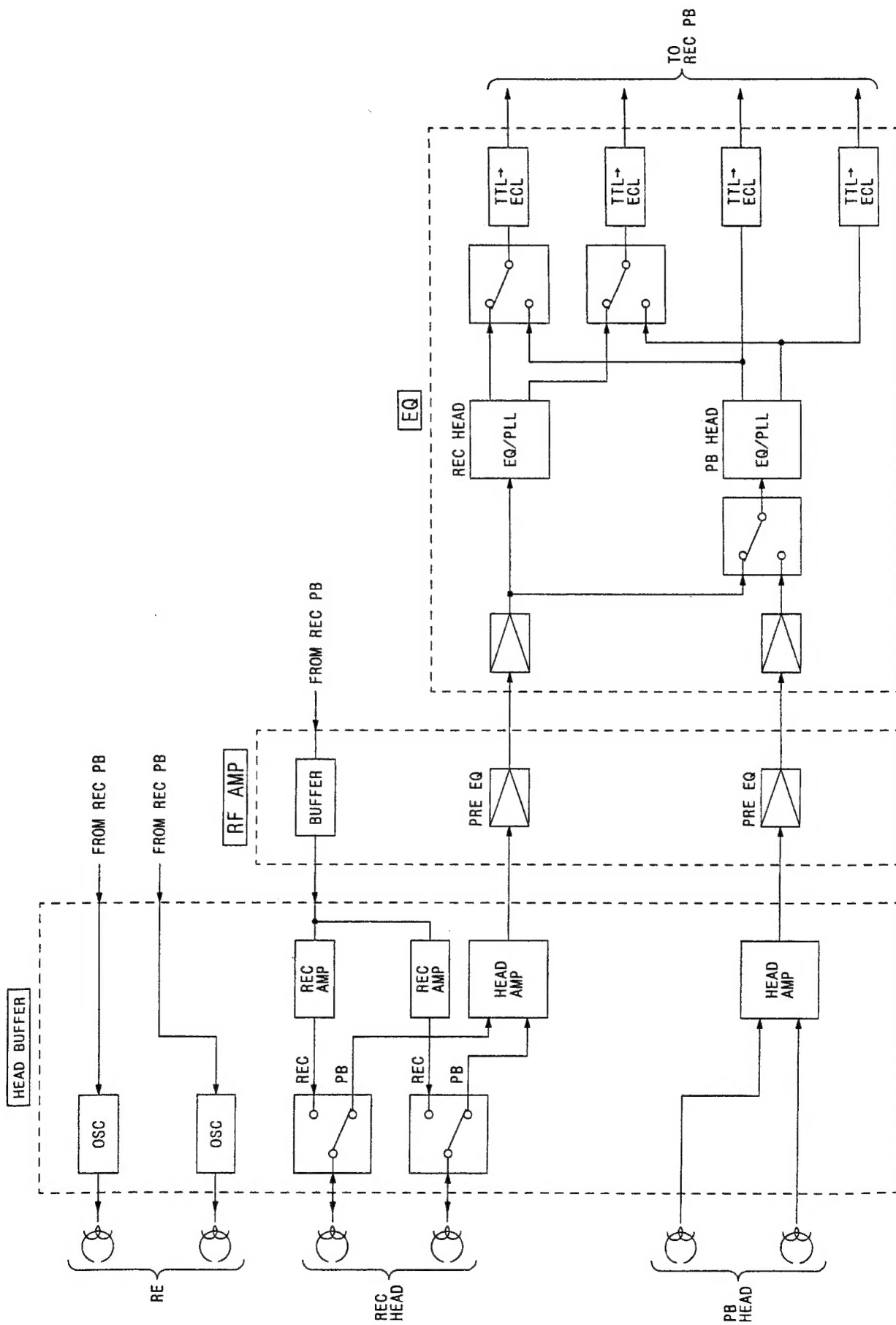
VIDEO OVERALL BLOCK DIAGRAM



AUDIO OVERALL BLOCK DIAGRAM



RF OVERALL BLOCK DIAGRAM



■ SERVO

[Outline, the characteristic]

- The motor drive circuit of the T reel, the S reel, the cylinder, the capstan
- The ATF servo
- 32 bits of one it controls all of the servos in CPU.

[Way of controlling]

- About the capstan mode and the reel mode of the reel control
The capstan mode is from stop to ± 10 times speed in shuttle.
The capstan mode is while the pinch roller is touch a capstan.
The reel mode is twice of speed from the \pm high speed.

- The T reel control

In the capstan mode, it is doing the control to turn at the torque which was fitted to the volume diameter using the volume diameter data (calculating by the T FG signal of 2 aspects and the S FG signal of 2 aspects).
In the reel mode, it is the speed control and the feedforward control which used FG signal.

- The S reel control

It is controlling tension capstan mode reel mode together.

- The capstan control

In record, it does the speed control which used FG signal.

Also, it is hanging a phase control by 1583 Hz to have made with the clock signal (the signal which divided 41.85Mhz in 1/2) of servo CPU and the signal with the occurrence of 294 pulses by the capstan 1 turn.

In playback, it is doing the optimal tracking by the ATF servo as phase control and speed control which used FG signal.

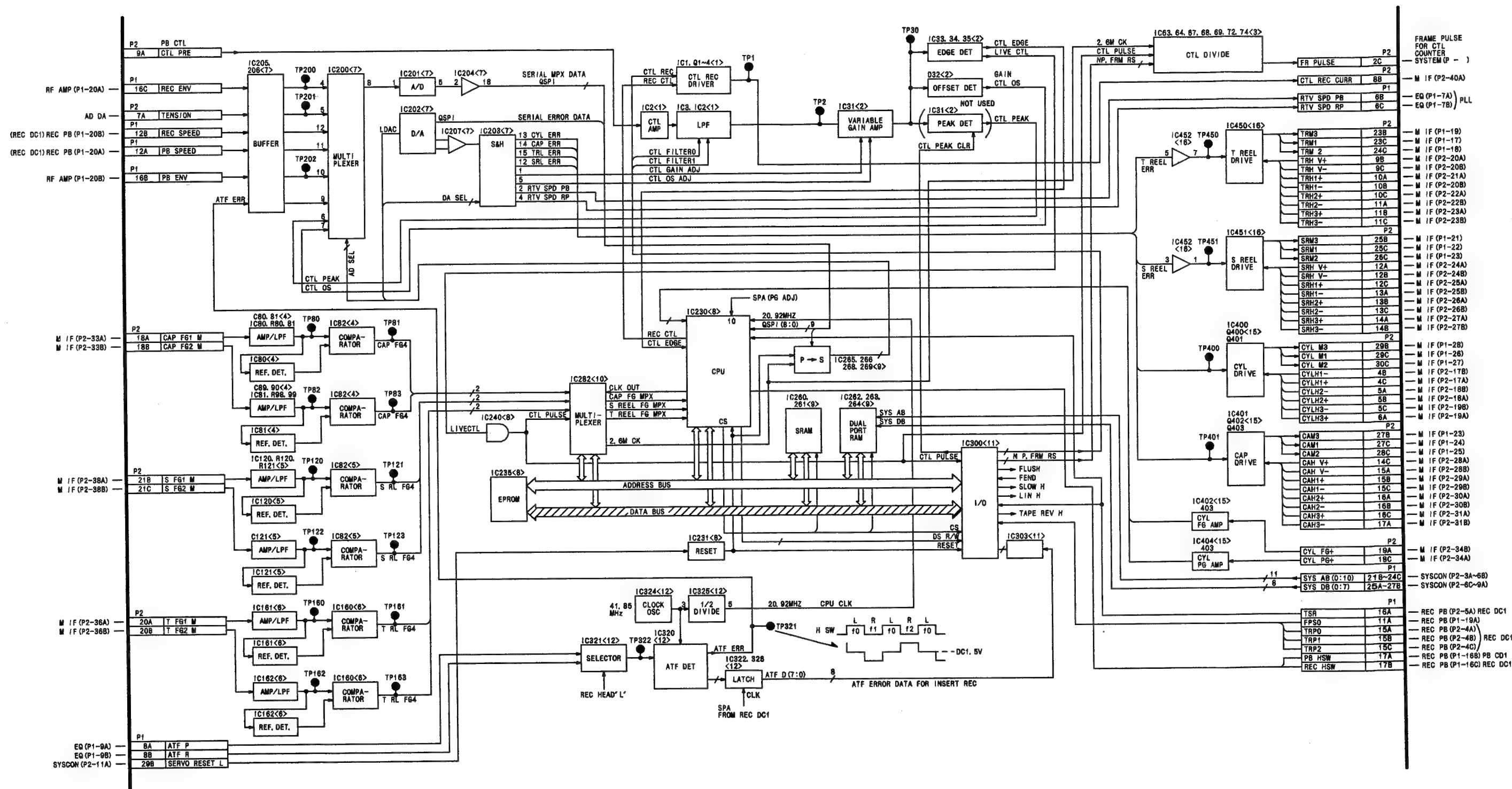
(It is doing the phase control of the capstan for ATF error voltage to be minimized).

- The cylinder control

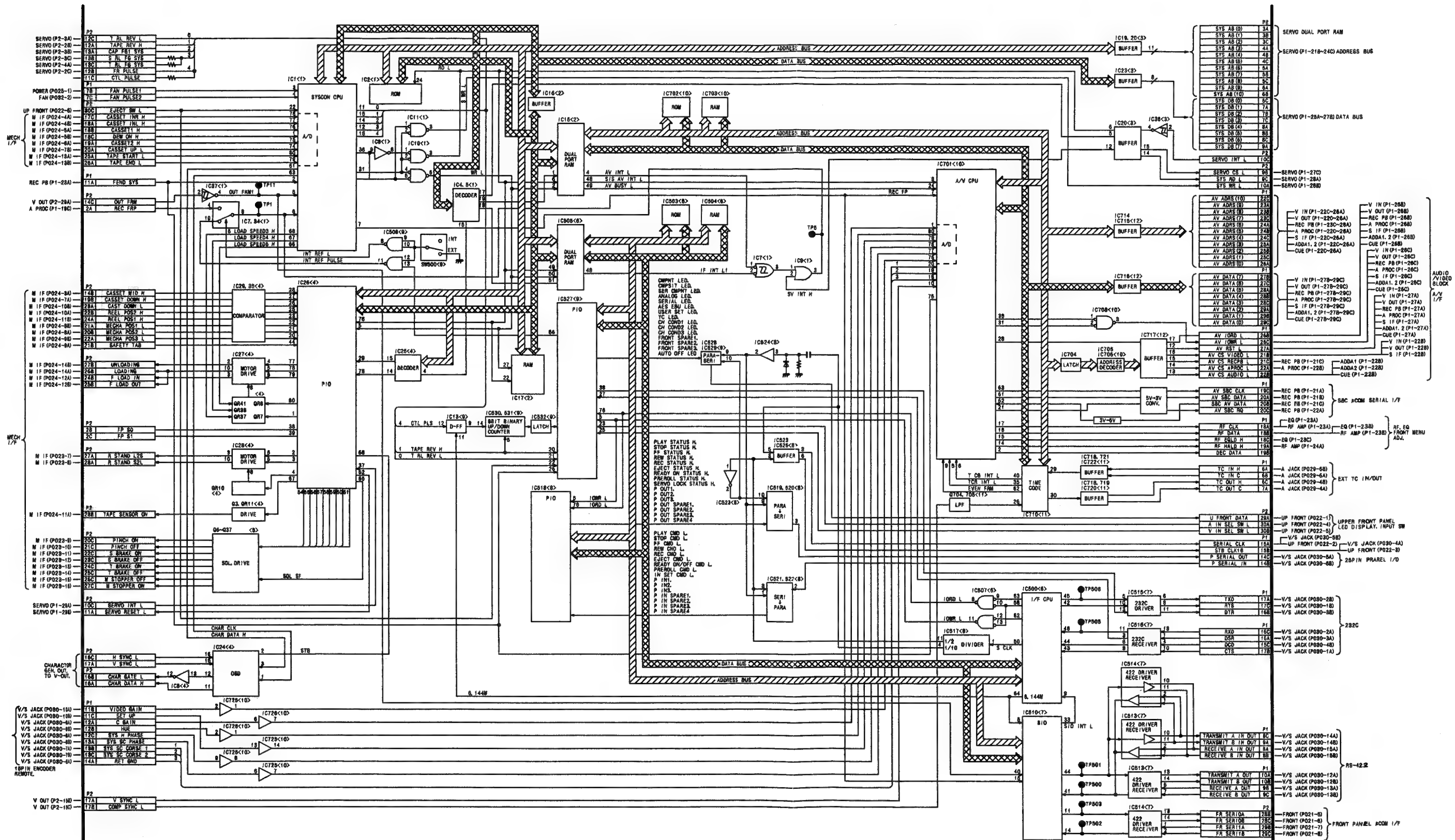
In record, in playback, together, it does a speed control using FG and the phase control goes in the TSR signal (from the REC PB board) and the head switching pulse.

When recording TSR signal, it is made from the input signal or the REF signal and in playback, it is made from the REF signal or the inner standard (INT SG).

F1 SERVO BLOCK DIAGRAM



F2 SYSCON BLOCK DIAGRAM



■ SYSCON

[Outline, the characteristic]

There are SERVO and FRONT in this board as three CPU(SYSCON, I/F, A/V) and CPU out of the board which has a mechanic interface, a remote interface and among CPU, they are linked with the dual port RAM.

[Composition]

•SYSCON-CPU	IC1
•SYSCON-ROM	IC2 (EEPROM)
•SYSCON-RAM	IC17
• The mechanism interface-PIO	IC26
•I/F-CPU	IC500
•I/F-ROM	IC503 (EEPROM)
•RS232C-DRIVER	IC515
•RS232C-RECEIVER	IC516
•RS422-DRIVER/RECEIVER	IC513, 514
•A/V-CPU	IC701
•A/V-ROM	IC702 (EEPROM)
•A/V-ROM	IC703
•TIMECODE	IC710

[Function]

The I/F part

The exchange of the signal with the upper front desk part

The exchange of the signal with FRONT CPU (It communicates with the serial).

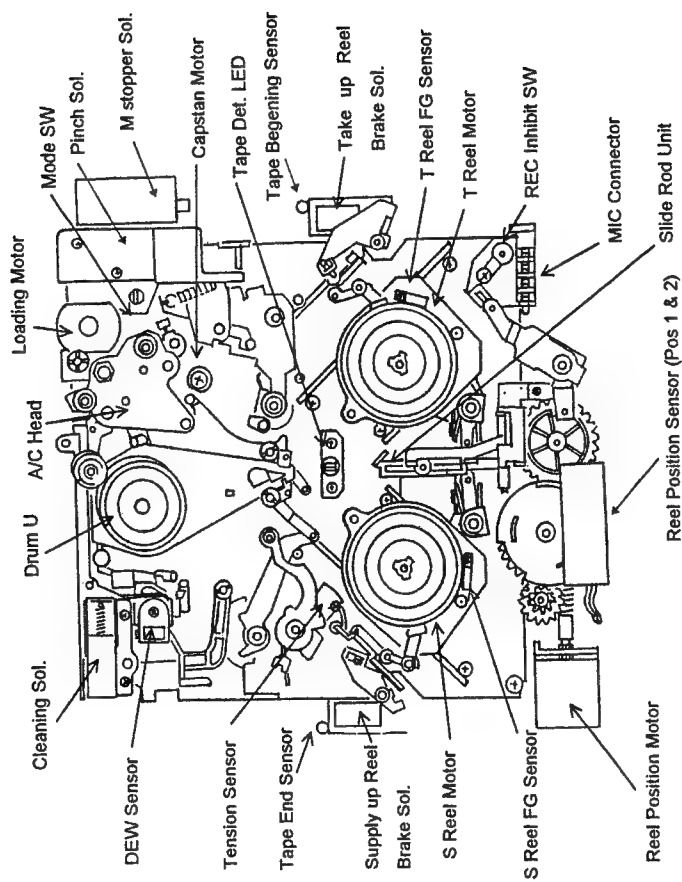
The exchange of the signal with the parallel port of 25 P

It converts from PIO(IC518) into the parallel signal with the jack board to the jack board through the connector P1 (15B from 14B) mother board through the serial OBU DO/parallel change IC(IC519, 520, 521, 522) through the bus.

The interface of RS-422A

The interface of RS-232C

Sensor Layout



■ SIF (This board is an option).

The input/output interface circuit of the component digital serial signal of 259M-C

- Input loop through
- Automatic Equalization
- No adjustment
- It is possible to 200 m transmit at the coaxial cable of 5C2V.
- 3 outputs
- The signal output is 75Ω $0.8V \pm 10\%$.

◆ The record system

A signal from the jack board is inputted to IC252 of the input equalizer and PLL with the coaxial cable. It compensates frequency characteristic here automatically and it extracts a input clock signal.

An input through signal is output to the jack board with the coaxial cable via driver circuit (IC255).

If the power supply of the VTR plugs, irrespective of the input choice, the through output always comes out.

The record signal from IC252 goes to serial to parallel conversion IC (IC254) and is changed into the 10 bits parallel signal.

After that, it separates an input audio signal at the SIF DECODER circuit.

A separated audio signal is output to 9 C, 10B of connector P2 through IC305.

The audio signal goes to the audio process board via the mother board.

The video signal goes from connector P1 (19B with 13 A) to the V_IN board via the mother board through TTL to ECL conversion IC (IC351,352,353) from buffer (IC304).

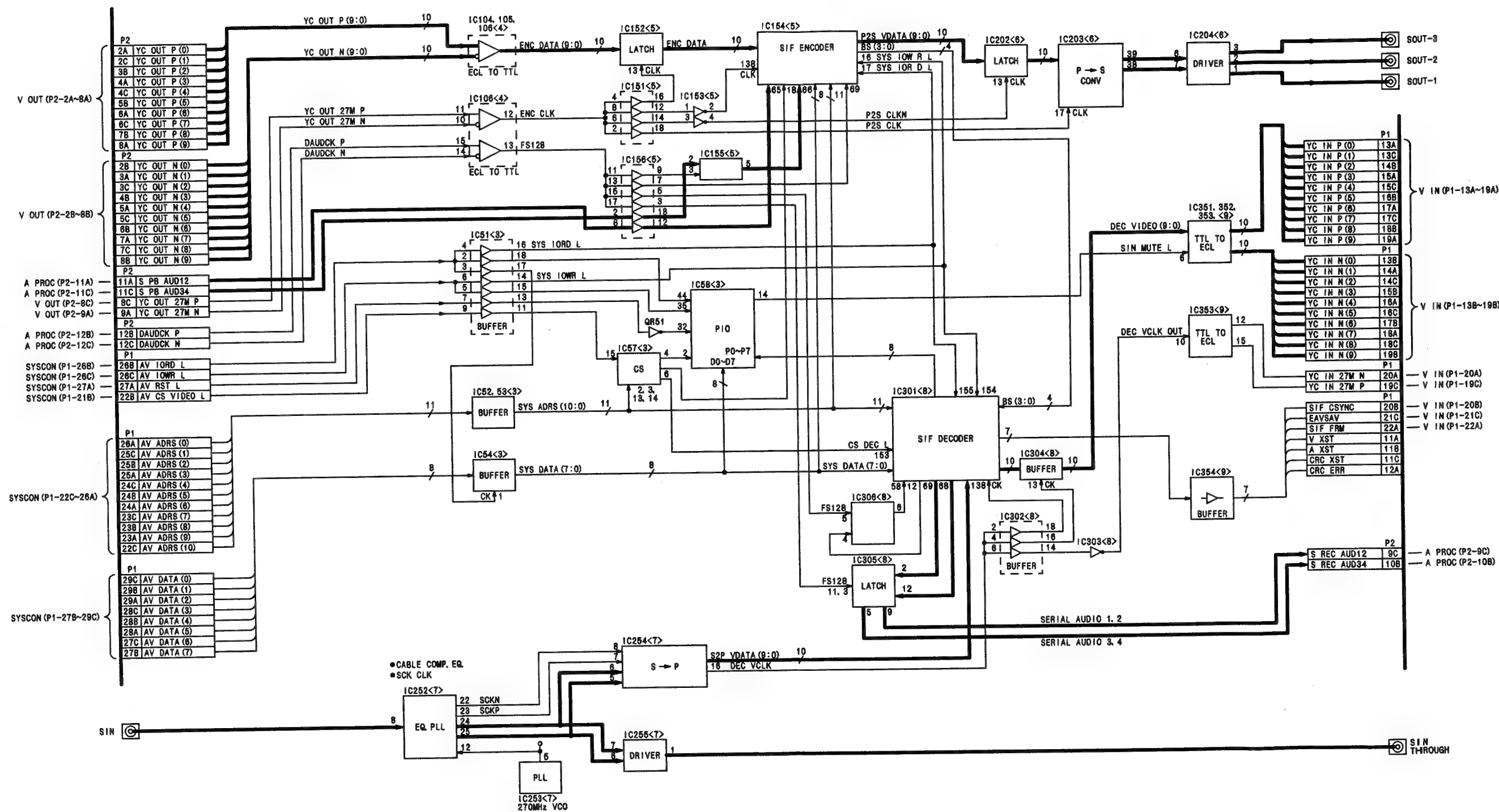
◆ The playback system

A signal from the V_OUT board is inputted from connector P2 (8B with 2 A) and is inputted to SIF ENCODER (IC154) via LATCH (IC152) after ECL to TTL conversion (IC104,105,106).

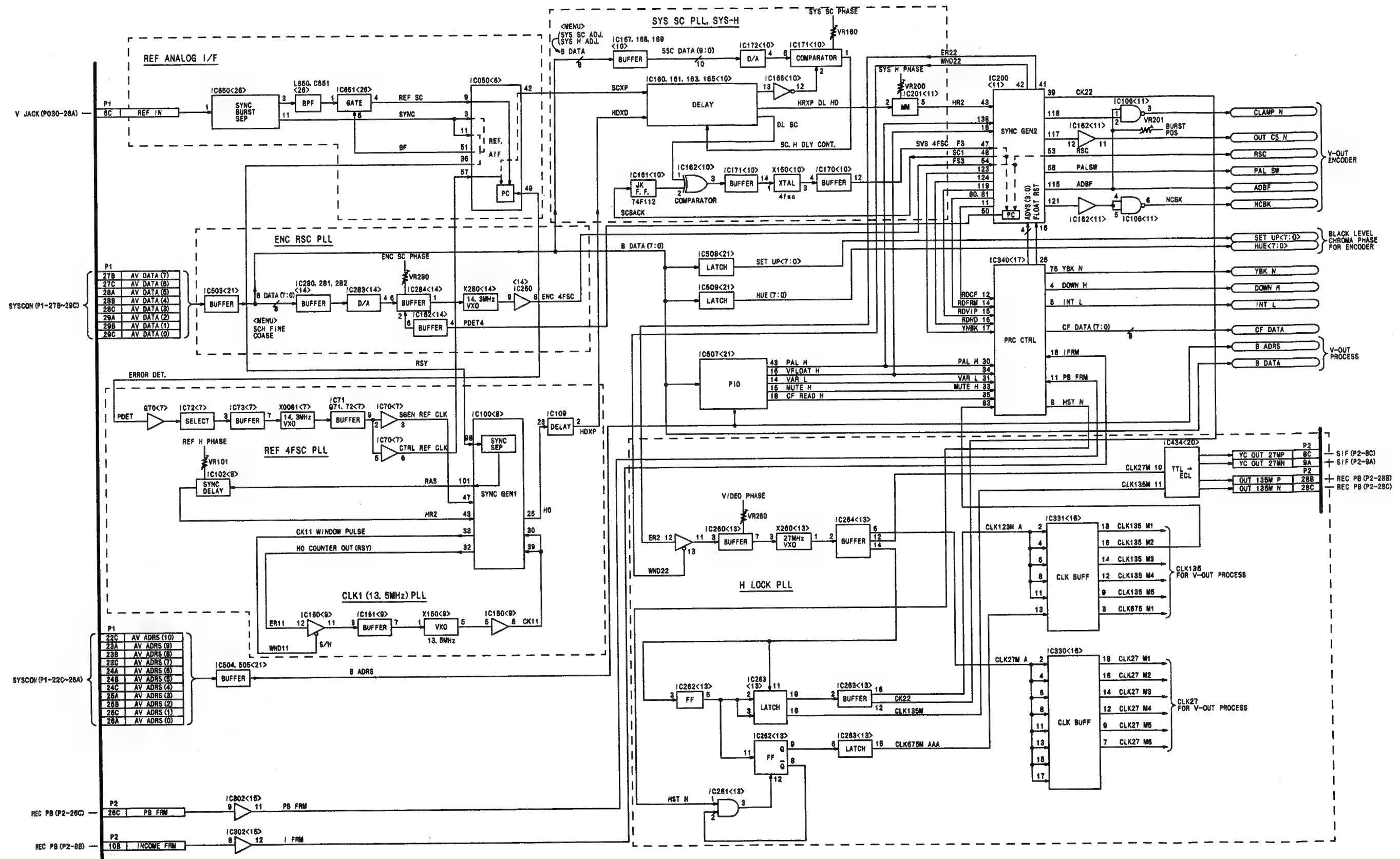
It adds an audio signal here.

This digital signal is changed into the serial signal with parallel to serial converter (IC203) via LATCH(IC202). It is output by the jack board via the 3 (SOUT-1,2,3) coaxial cable from DRIVER (IC204).

F3 SIF BLOCK DIAGRAM



F4 V-OUT BLOCK DIAGRAM (2/2)



■ V_OUT

This board processes a video signal after expansion from the REC PB board.

- The signal compensation in the slow playback mode
- External synchronization
- Video Process control
- The output of the digital signal to the SIF board
- The conversion to the analog signal (The analog component)
- The output of the analog component signal
- The change into the analog composite signal (Encoder)
- The output of the analog composite signal (3 signals)
- The VIDEO OUT3 has the superimpose.

A video signal after expansion from the REC PB board is inputted in connector P2 (from 21A to 26B).

Y signal is inputted in IC(IC362) of the interpolation through 1-H delay circuit (IC352) via LATCH(IC300).

A main signal is output via the MUX part and is input in VPROC-IC(IC370).

After that, a main signal is input in SAV EAV CODE ADD BLANKING MUTE(IC371) through variable delay (IC373,374).

In IC371, a main signal is mixed with the C signal.

C signal is input in IC(IC362) of the interpolation through 1-H delay circuit (IC358) via LATCH(IC301).

A main signal is input in VPROC-IC(IC370) via the MUX part.

A main signal is input in SAV EAV CODE ADD BLANKING MUTE(IC371) through the 1-H delay (IC372).

A main signal is mixed with the Y signal.

IC(IC362) of the interpolation keeps the continuity of the flaming in case of trick playback by compensating the upper and lower line signal.

It adds SAV and EAV signal in SAV EAV CODE ADD BLANKING MUTE(IC371).

IC371 mute a blanking part and mixes Y and C signal.

The digital output signal goes from connector P2 (8B with 2 A) to the SIF board via the mother board after the change in the ECL signal with TTL to ECL conversion (IC434, 433, 432).

An analog output signal is input in YC DELAY (IC550,551).

The YC signal is decoded by REC-601 DEC(IC552) and becomes a component signal.

The digital component signal is converted to the analog signal by D/A (IC700).

It is output from the VTR with the going BNC connector by the jack board via the mother board from connector P1 (12 C, PB are 13 C, PR about 11 C, PR about Y) via LPF, CLAMP, BUFFER.

An analog composite signal is made with the D/A converted component signal.

As for the Y signal, a sync is mixed by SYNC ADD(IC901) after CLAMP(IC900).

C signal is mixed with the Y signal and is output to VIDEO OUT1, 2 via BUFFER(Q904).

VIDEO OUT1, 2 signals are output from the VTR with the going BNC connector by the jack board via the mother board from connector P1(8C, 9C). VIDEO OUT3 is SUPER MIX(IC980), and it MIXs a character and is output from the VTR with the going BNC connector by the jack board via the mother board from connector P1(10C).

It encodes C signal in ENCODER(IC805) and it MIXs it with the Y signal through BPF(L808, C878).

■ REC/PB

At this board, it is doing main record regenerative signal processing by DVCPRO such as the compression of DVCPRO/the expansion, the sub code signal processing.

◆ The record system

The signal from the V_IN board is inputted from connector P2 (from 10 A) to (15 A) and does shuffling for the compression in REC SHUFFLE (IC3) and REC SHUFFLE MEMORY (IC4) via buffer (IC131,132).

REC COMPRESSION (IC4) compresses a signal.

Then, it connects with the DVC bus which is called REC BD. REC BD is composed with data bus and 3 control signals which are REC BQUIET, REC BDCK and REC BDEN.

An audio signal (from IC143) and VIDEO AUX signal (from IC24) are added to this bus. EE signal is delayed by IC26, 27, 28 and inputted to SELECT EE (IC2) and it is output to REC ECC(IC7).

REC ECC(IC7) does addition of error correction code, deshuffling and addition of a sub code signal (from IC501) using MEMORY(IC8).

The signal is sent to REC DCI(IC9). At the REC DCI, the recorded signal is converted to 41.85 MHz serial signal which is adequate for recording.

The record signal goes from connector P1 (from 6A to 7A) to the RF AMP board via the mother board after the change to ECL signal with TTL to ECL conversion (IC162).

An audio signal is output to connector P2 (17 A from 15B) via the mother board from the AUDIO PROCESS board.

After that, an audio signal is output to the bus which is called REC BD through buffer (IC143) from REC AUDIO(IC6) through buffer (IC142).

VIDEO AUX signal is output from buffer (IC131) and is inputted to IC24.

It extracts and decodes VITC and a closed caption signal here.

It connects with the REC BD bus as the VIDEO AUX signal.

◆ Playback system

There are 2 kinds of playback signals, they are from REC head and PLAY head.

The playback signal comes from the EQ board via the mother board.

The connector is P1 (from 9A to 10A and from 10B to 11B).

The playback signal from the plaback head is inputted from a connector P1 (from 10B to 11B).

Then, the signal enters from ECL to TTL conversion (IC213) to IC22.

It goes from there to PB DCI(IC10) via the selecting circuit.

It enters from there to PB ECC(IC11) via the return REC HEAD/PB HEAD selecting circuit once again to IC22.

PB ECC (IC11) does Error correction, shuffling, expansion and the sub code signal addition by using MEMORY IC (IC12).

The signal is sent to SELECT EE IC (IC2).

The EE signal and the VV signal are selected by the SELECT EE circuit.

The signal is connected with the PB BD bus via BUFFER (IC43).

An audio signal is extracted in PB AUDIO(IC14) from this bus.

The audio signal goes to connector P2(19A) via buffer (IC181).

After that, the audio signal goes to the AUDIO PROCESS board via the mother board.

VITC, a closed caption signal are extracted in VIDEO AUX I/F(IC24) from this bus, and they are encoded by VITC CC ENC (IC24).

A video signal is expanded in PB COMPRESSION(IC13) from this bus.

The video signal is deshuffled by PB SHUF MEMORY(IC17) and PB SHUFFLE(IC16).

Y signal is mixed VITC and closed caption signal and it send to TBC circuit via PRE SHUFFLE IC (IC35).

TBC circuit is composed of TBC/FILTER(IC31) and FRAME MEMORY(IC18,20).

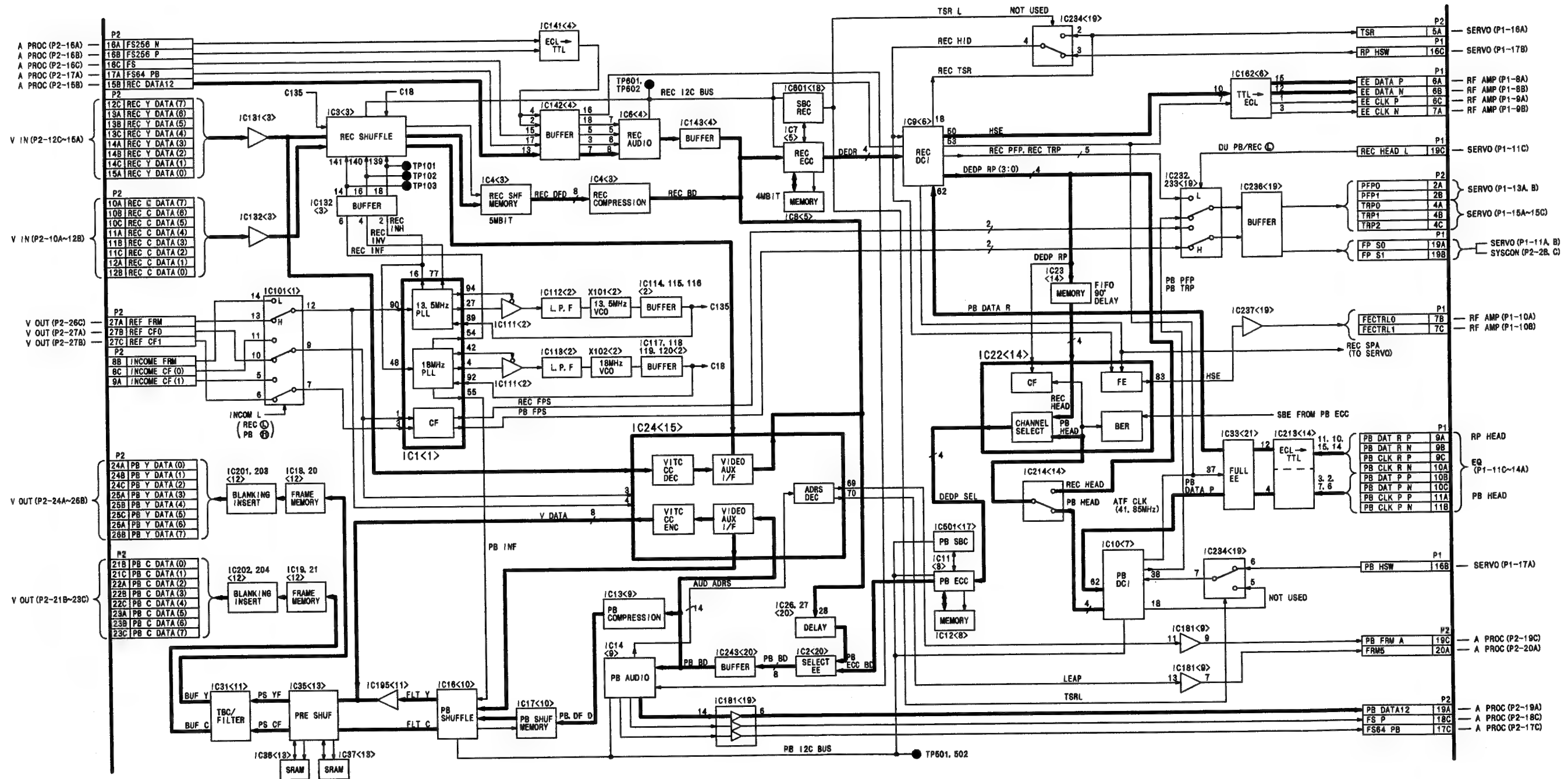
A blanking part is inserted by BLANKING INSERT(IC201,203).

It goes from connector P2 (from 24 A to 26B) to the V_OUT board via the mother board.

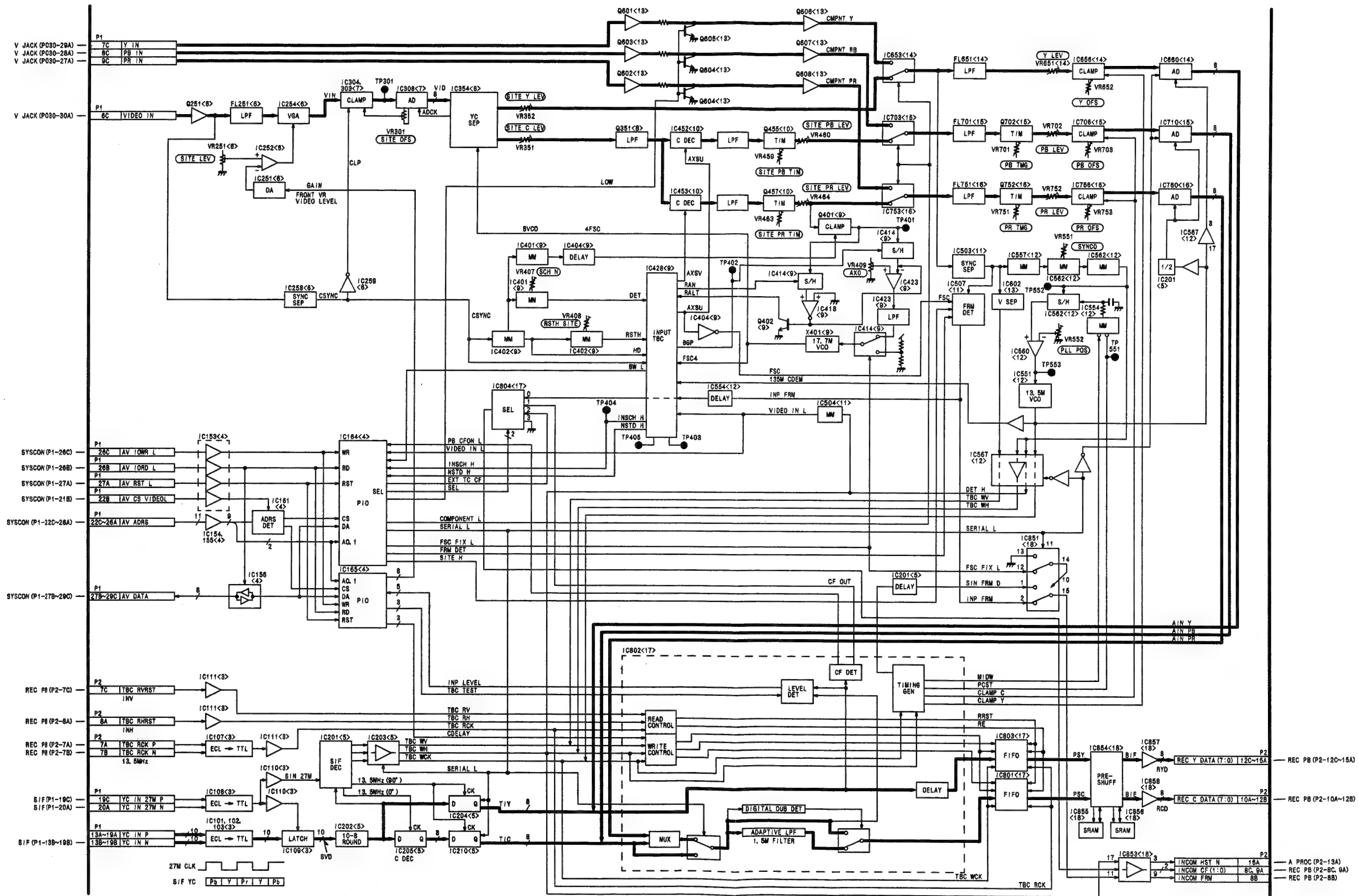
The C signal send to BLANKING INSERT IC (IC202 and IC204) for insert blanking portion to C signal via TBC circuit (the composition is the same as Y process circuit , which is component by TBC/FILTER (IC31) and FRAME MEMORY(IC19 and 21).

And the C signal send to V_OUT p.c-board via connector P2 (21B to 23C) and Mother p.c-board from the BLANKING INSERT IC (IC202 and IC204).

F5 REC PB BLOCK DIAGRAM



F6 VIDEO IN BLOCK DIAGRAM



■ VIDEO IN

It switches three kinds of input signals, an analog component, an analog composite and digital serial component (option).

It makes a non standard signal a standard signal by input TBC and it outputs to the RECPB board.

- It selects 3 input signals.
- Digital Y/C separation, C demodulation
- Input TBC (The non standard signal correspondence)

An analog component input signal is inputted to switching switch (IC653, 703, 753) via the entering buffer from connector P1(7C, 8C, 9C).

An analog composite input signal is inputted from connector P1(6C) and is output to A/D converter (IC308) through LPF(FL251) and gain control amplifier (IC254). Gain control amplifier (IC254) is controlled by VR on the front panel.

The composite signal which was made a digital signal is separated by Y and C(4.43MHz) in YCSEP IC(IC354).

This IC inputs are digital and the output is analog signal.

The sampling frequency is 17.7 MHz and this signal is composed by IC428, X401 and the surrounding circuit.

Y signal is inputted to selecting switch (IC653).

C signal is changed into the Pb, Pr signal with decoder (IC452, 453) and then they are inputted to switching IC (IC703, 753).

The component or the composite of the analog input signal which was chosen with switch IC (IC653, 703, 753) is changed into the digital signal by the A/D converter.

This sampling frequency is 13.5 MHz and the sampling clock is made with circuit of the surrounding of IC551 and IC551.

Then, it is inputted to IC (IC802) of input TBC.

A digital input signal is inputted from connector P1 by the parallel (10 bits) ECL signal via the SIF board. (P1=13A-19A, 13B-19B)

It is changed into the TTL signal at IC108, 101, 102, 103 and it is changed into 8 bits in IC202 and it is inputted to IC (IC802) of input TBC.

Input TBC is used to change a non standard signal into the standard signal.

The main composition is IC802 and the memory IC803, IC801.

The write clock for TBC memory, which is made by IC551.

The read clock for TBC memory, which is supplied from REC PB p.c-board via connector P2-7A, 7B.

The video data signal send to PRE SHUFFLE IC (IC854) from the TBC memory, and it send to connect P2 (12C to 15A, 10A to 12B) via buffer IC (IC857 and 858).

The video data send to REC PB p.c-board via Mother p.c-board from the connector P2 on the Video IN p.c-board.

■ A PROC

[Outline, the characteristic]

It processes a record playback signal by the digital audio signal of DVCPRO.

- The interface of AES/EBU
- The 4 frame memory for the playback at the time of JOG/VAR
- The rate converter (32KHz4ch→48KHz2ch : For the consumer compatibility playback)
- The input selecting circuit (The analog mode, the AES/EBU mode/the serial digital mode)
- The meter circuit

[Flow of the signal]

◆ REC mode

An analog input signal is inputted from connector P1(17C) via the mother board from the ADDA board and then is connected with switching switch (IC600) through BUFFER(IC1), DELAY(IC651, 650).

The AES/EBU input signal with digital input mode enters from the jack board to DIF(IC151) via entering RECEIVER(IC5, 12) to connector P1(8B, 6C) (This IC is the IC of the digital interface of AES/EBU).

It enters (using this IC to compensate the difference of outside the clock phase on this inside of the board) from there to FIFO(IC453) and it is connected with switching switch (IC556) with the serial mode next.

The signal with serial digital input mode is separated from the video signal with the SIF board and goes to the mother board.

CH12 is inputted to connector P2(9C).

CH34 is inputted to connector P2(10B).

It enters DIF(IC200) after choice in CH12 or CH34 with switching switch (IC201) (This IC is the IC of the digital interface of the serial input).

It enters from there to FIFO(IC455) (It uses this IC to compensate the difference of outside the clock phase on this inside of the board).

Next, it is connected with switching switch (IC556) with the AES/EBU mode.

The signal which was switched with switch (IC556) is connected with switching switch (IC600) from INPUT VR(IC600) via DELAY(IC450, 452).

This switching switch does the selecting of analog mode input/digital mode input with 3 types.

After that, through DELAY(IC250, 251) (using this IC for the audio signal, too, to delay a part of being behind in the video signal in in TBC) through MIX(IC750), it goes from connector P2(15B) (the signal name : REC DATA12) through BUFFER(IC6) to the REC PB board via the mother board.

The output of switching switch (IC600) branches and it goes from connector P1(21A) through CUE MIX(IC750) to the CUE board via the mother board.

It uses this to record a signal with digital record mode to the linear track (the CUE track).

◆ PB mode

A playback signal from the REC PB board is inputted to connector P2(19A) via the mother board.

A signal via RATE CONV(IC550) and the signal of passing without dropping are inputted to switching switch

(IC551) from BUFFER(IC1).

RATE CONV(IC550) is the circuit which changes into the clock frequency of DVCPRO in case of playback of the tape which was recorded by the consumer format (the clock frequency is different) (32KHz Being 48KHz in 4ch Converting into 2ch).

As for the output of switching switch (IC551), it goes from OUTPUT VR(IC600) through FIFO(IC602) to FADE(IC751) via SW(IC600) from BUFF MEM CTRL(IC600).

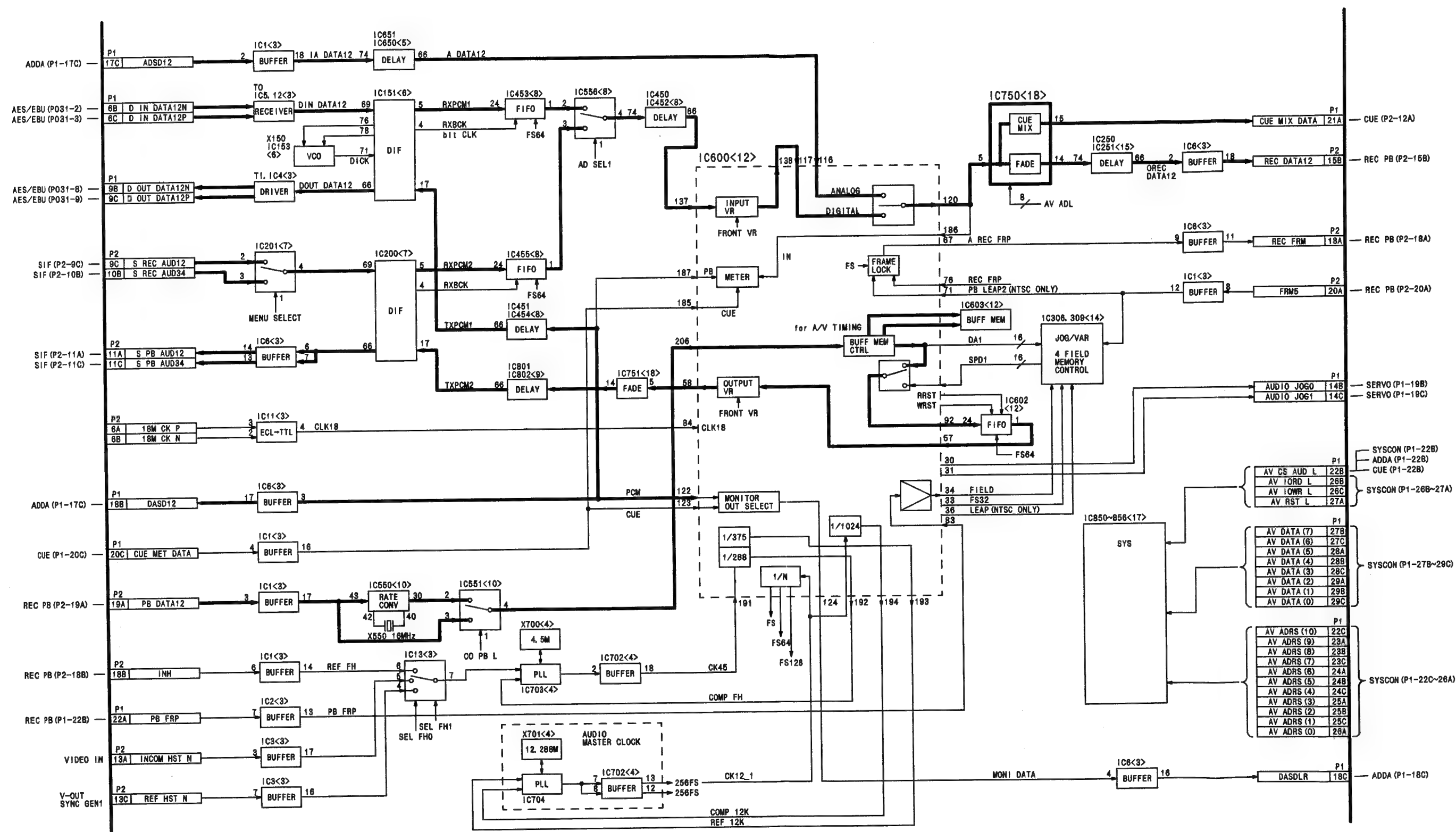
The AES/EBU mode goes from connector P1(8B, 9C) to the AES/EBU output connector of the jack board via DRIVER(IC4, T1) through DIF(IC151) via DELAY(IC451, 454).

The serial mode goes from connector P2(11A, 11C) to the SIF board via the mother board via BUFFER(IC6) through DIF(IC200) via DELAY(IC801, 802).

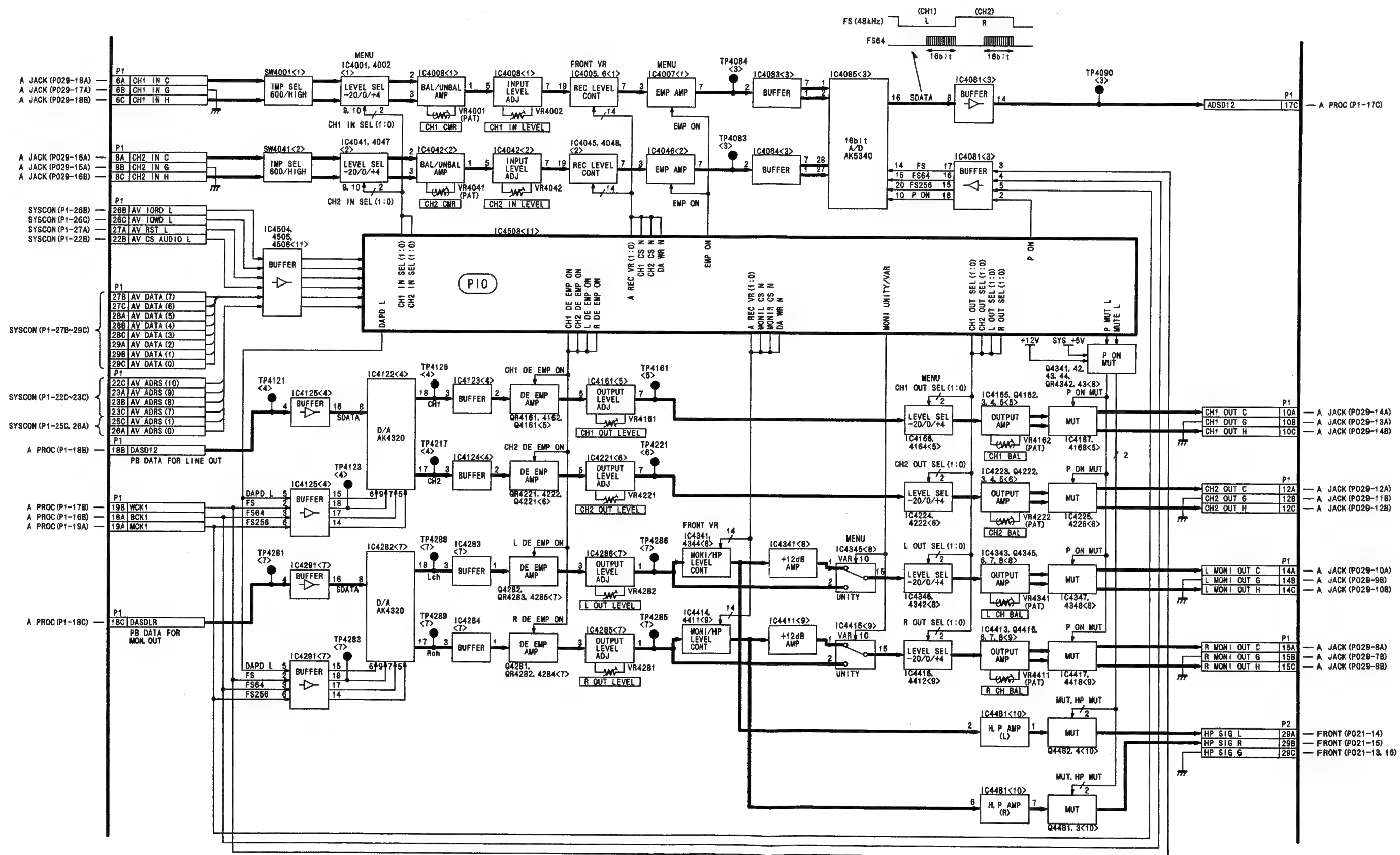
The analog output mode goes from connector P1(18B) to the ADDA board via the mother board via BUFFER(IC8).

The monitor output mode goes from connector P1(18C) to the ADDA board via the mother board via BUFFER(IC6).

F7 A PROC BLOCK DIAGRAM



F8 ADDA BLOCK DIAGRAM



■AD DA

[Outline, the characteristic]

It does the input interface and A/D of the analog audio of CH1, CH2 and it outputs a signal to the AUDIO PROCES board as digital audio.

It does the output interface of the analog audio of CH1, CH2, monitor OUT(L/R CH) and the head phone output.

[Input part]

- The impedance selection : 600 Ω/HIGH(10K Ω)
- The balance input
- Level selection :20/0/+4 dBu
- The A/D converter (Doing the sampling select of 16 bits, 48kHz)

[Output part]

- Level selection :20/0/+4 dBu
- The LOW impedance balance output
- The D/A converter

[Flow of the signal]

◆CH1 input part

A balance analog audio signal from the jack board is input in connector P1(6A, 6B, 6C) via the mother board. With IMP SEL(SW4001) in the board, the impedance of 600 Ω/HIGH(10K Ω) can be selected.

Next, it is inputted to LEVEL SEL circuit (IC4001, 4002).

Here, the input level is - 20/0/+4 dBu. It is possible to select three kinds of levels by menu.

Next, it converts into the unbalanced signal with the BAL/UNBAL AMP(IC4008) circuit.

Next, it is inputted to INPUT LEVEL ADJ(IC4008).

It adjusts a gain from the input by the A/D converter.

Next, it is output to REC LEVEL CONT(IC4005, 6).

Here, the REC level can be changed by VR on the front panel.

Next, it is inputted to EMP AMP(IC4007).

Next, it is inputted to the A/D converter through BUFFER(IC4083).

The resolution is 16 bits and the sampling frequency is 48 kHz. CH1 and CH2 signals are sent from connector P1(17C) via the mother board from the output of the A/D converter via BUFFER(IC4081) at the same time to the A PROC board.

◆CH2 input part

A balance analog audio signal from the jack board is stored in connector P1(8A, 8B, 8C) via the mother board to the same CH1 style.

After that, by IMP SEL(SW4041), the selecting of the impedance of 600 Ω/HIGH(10K Ω) is made of the switch (in the board).

Next, it is inputted to LEVEL SEL(IC4041, 4047).

It selects here by VAR/UNITY and it is inputted to LEVEL SEL(IC4346, 4342).

It sets the selecting of the output level of - 20/0/+4dBu here with the menu.

It goes from connector P1(14A, B, C) to the cannon connector of the jack board via the mother board via MUT(IC4347, 4348) from OUTPUT AMP(IC4343).

MUT does noise mute at the time of power supply ON/OFF.

◆R MONI output part

It is processed in the same way as monitor Lch and the signal of Rch of the D/A converter (IC4282) output is output to DE EMP AMP(QR4282, 4284, Q4281) via BUFFER(IC4284).

After that, via OUTPUT LEVEL ADJ(IC4285), UNITY mode is inputted to switch (IC4415).

The VAR signal can do level variableness here at head phone VR at the front panel to MONI/HP LEVEL CONT(IC4414).

Next, it is inputted to switch (IC4415) through 12dB AMP(IC4411).

It selects here by VAR/UNITY and it sets the selecting of the output level of - 20/0/+4dBu to LEVEL SEL(IC4416, 4412) here with the menu.

It goes from connector P1(15A, B, C) to the cannon connector of the jack board via the mother board via MUT(IC4417, 4418) from OUTPUT AMP(IC4413).

MUT does noise mute at the time of power supply ON/OFF.

◆ head phone output part

The head phone Lch goes via MUT(Q4482, 4) via H.P AMP(IC4481) from the output of MONI/HP LEVEL CONT(IC4341) and goes from connector P2(29A) to the head phone jack of the front panel via the mother board.

The head phone Rch is H.P in the same way as Lch with the output of MONI/HP LEVEL CONT(IC4414). It goes from connector P2(29B) to the head phone jack of the front panel via the mother board via MUT(Q4481, 3) via AMP(IC4481).

◆ The others

PIO(IC4503) decodes a parallel signal from the data bus of AV DATA and distributes it among each circuit as the control signal.

Here, the input level is - 20/0/+4 dBu. It is possible to be select with three kinds of level by menu .

Next, it changes into the unbalanced signal here to BAL/UNBAL AMP(IC4042) and it adjusts a gain from the input to the A/D converter to INPUT LEVEL ADJ(IC4042).

Next, here, it comes to REC LEVEL CONT(IC4045, 4048) variably in the REC level in VR at the front panel.

Next, it is inputted to the A/D converter next through BUFFER(IC4084) by EMP AMP(IC4046).

The resolution is 16 bits and the sampling frequency is 48 kHz.

CH1, 2 signals are sent from connector P1(17C) via the mother board from the output of the A/D converter via BUFFER(IC4081) at the same time to the A PROC board.

◆CH1 output part

A CH1 from the PROC board, 2 audio signals are inputted from connector P1(18B) via the mother board (The data name : DASD12).

After that, it is inputted to D/A converter (IC4122) through BUFFER(IC4125).

It is changed into CH1, 2 analog audio signals here and it is output by 2 systems.

The signal of CH1 is inputted to DE EMP AMP(QR4161, 4162, Q4161) via BUFFER(IC4123).

After that, it is inputted to LEVEL SEL(IC4166, 4164) via OUTPUT LEVEL ADJ(IC4161).

It sets the selecting of the output level of - 20/0/+4dBu here with the menu.

The signal goes from connector P1(10A, B, C) to the cannon connector of the jack board via the mother board via OUTPUT AMP(IC4165) and MUT(IC4167, 4168).

MUT does noise mute at the time of power supply ON/OFF.

◆CH2 output part

In the same way as CH1, it inputs the output of the side of CH2 of the D/A converter to DE EMP AMP(QR4221, 4222, Q4221) via BUFFER(IC4124).

After that, it inputs to LEVEL SEL(IC4224, 4222) via OUTPUT LEVEL ADJ(IC4221).

It sets the selecting of the output level of - 20/0/+4dBu here with the menu.

The signal goes from connector P1(12A, B, C) to the cannon connector of the jack board via the mother board via OUTPUT AMP(IC4223) and MUT(IC4225, 4226).

MUT does noise mute at the time of power supply ON/OFF.

◆L The MONI output part

The audio signal of monitor L/R from the A PROC board is inputted in the same way from connector P1(18C) via the mother board in CH1, 2 (The data name : DASDLR).

After that, it is inputted to D/A converter (IC4282) through BUFFER(IC4291).

It is changed into the analog audio signal of L/R here and it is output by 2 systems.

The signal of Lch is inputted to DE EMP AMP(QR4283, 4285, Q4282) via BUFFER(IC4283).

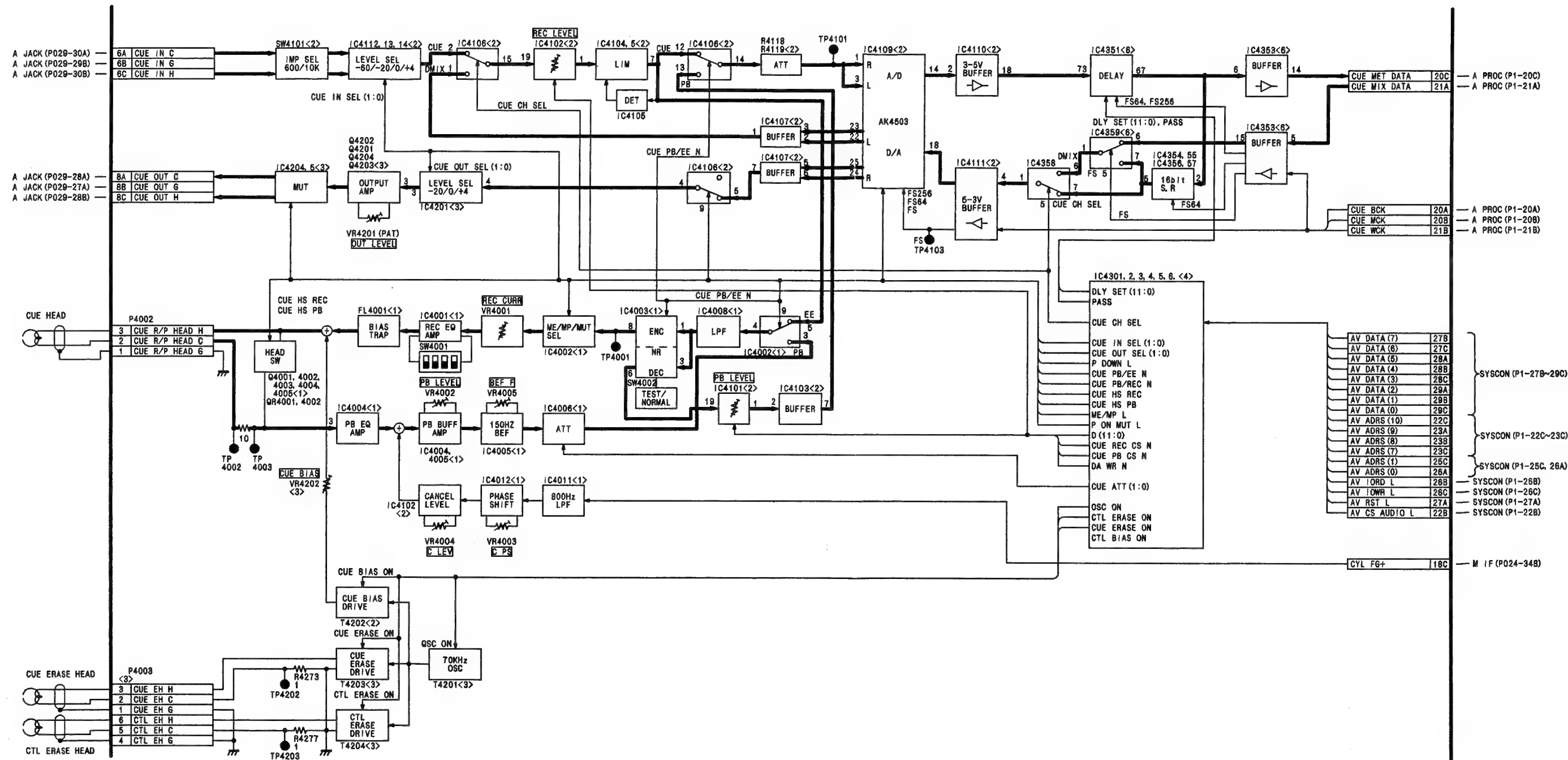
After that, via OUTPUT LEVEL ADJ(IC4286), UNITY mode is inputted to switch (IC4345).

VAR signal is inputted to MONI/HP LEVEL CONT(IC4341).

Here, level variableness is made at head phone VR at the front panel.

Next, it is inputted to switch (IC4345) through 12dB AMP(IC4341).

H2 CUE BLOCK DIAGRAM



■ CUE

[Outline, the characteristic]

It records and playback a CUE signal in the linear track.

- The Impedance selection : 600 Ω /10K Ω
- Input level selection : -60/-20/0/+4 dBu (-60 is for the microphone).
- Output level selection : -20/0/+4 dBu
- The AD/DA converter
- The 70KHz oscillator (The CUE bias, the CUE erasure, the CTL erasure)

[Flow of the signal]

◆REC mode

As for the CUE input (the cannon connector) of the jack board, the selecting of the impedance of 600 Ω /10K Ω is made of switch (in the board) in entering IMP_SEL(SW4101) from connector (8A, B, C).

Next, here, it is - 60/-20/0/+4 to LEVEL_SEL(IC4112, 4113, 4114) it is possible to be select with the 1st menu of four kinds of input levels of dBu.

Next, it enters switch (IC4106), this switch switches the signal to record to the CUE track and can switch CUE and D_MIX.

Next, this IC which goes to REC_LEVEL(IC4102) can do REC level variably in VR at the front desk in EVR.

Next, it enters a switch (the 5th terminal of IC4002) and a switch (the 12nd terminal of IC4106) via LIM(IC4104, 4105).

The signal to record to the head encodes Dolby B in NR_ENC(IC4003) after that from the switch (entering from the 5th terminal of IC4002 and outputting from the 4th terminal) to LPF(IC4008) and here, it is selecting a record electric current to ME/MP/MUT_SEL(IC4002) by the kind of the tape.

After that, here, it sets a record electric current to REC_CURR(VR4001), and next, it MIXs a bias signal next via BIAS_TRAP(FL4001) to REC_EQ_AMP(IC4001) and it records it with the head from connector P4002(3) and in record, the side of TP4003 falls to GND with the HEAD_SW (4005 from Q4001) circuit.

The signal which entered from LIM(IC4104, 4105) to the 12nd of switch (IC4106) is DELAY(IC4351), changing the mode signal of 3 V into the mode signal of 5 V in 3-5V_BUFFER(IC4110) to A/D(IC4109) via ATT(R4118, 4119) (5 frames of digital mode signals delay 5 frames of CUE signals here because it is behind in them).

It uses the signal which went from BUFFER(IC4353) to the A_PROC board via connector (20C) for the meter display, the monitor mode (containing a head phone) output.

The signal of the jack board for the CUE output shifts 16-bit data back here from DELAY(IC4351) to 16bitS.R (4357 from IC4354).

This is because the D/A converter processes 16 bits of the second half in 32 bits.

Next, it changes the mode signal of 5 V into the mode signal of 3 V in 5-3V_BUFFER(IC4111) via switch (IC4358) and it inputs it to D/A converter (IC4109).

It inputs the signal which was changed into being analog to LEVEL_SEL(IC4201) via the switch (the output of 4th of the 5th input of IC4106) through BUFFER(IC4107).

Here, it is possible of three kinds of - 20/0/+4 of output levels to be select with the menu.

It goes from connector (8A, B, C) to the cannon connector of CUE_OUT of the jack board through that it is possible to do passing MUT(IC4204, 5) to OUTPUT_AMP (4204 from Q4201).

The digital CUE_MIX signal (the signal name : CUE_MIX_DATA) passes switch (IC4359) and switch (IC4358) via entering BUFFER(IC4353) from the A_PROC board via the mother board to connector (21A), changes 5 V into 3 V in 5-3V_BUFFER(IC4111) and goes to D/A converter (IC4109).

The signal which was changed into being analog goes from 22, the 23rd terminal to the 1st terminal of switch (IC4106) through BUFFER(IC4107).

Since this, the flow of the record signal to the CUE head is same as CUE_IN.

◆PB mode

The playback signal from the CUE head goes to entering PB_EQ_AMP(IC4004) at connector P4002(2).

The P4002(3) side shoten to GND with the HEAD_SW (4005 from Q4001) circuit. As for the output of PB_EQ_AMP(IC4004), it goes from PB_BUFFER(IC4004, 4005) to 150Hz_BEF(IC4005) (being the filter to remove noise from the cylinder).

Next, it makes attenuate because the playback level of the CUE signal becomes high when the tape speed becomes high-speed in (this place to ATT(IC4006) when searching.

It is select at 0/12 dB of the attenuation level according to the speed.

Next, it decodes Dolby B in NR_DEC (entering from the 3rd terminal of IC4003 and outputting from the 6th terminal) after that from the switch (entering from the 3rd terminal of IC4002 and outputting from the 4th terminal) to LPF(IC4008) and it goes to PB_LEVEL(IC4101).

This IC can do PB level variably in VR at the front panel in EVR.

Next, the signal which was stored in the 13rd of switch (IC4106) through BUFFER(IC4103) is processed in the flow to be same as the REC mode as to connector (8A, B, C) with connector (20C) by.

The CUE_MIX signal which entered from connector (18C) goes to CANCEL_LEVEL(IC4102) through PHASE_SHIFT(IC4012) through 800Hz_LPF(IC4011).

It makes cancel the CUE_MIX component which dives from the cylinder which is contained in the playback signal from the CUE head by MIXING in the output part of PB_EQ_AMP(IC4004).

It does a phase adjustment in VR4003 of PHASE_SHIFT(IC4012), it adjusts a level in VR4004 of CANCEL_LEVEL(IC4102) and it makes cancel FG component.

■ EQ

[General]

The EQ circuit compensates a frequency and a phase in the playback signal from the head that it is possible to recover in the best condition.

There are a circuit for REC HEAD and a circuit for PB HEAD.

The circuit for PB HEAD has the circuit of the viterbi decode.

The playback of REC HEAD in consumer playback but at this time, it uses a circuit for PB HEAD.

- One chip Equalizer PLL IC which has Delay circuit.

◆ PB HEAD mode

A signal from RF AMP is input to connector (26A, 26B) via the mother board.

The signal for ATF goes from 9 A of connectors through PRE FILTER(IC5408) through AMP (Q5108 from Q5101) to the servo board via the mother board. PRE FILTER(IC5408) is composed of BPF and amplifier and BPF makes pass the signal of 470KHz and 680KHz.

The gain of the amplifier can be adjusted by EVR.

The main signal is input in switching IC (IC5101) through AMP (Q5108 from Q5101) and goes to MAIN EQ(IC5408) through AGC(IC5102).

MAIN EQ can adjust gain, phase and group delay by EVR.

AUTO EQ(IC5408) does the automatic fine adjustment of the equalizer for the compatible playback to improve an error rate.

After that, it enters a $1 + D$ circuit.

The $1 + D$ circuit processes $1/(1-D)^2$ in "the interleaved NRZI modulation" of the record mode.

It returns this to the origin and it makes a signal "1" but it is possible to return to the form before the modulation of the record mode by the tape head mode if processing "1+D" with the circuit because the processing of "1-D" is done because it is the differential characteristic.

Therefore, it is doing "1+D" in IC5408.

$$1/(1-D)^2(1-D)(1+D)=1$$

After that, it extracts a clock signal in PLL(IC5408) and it outputs PB DAT, PB CLK signal from IC5408.

The PB DAT signal which passed buffer (IC5802) is converted into the ECL signal with TTL to ECL conversion (IC5807) and goes from connector (13C, 14A) to the REC PB board via the mother board.

IC5409 controls the PLL loop of PLL(IC5408).

Normally, PLL is ON.

When the envelope level becomes $1/3$, ENV DET(IC5407) makes function IC5409 OFF and cuts a loop and makes PLL a hold condition.

This works as the PLL malfunction prevention by the envelope level decline.

It takes out a signal from the back of the $1 + D$ circuit of IC5408, it makes viterbi decode a digital signal with A/D converter (IC5603)(8bit, 41.85MHz) after the amplification in (PB VTB)AMP (8 from IC5601, 2, Q5601) and it sends it to VTB(IC5901).

◆ REC HEAD mode

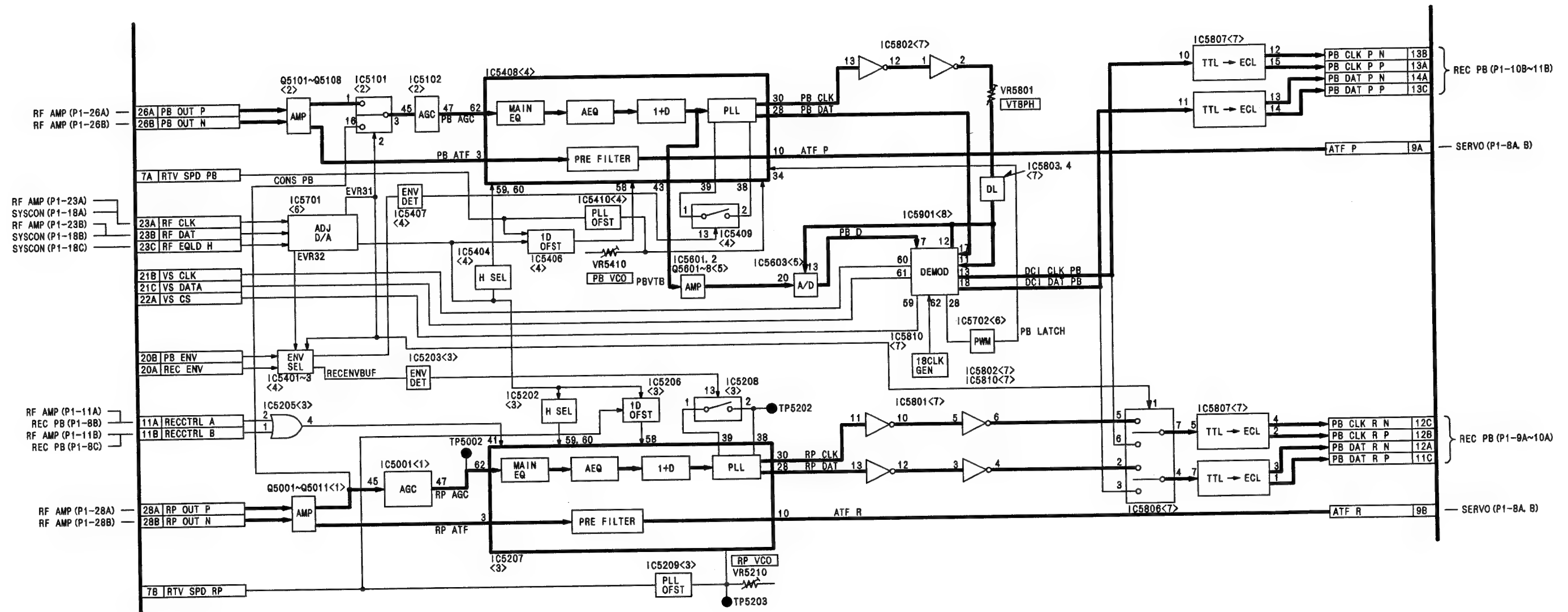
A signal from RF AMP is input in connector (28A, 28B) via the mother board.

The function of each circuit (IC) of the after signal processing is the same as the PB HEAD mode. There is not viterbi decode on this side.

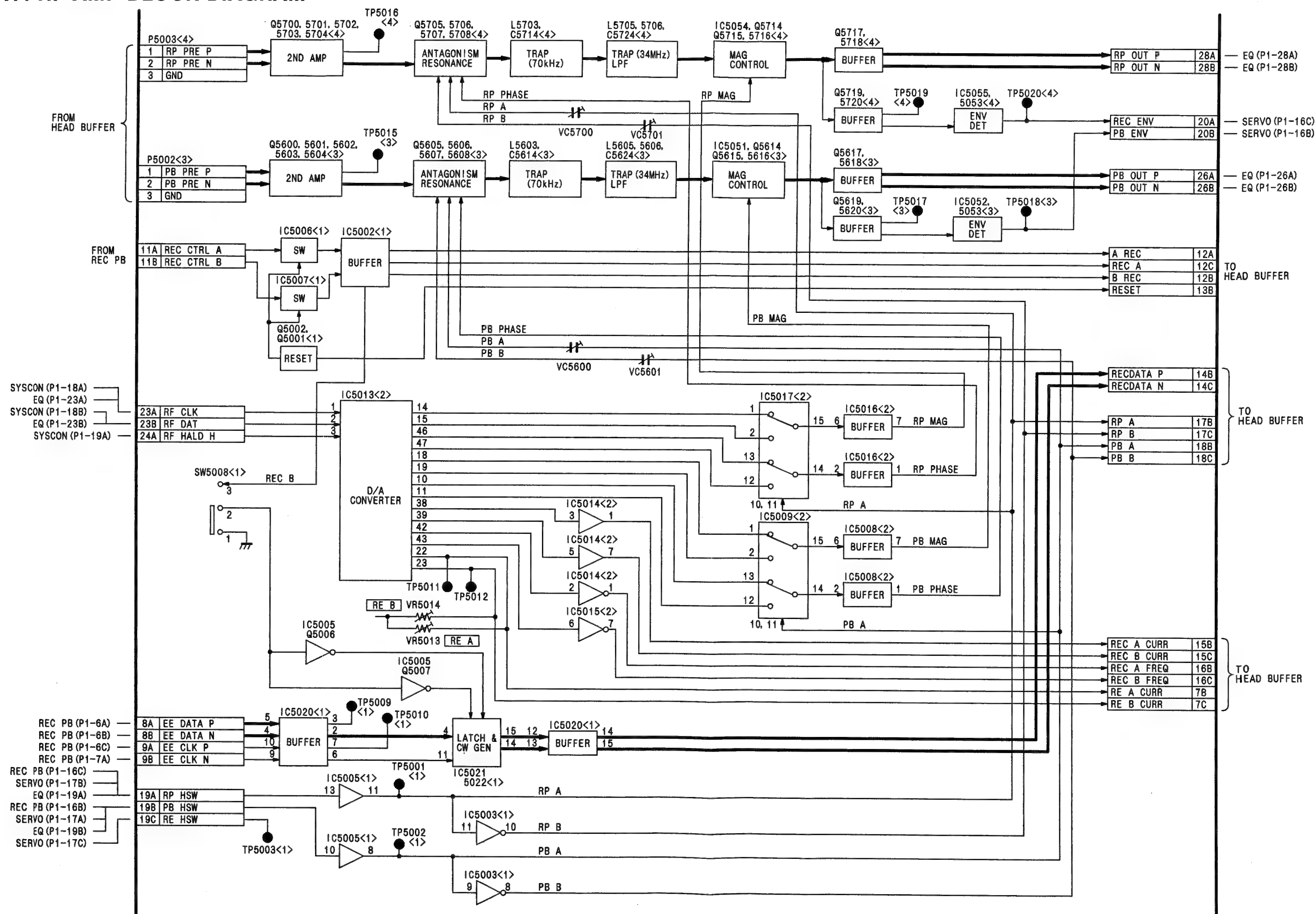
It is recorded by the consumer format and it does the playback of the tape in REC HEAD but the equalizer circuit uses the side of PB HEAD.

The switching circuit for its purpose is IC5101 of the switch, 5806.

H3 EQ BLOCK DIAGRAM



H4 RF AMP BLOCK DIAGRAM



■ RF AMP

In the REC mode, it is used as the buffer for the signal between REC PB and HEAD BUFFER, in the PB mode it is used as a pre equalizer between HEAD BUFFER and EQ and also it converts a control signal to digital by D/A circuit and sends them to the HEAD BUFFER board via the data bus.

- The carrier wave generator for the test
- REC AMP buffer
- The D/A converter
- pre equalizer

◆ REC signal

REC signal from the REC PB board is input to connector (8A, 8B, 9A, 9B) via the mother board. It inputs to LATCH CW GEN (IC5021, 5022) through BUFFER(IC5020).

Normally, it hangs a latch on this place.

In the test mode (short-circuiting among 2-3 of SW5008), make 20.9-MHz CW for maintenance, and it records and it uses this for the measurement of C/N. Then, it goes to the HEAD BUFFER board via connector (14B, 14C) and the mother board from BUFFER(IC5020).

◆ The playback signal of REC HEAD

The playback signal of REC HEAD from the HEAD BUFFER board is inputted to connector P5003 via the mother board.

It enters ANTAGONISM RESONANCE (5708 from Q5705) through 2ND AMP (5704 from Q5700).

Here, a phase and level adjustment of every channel are done by EVR.

After that, it attenuates the CUE erase and bias frequency component (70KHz) at TRAP(L5703, C5714) and it is sent to TRAP LPF(L5705, L5706, C5724).

TRAP LPF is composed of composition in the 34-MHz trap and LPF.

Next, it goes to MAG CONTROL (Q5716 from IC5054, Q5714).

Here, it adjusts a gain by EVR.

Next, it goes from BUFFER(Q5717, 5718) to the EQ board via the mother board and connector (28A, 28B).

◆ PB HEAD playback signal

The playback signal of PB HEAD from the HEAD BUFFER board is inputted to connector P5004 via the mother board.

The signal goes from connector (26A, 26B) to the EQ board via the mother board, being similar flow as the playback of REC HEAD.

■ HEAD BUFFER

HEAD BUFFER is interface board which delivers a signal to REC HEAD, PB HEAD, RE HEAD of drum.

HEAD BUFFER is installed on the frame among the a mechanism chassis and H boards.

A connection with the drum is connector (P5002, 5003) with two sheets of flexible boards.

There is no adjustment for the playback mode.

[Composition]

- Two sets of oscillation circuits of the rotary erase (RE)
- Two sets of REC AMP circuits
- Two sets of HEAD AMP (of REC HEAD and for PB HEAD) and rotary erase circuits

Signal Flow

◆ Rotary Erase

The RE CONTROL circuit (IC5008, IC5025, IC5027, Q5300, Q5301, IC5009, IC5026, IC5028, Q5330, Q5351) controls RE OSC (Q5302, Q5303 and Q5352, Q5353) in the control signal with ON/OFF and electric current value from the REC PB board.

It applies an erasure electric current to the drum with connector P5002 (from 8 to 11).

The erasure frequency is about 34 MHz and the electric current is from 120 to 130 mA .

◆ Record

The record signal is supplied from REC AMP via mother board. Then the signal is supplied from connector (13A,13B), RF board and goes to the drum from P5002 via R/P SW. The recording current is 50 to 70 mA pp. In REC AMP(Q5405, 5408, 5409, 5505, 5508, 5509), the adjustment of the frequency characteristic, the record electric current is made from the outside.

The playback signal from REC HEAD enters from the drum to R/P SW via P5002(3, 4, 5, 6) then goes to HEAD AMP(IC5060)

It goes from BUFFER(Q5700,5701) to the RF AMP board through the mother board via connector (23A,23B). R/P SW is the circuit which selects the connection of the head. R/P SW is composed of Q5401 to Q5405 and Q5501 to Q5504.

In record, it connects with REC AMP and in playback, it connects with HEAD AMP.

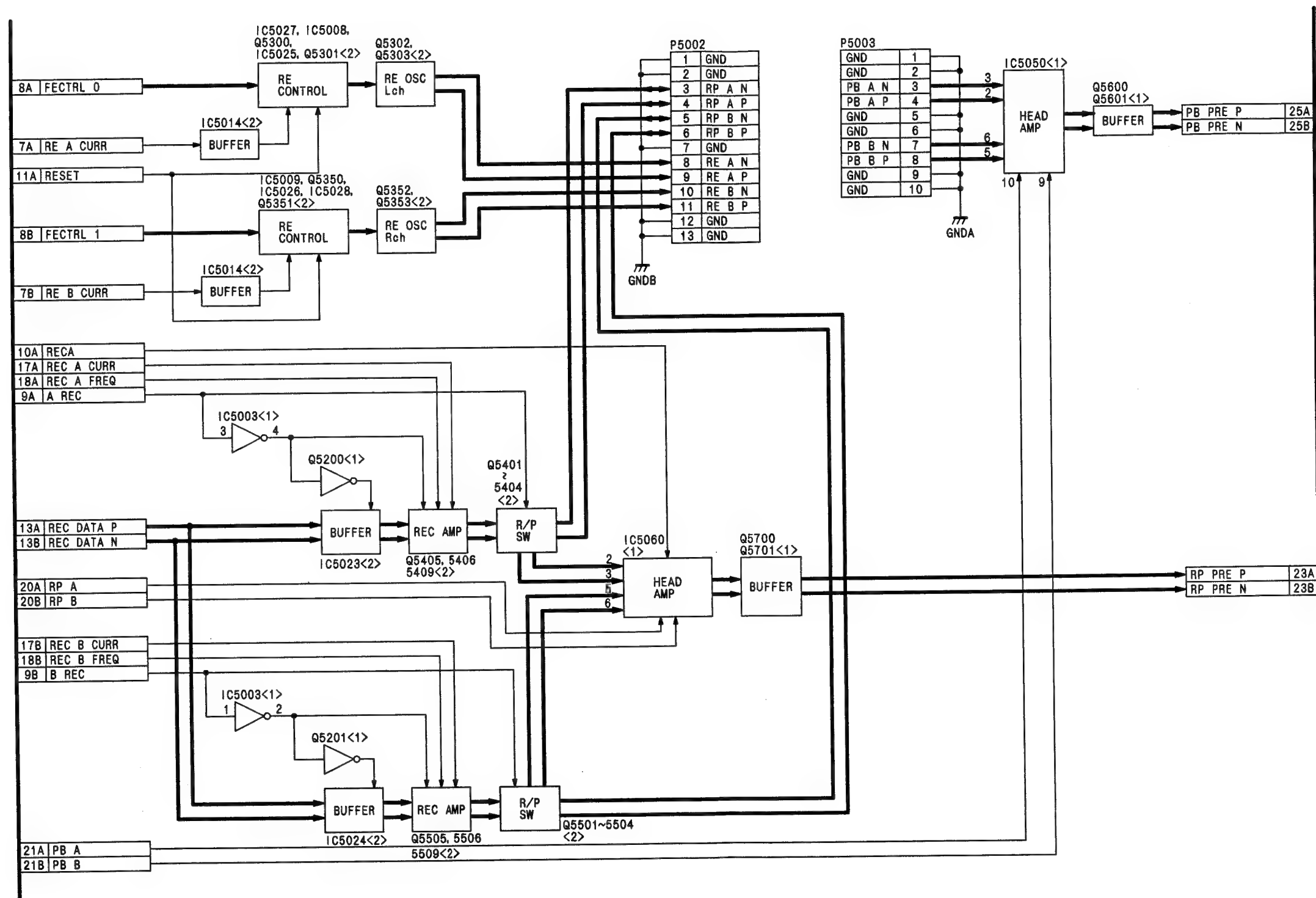
◆ Playback

There are two kinds of playback mode, one is by REC head and the other is by PLAY head.

The playback signal from REC HEAD goes to HEAD AMP(IC5060) from Drum via P5002 (3, 4, 5, 6 pin). It goes to RF AMP board through the mother board via connector (23A,23B).

The playback signal from PLAY HEAD goes to HEAD AMP(IC5050) from Drum via P5003 (3, 4, 7, 8 pin). It goes to RF AMP board through the mother board via connector (25A,25B).

HEAD BUFFER BLOCK DIAGRAM



SECTION 2

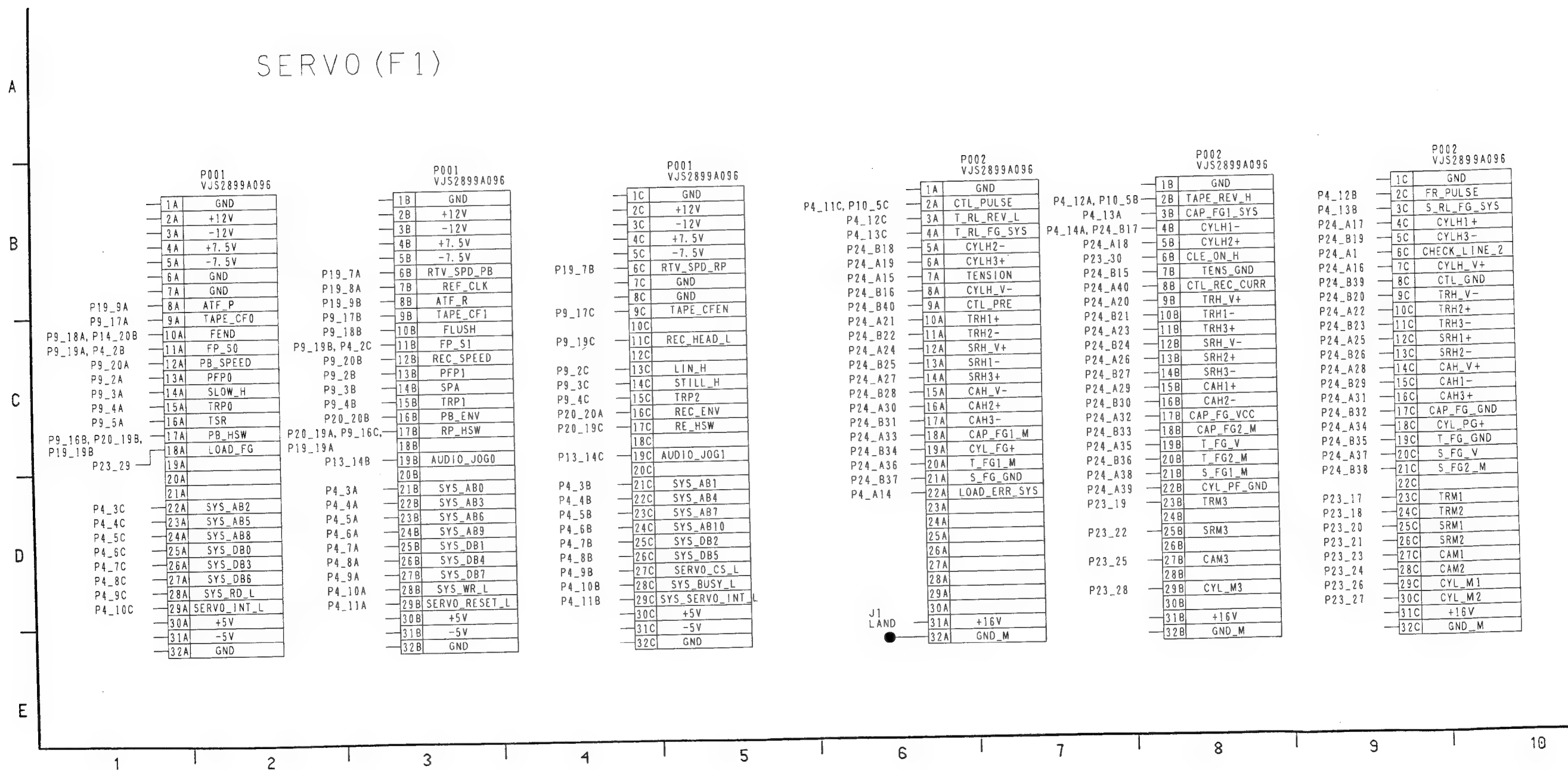
SCHEMATIC DIAGRAMS

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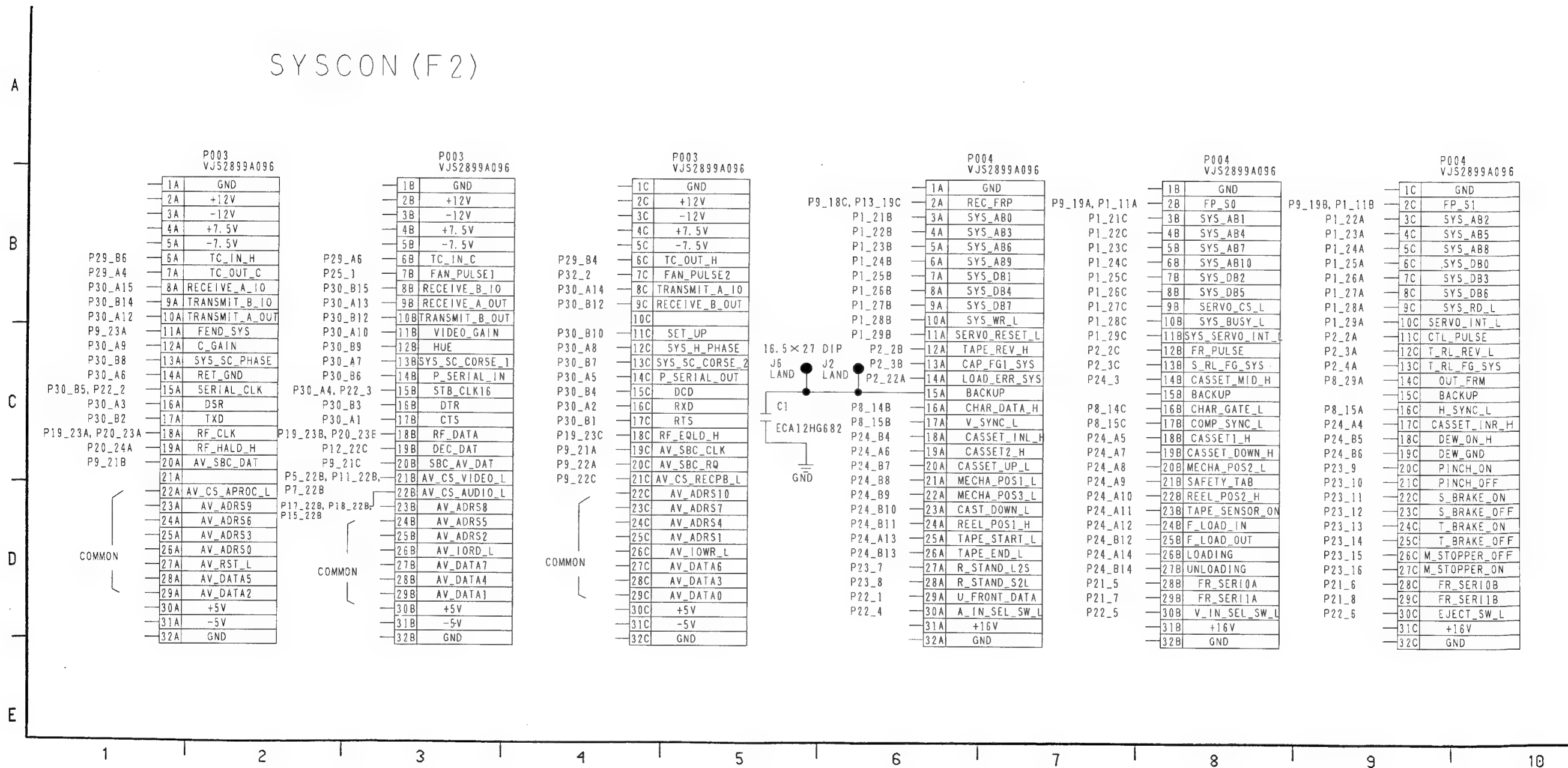
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F8 ADDA -----	2-147	FRONT CPU SUB -----	2-200
H2 CUE -----	2-159	FRONT SW -----	2-201
H3 EQ -----	2-165	FRONT VR1 -----	2-205
H4 RF AMP -----	2-174	FRONT VR2 -----	2-205
HEAD BUFFER -----	2-179	AES/EBU -----	2-206
VS JACK -----	2-181		

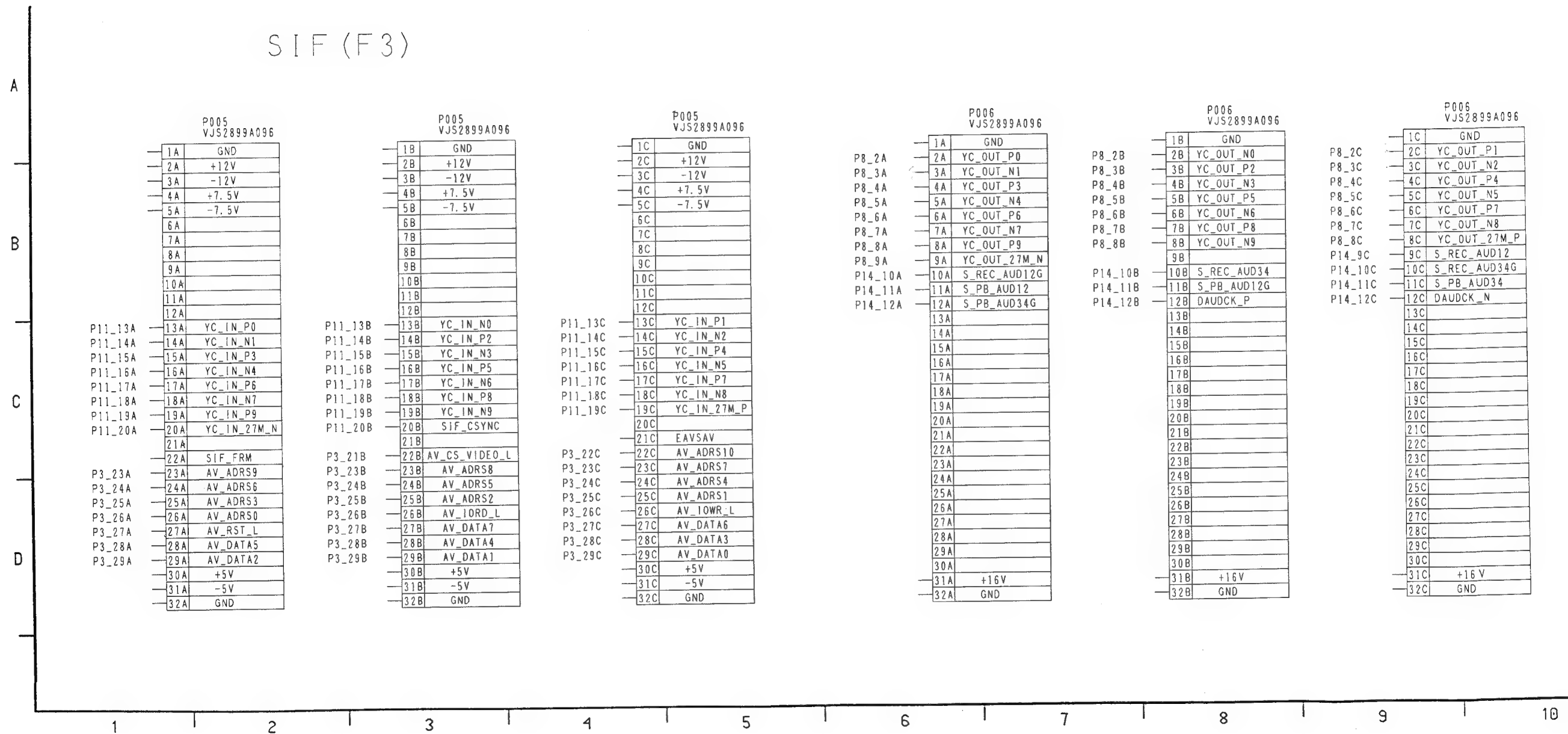
MOTHER (1/11) SERVO (F1) SCHEMATIC DIAGRAM



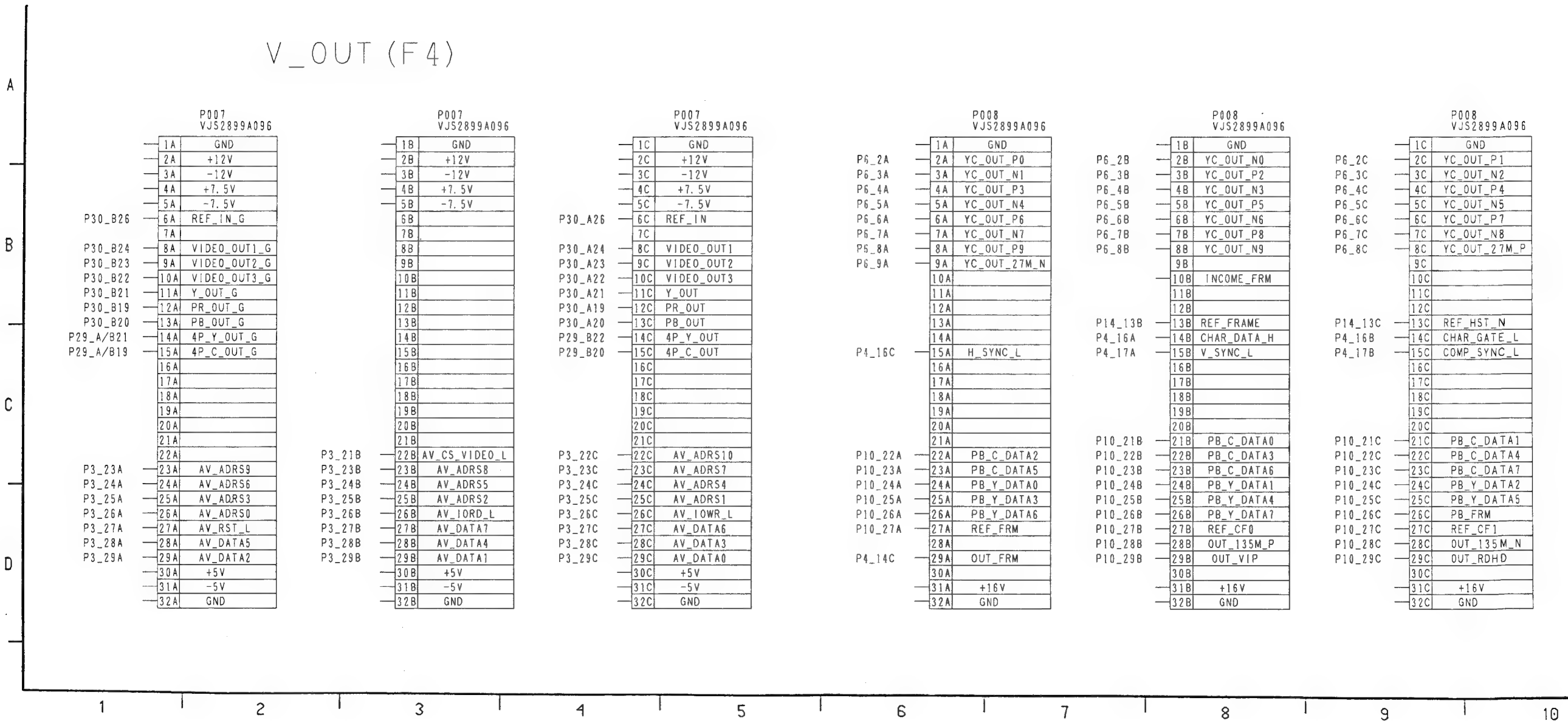
MOTHER (2/11) SYSCON (F2) SCHEMATIC DIAGRAM



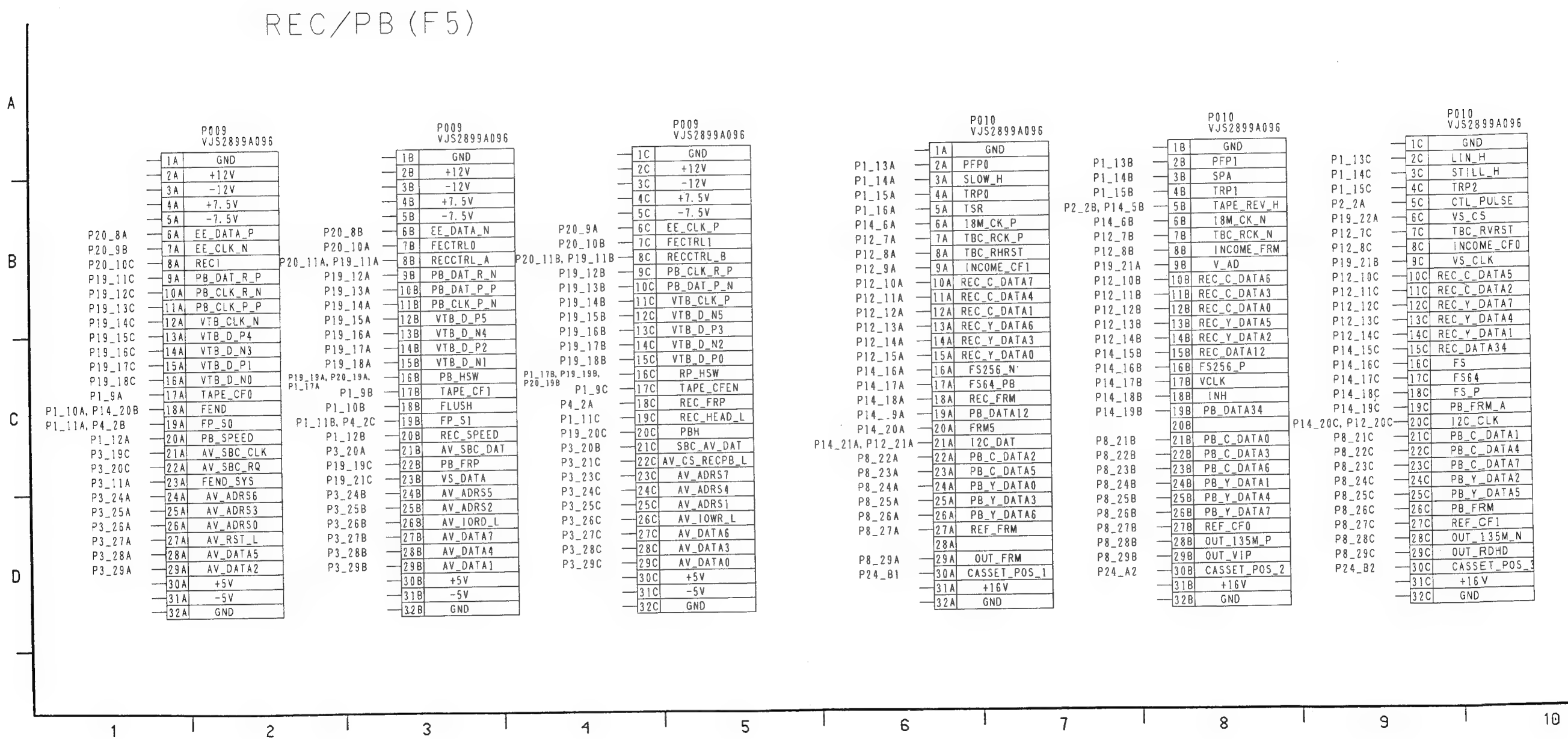
MOTHER (3/11) SIF (F3) SCHEMATIC DIAGRAM



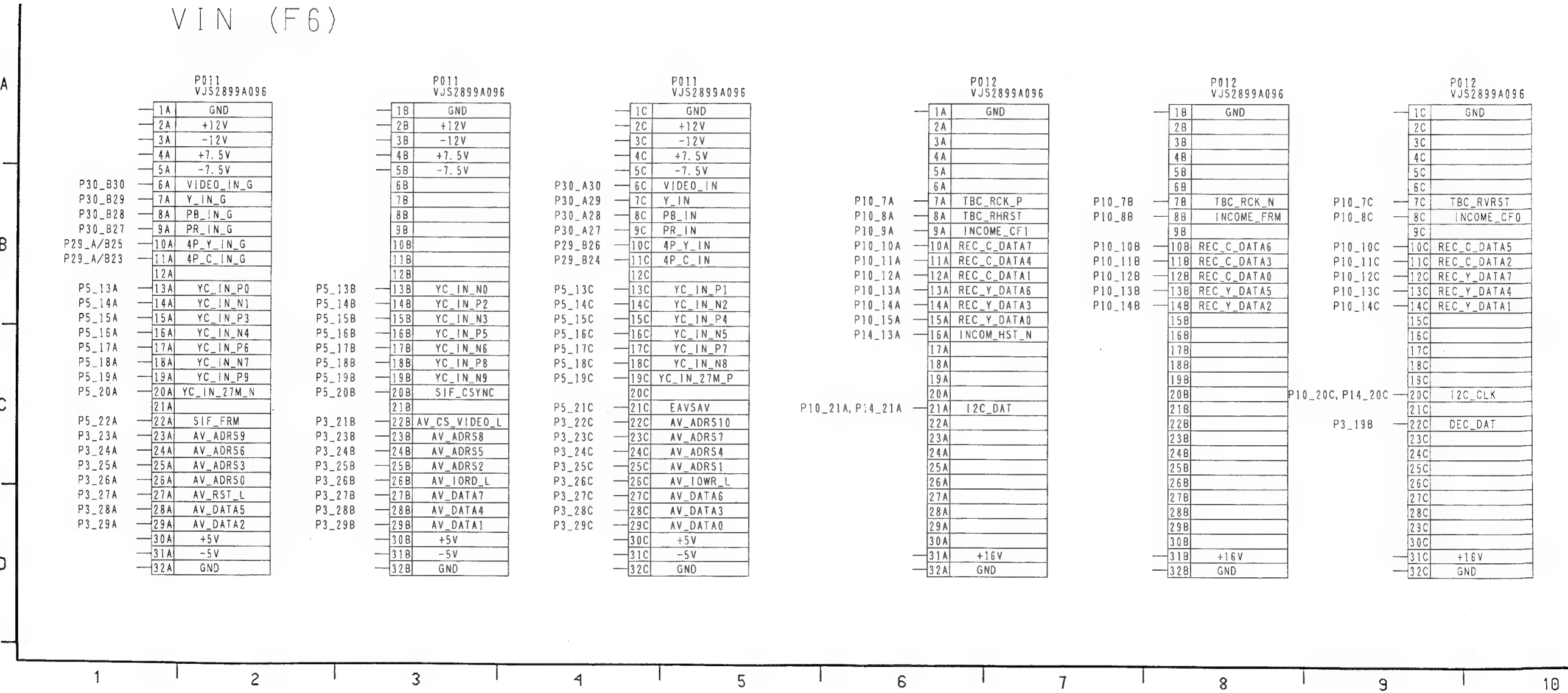
MOTHER (4/11) V OUT (F4) SCHEMATIC DIAGRAM



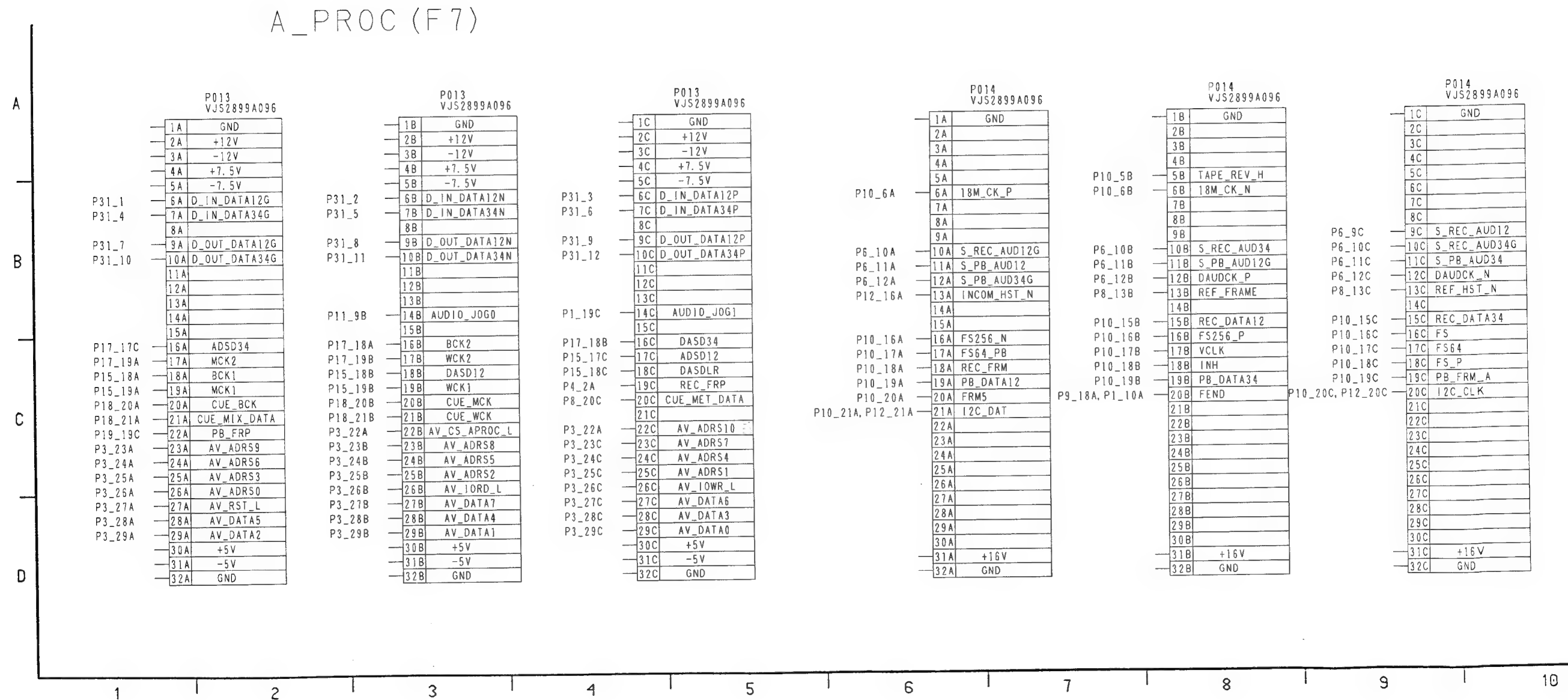
MOTHER (5/11) REC PB (F5) SCHEMATIC DIAGRAM



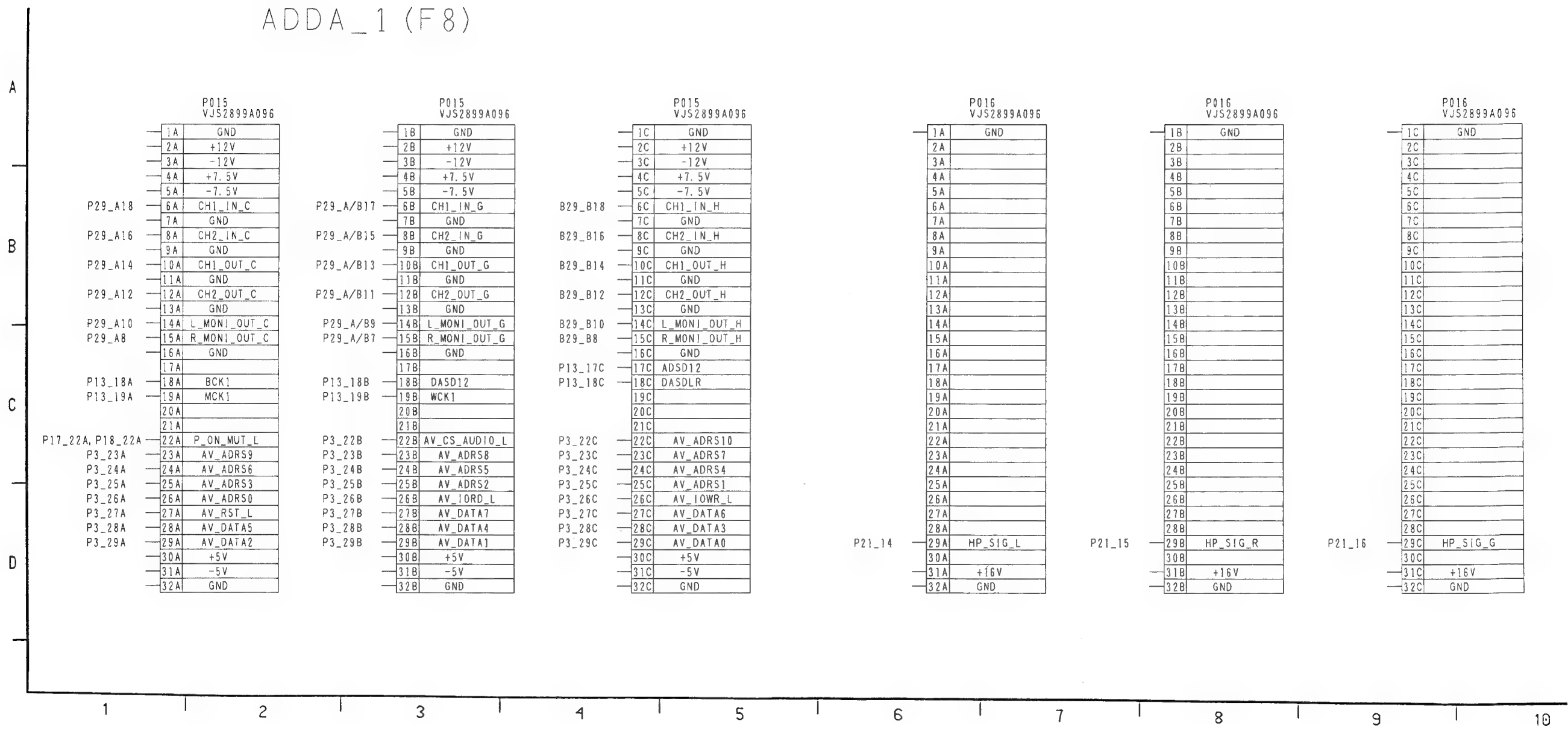
MOTHER (6/11) V IN (F6) SCHEMATIC DIAGRAM



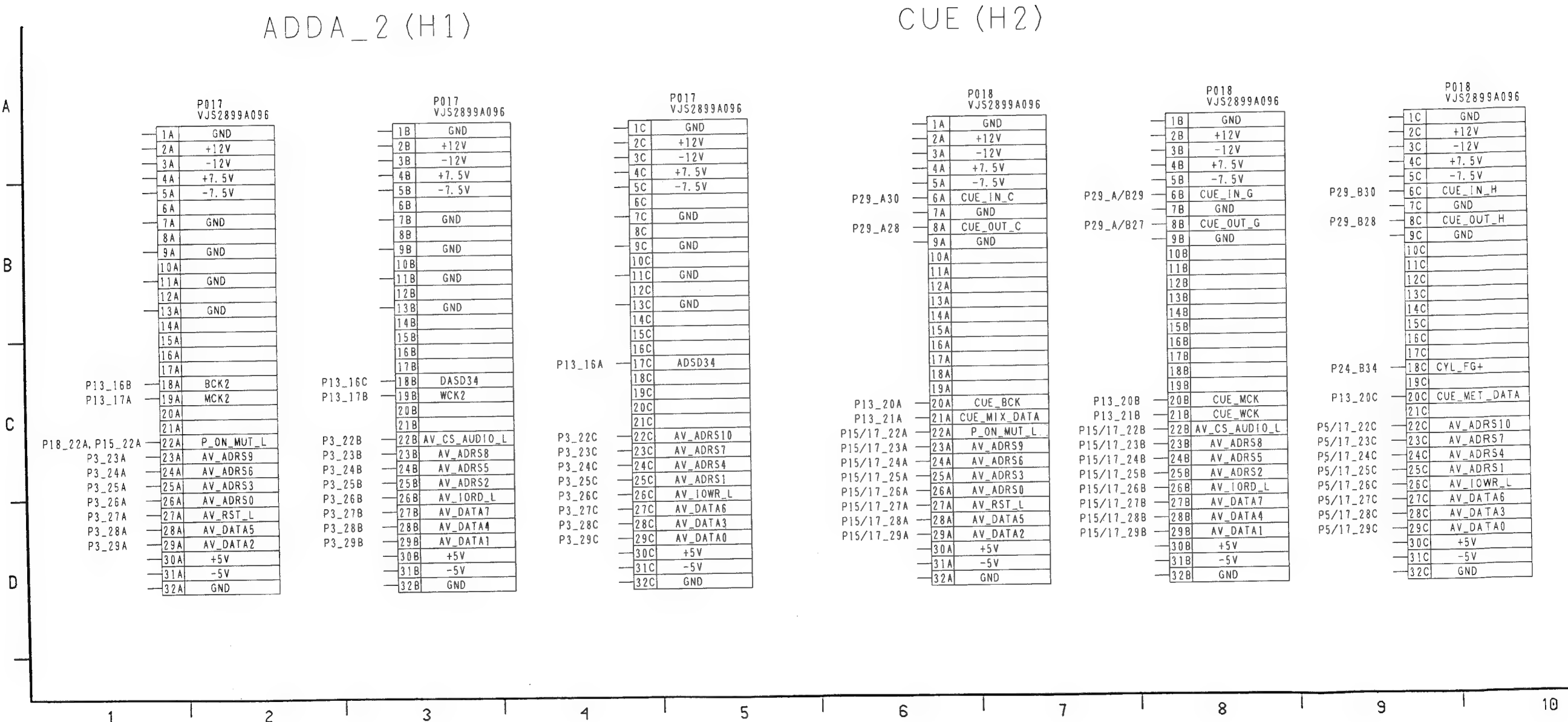
MOTHER (7/11) A PROC (F7) SCHEMATIC DIAGRAM



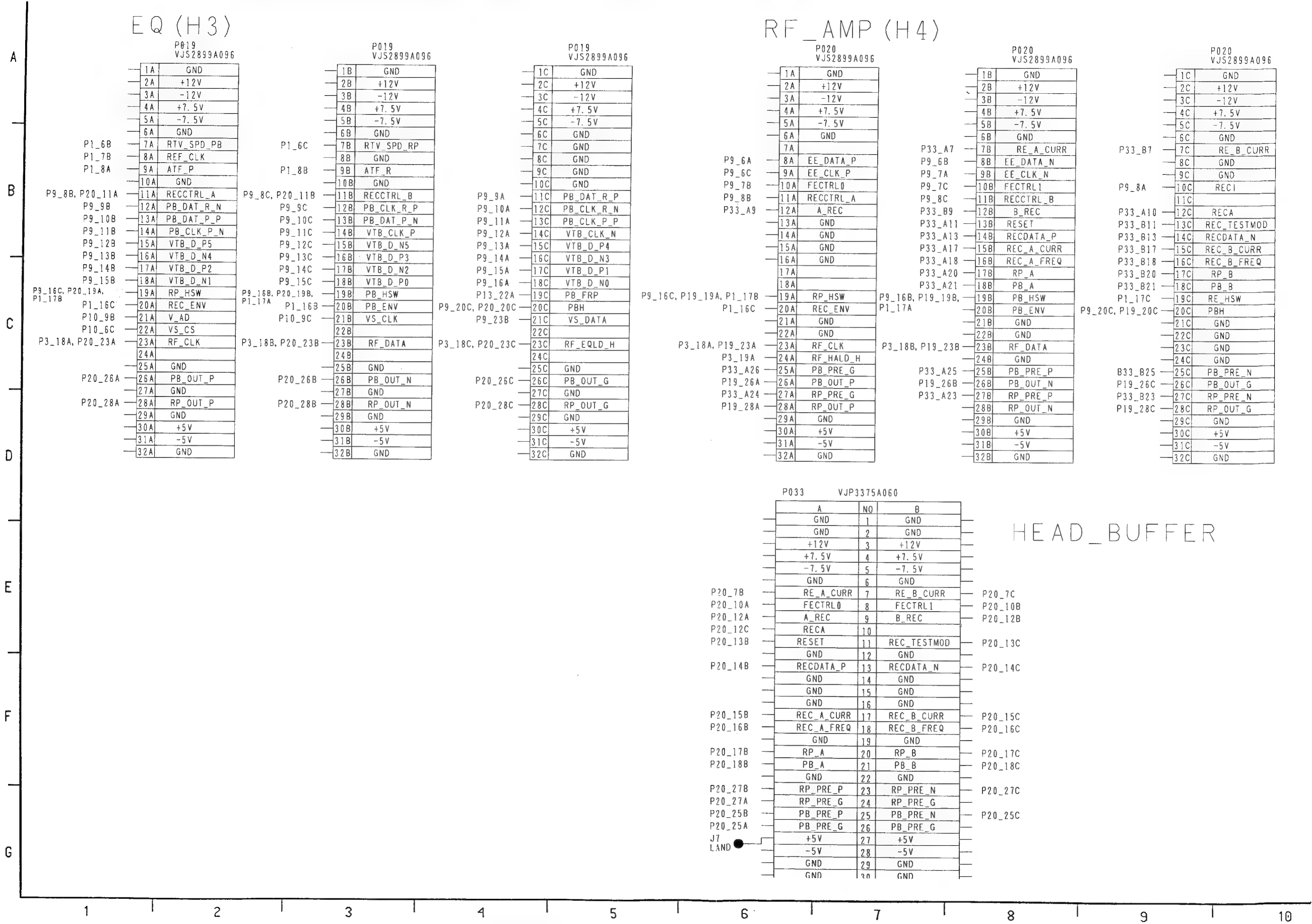
MOTHER (8/11) ADDA 1 (F8) SCHEMATIC DIAGRAM



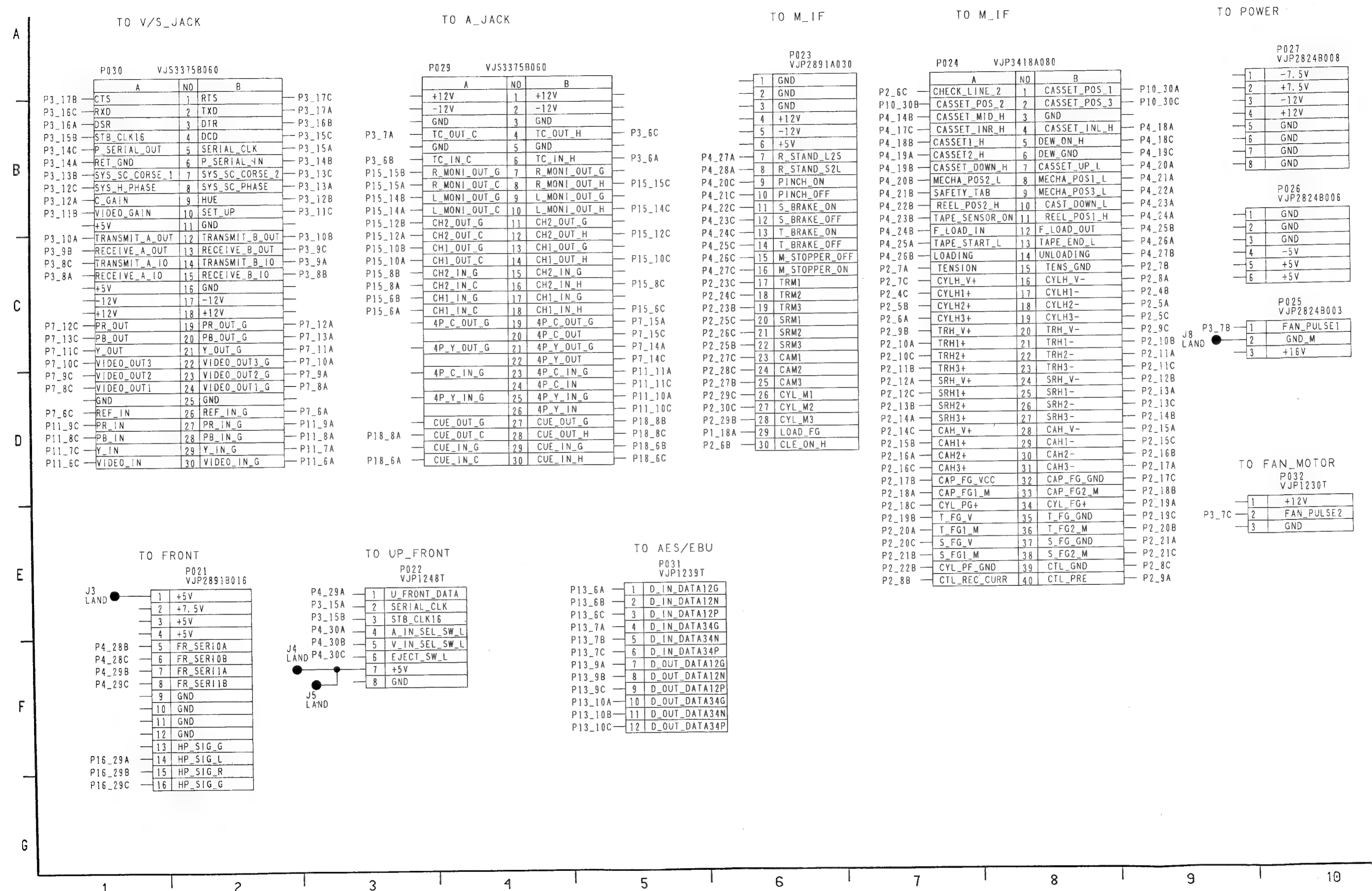
MOTHER (9/11) ADDA 2 (H1)/CUE (H2) SCHEMATIC DIAGRAM



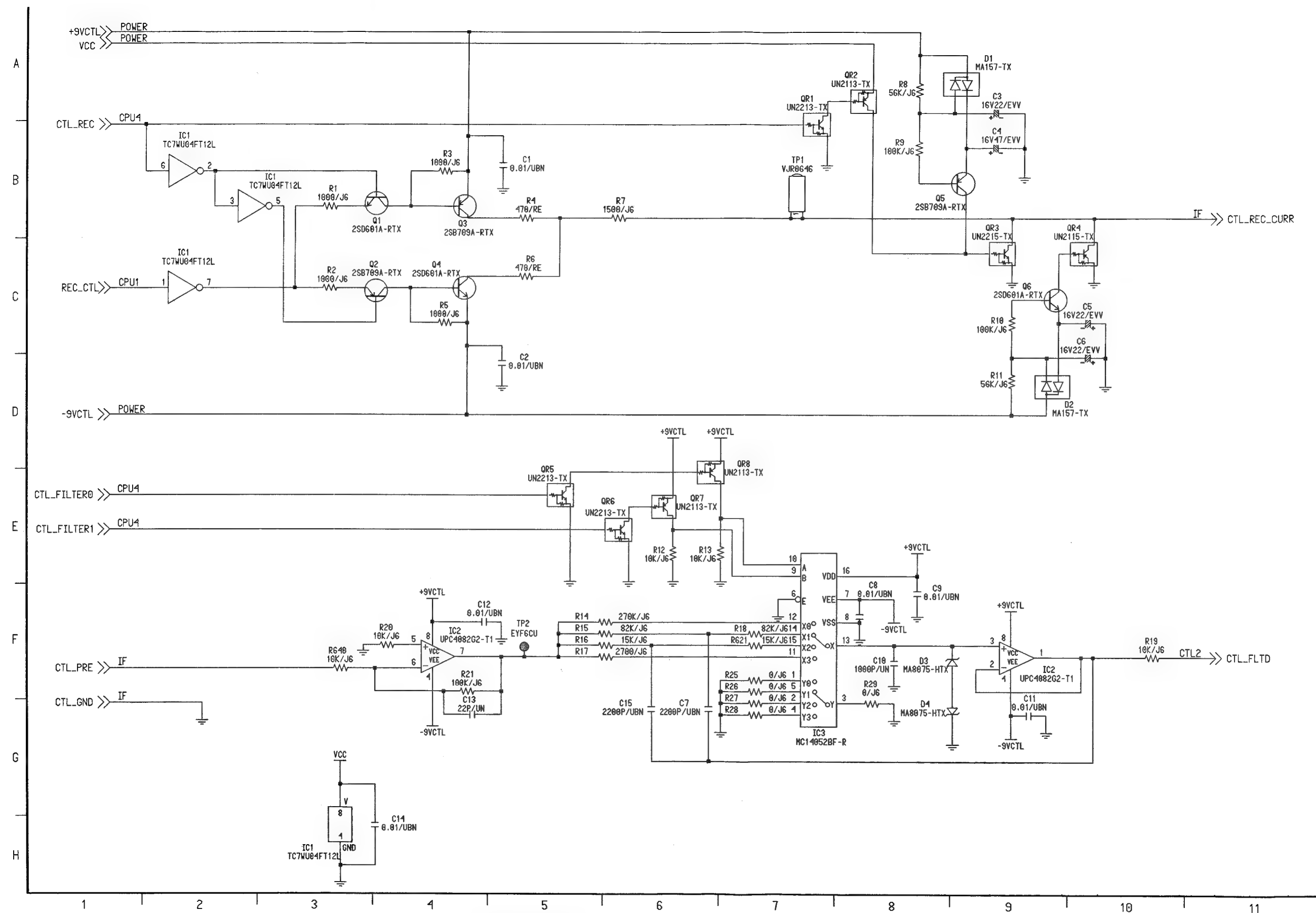
MOTHER (10/11) EQ (H3)/RF AMP (H4)/HEAD BUFF SCHEMATIC DIAGRAM



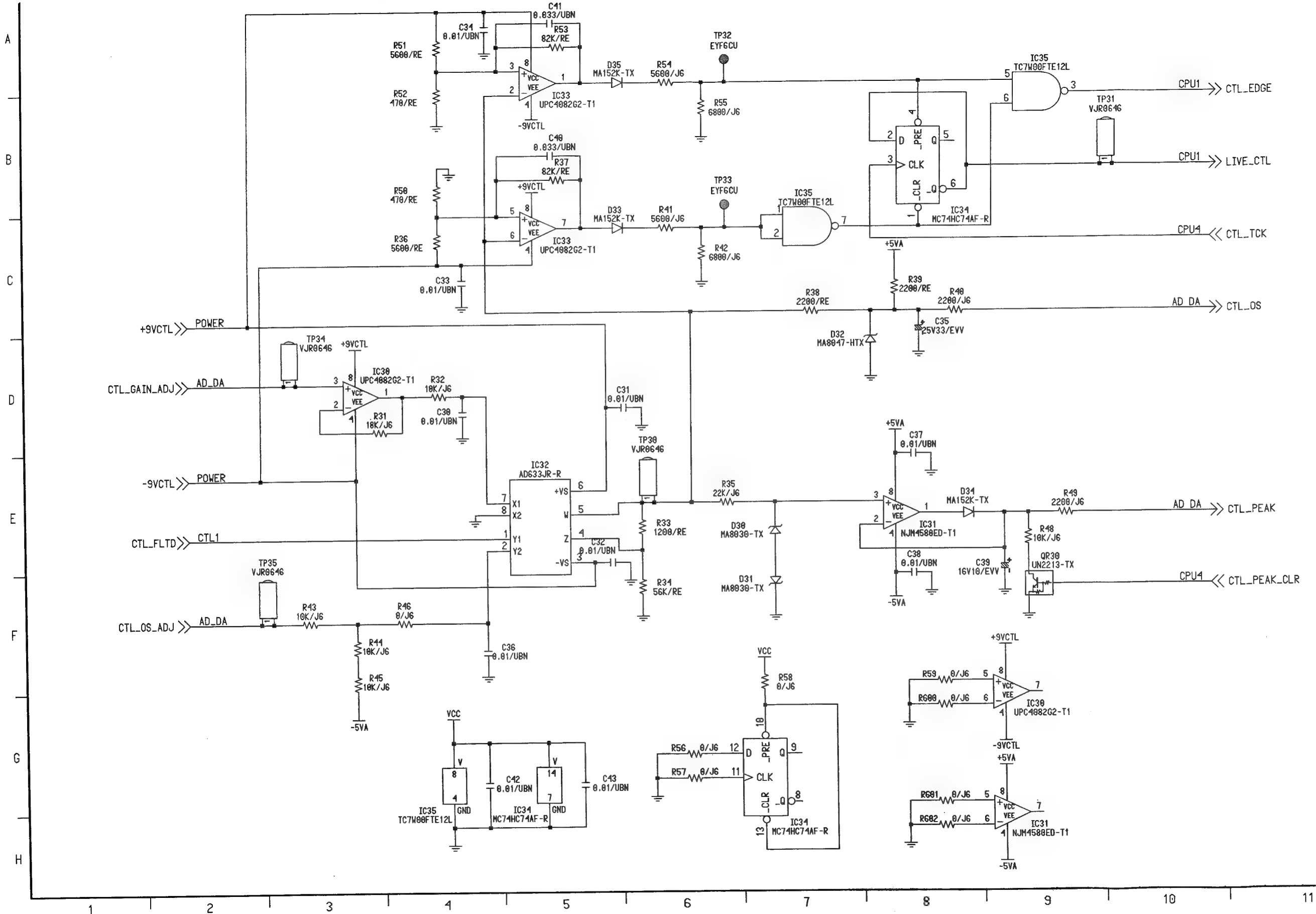
MOTHER (11/11) OTHERS SCHEMATIC DIAGRAM



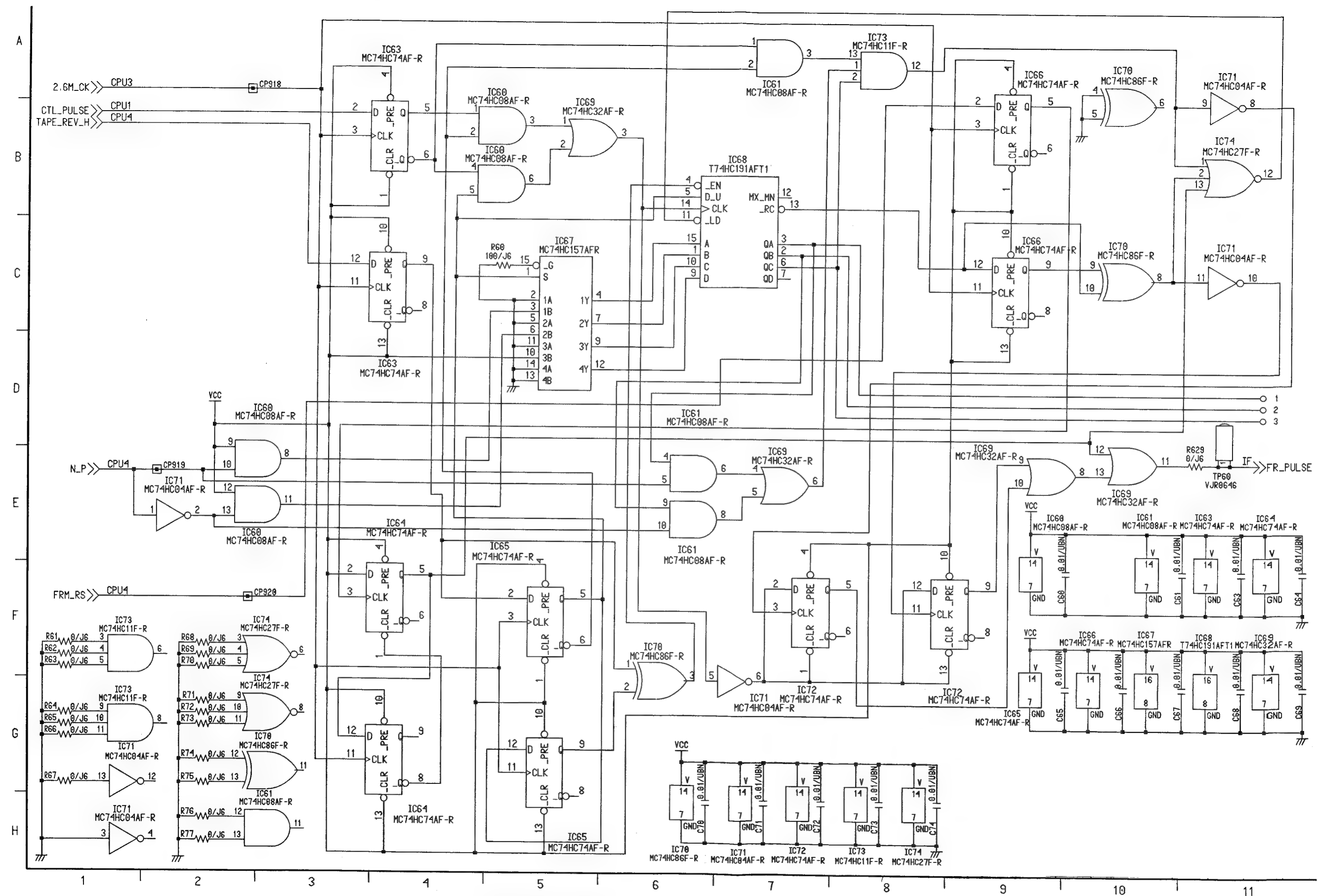
SERVO (F1 1/19) CTL1 SCHEMATIC DIAGRAM



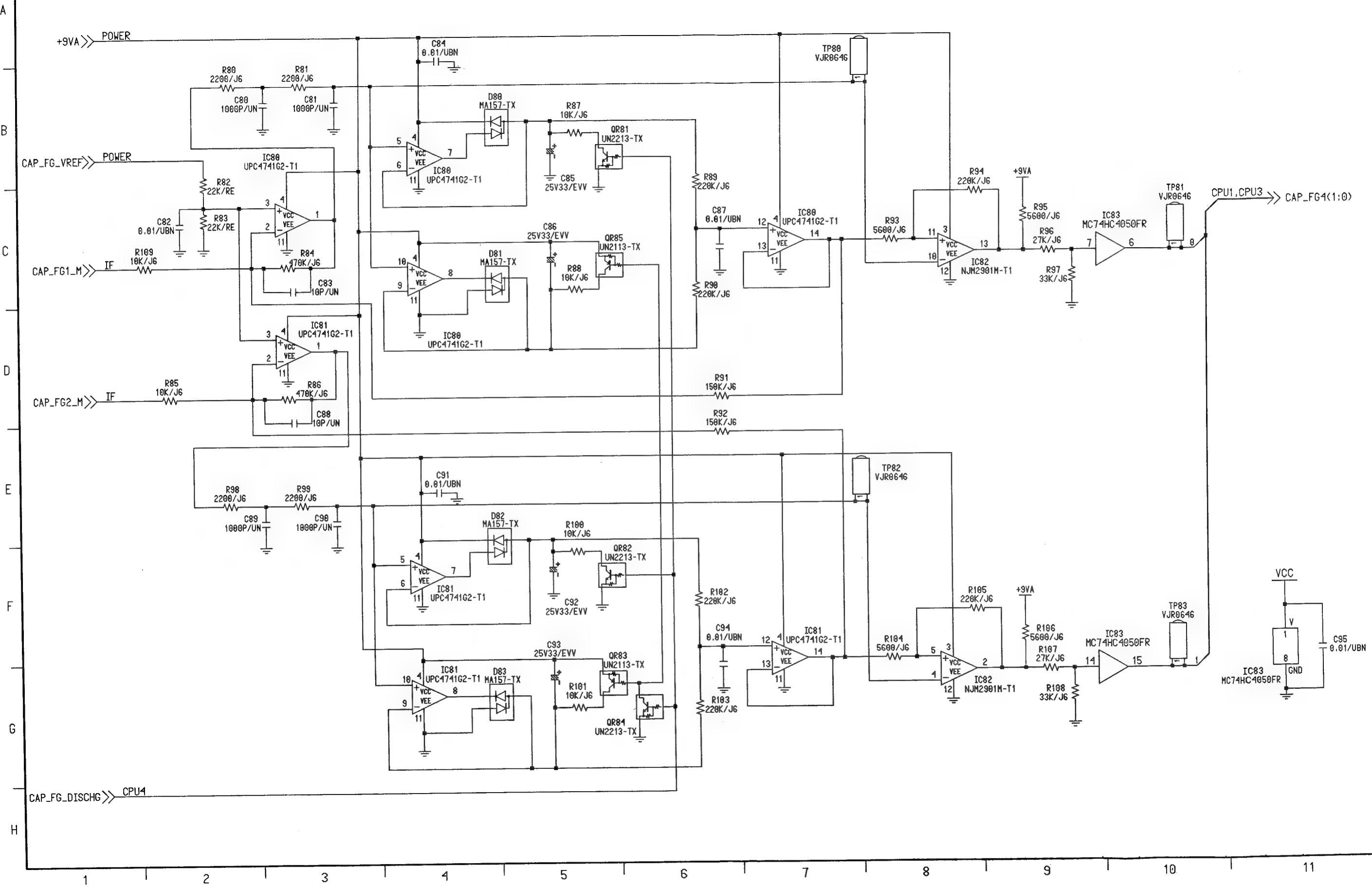
SERVO (F1 2/19) CTL2 SCHEMATIC DIAGRAM



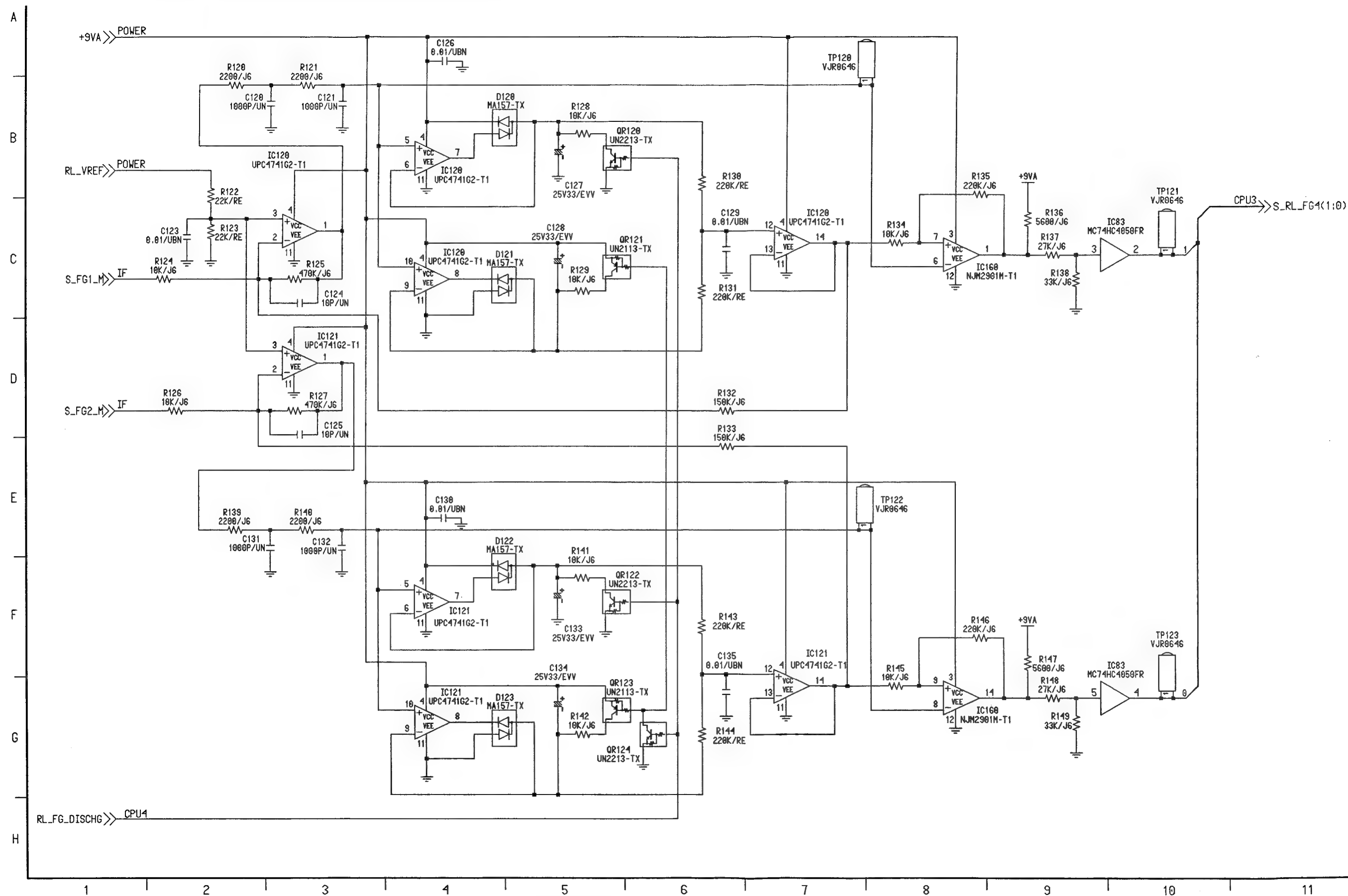
SERVO (F1 3/19) CTL3 SCHEMATIC DIAGRAM



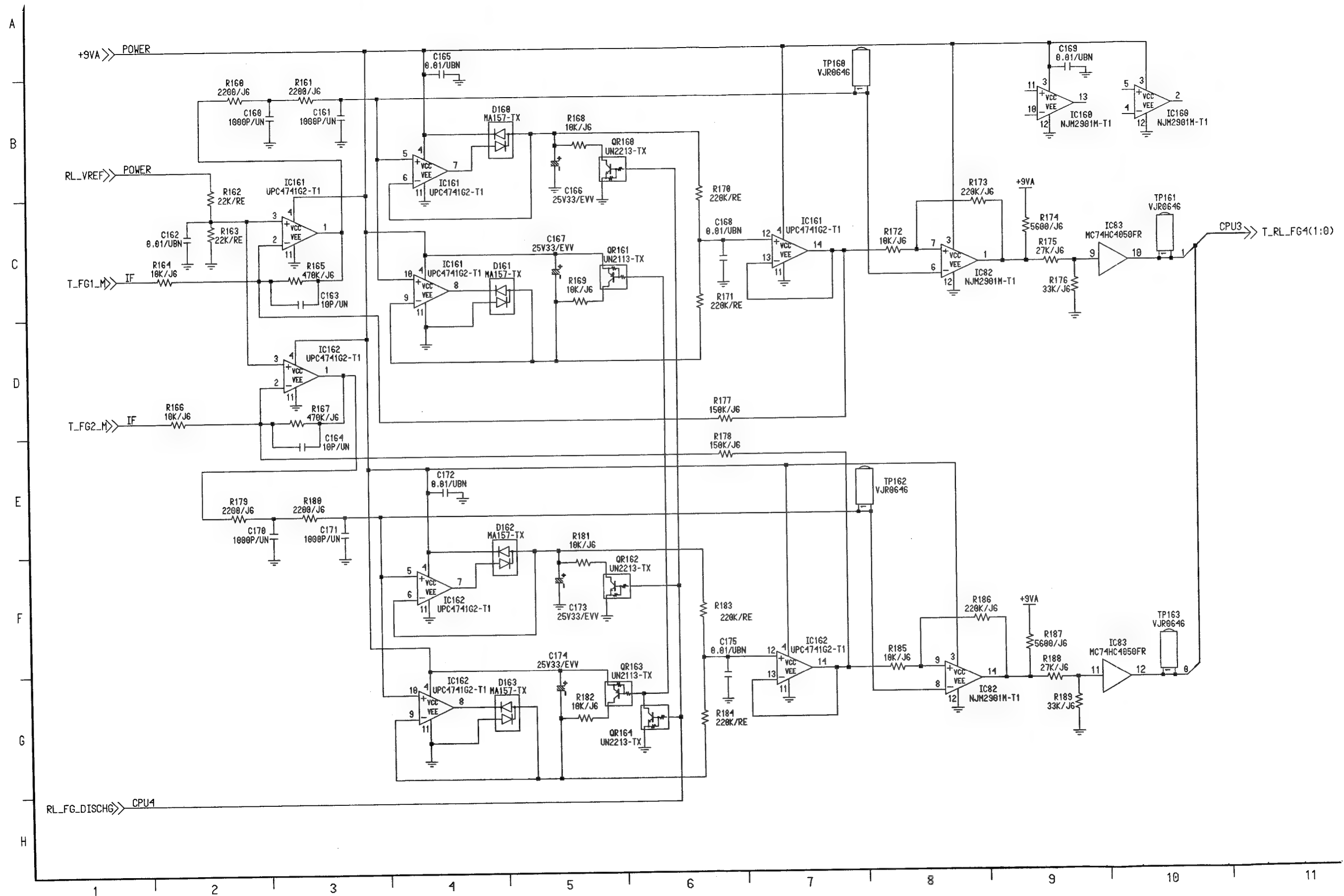
SERVO (F1 4/19) CAP FG SCHEMATIC DIAGRAM



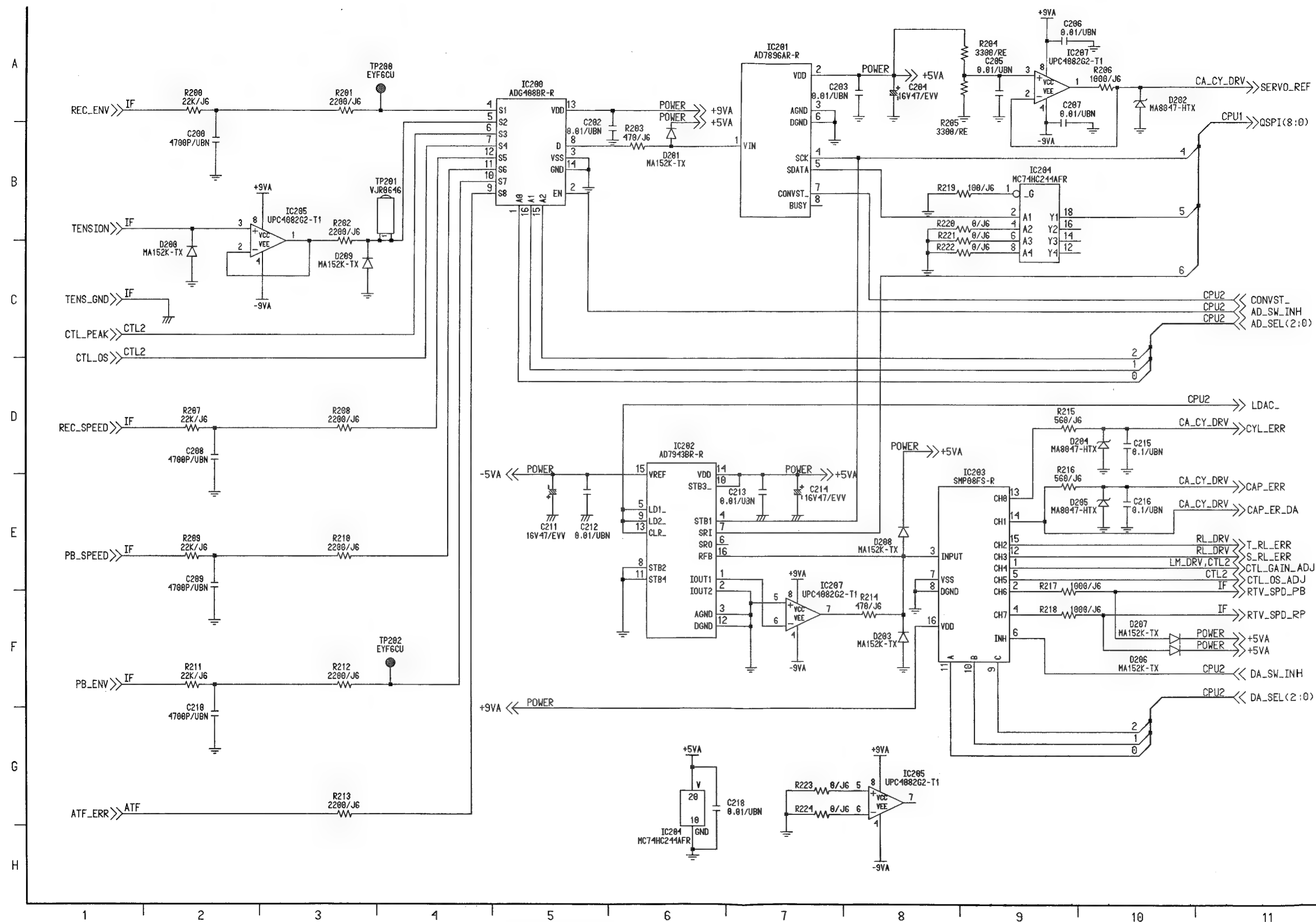
SERVO (F1 5/19) S FG SCHEMATIC DIAGRAM



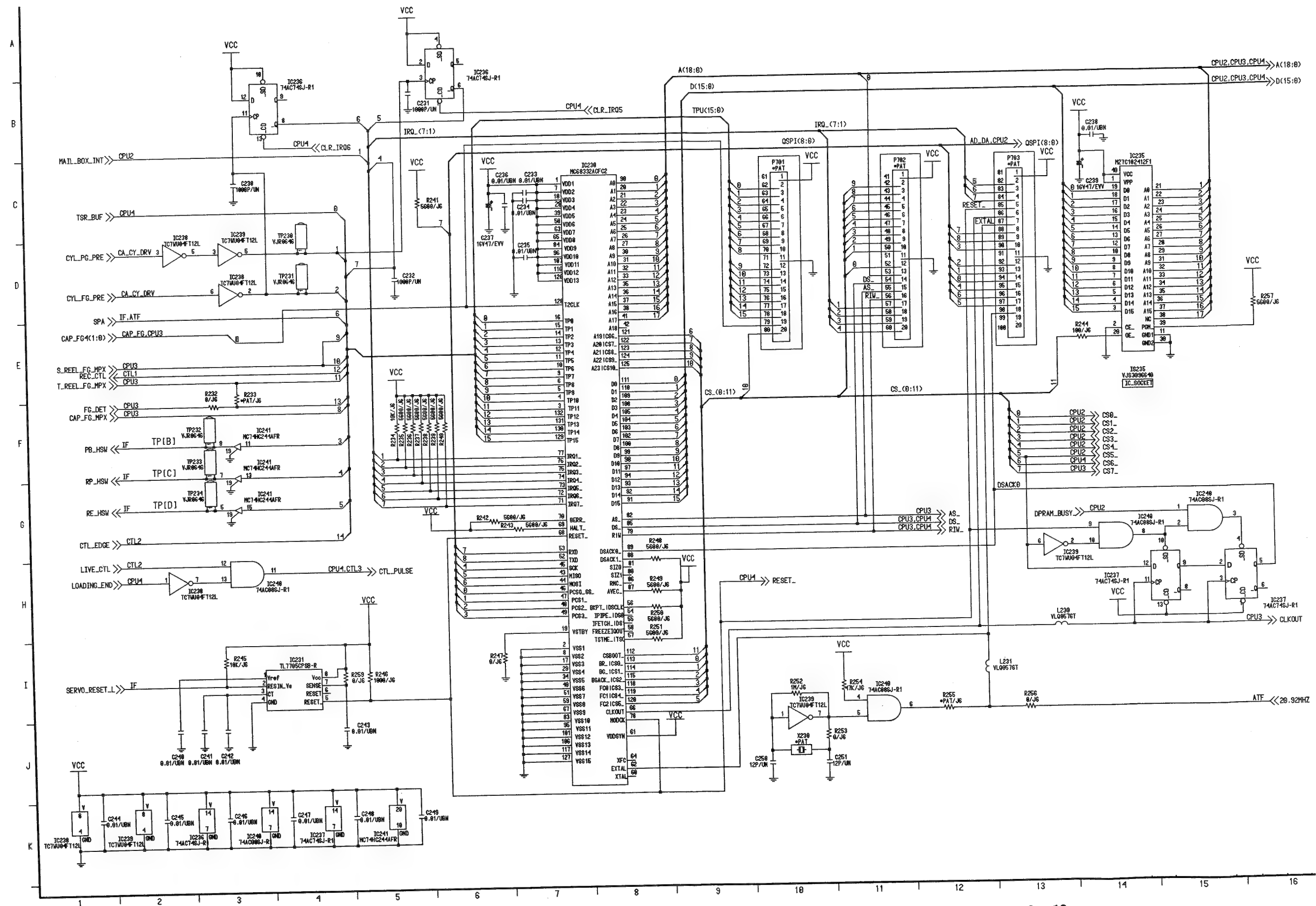
SERVO (F1 6/19) T FG SCHEMATIC DIAGRAM



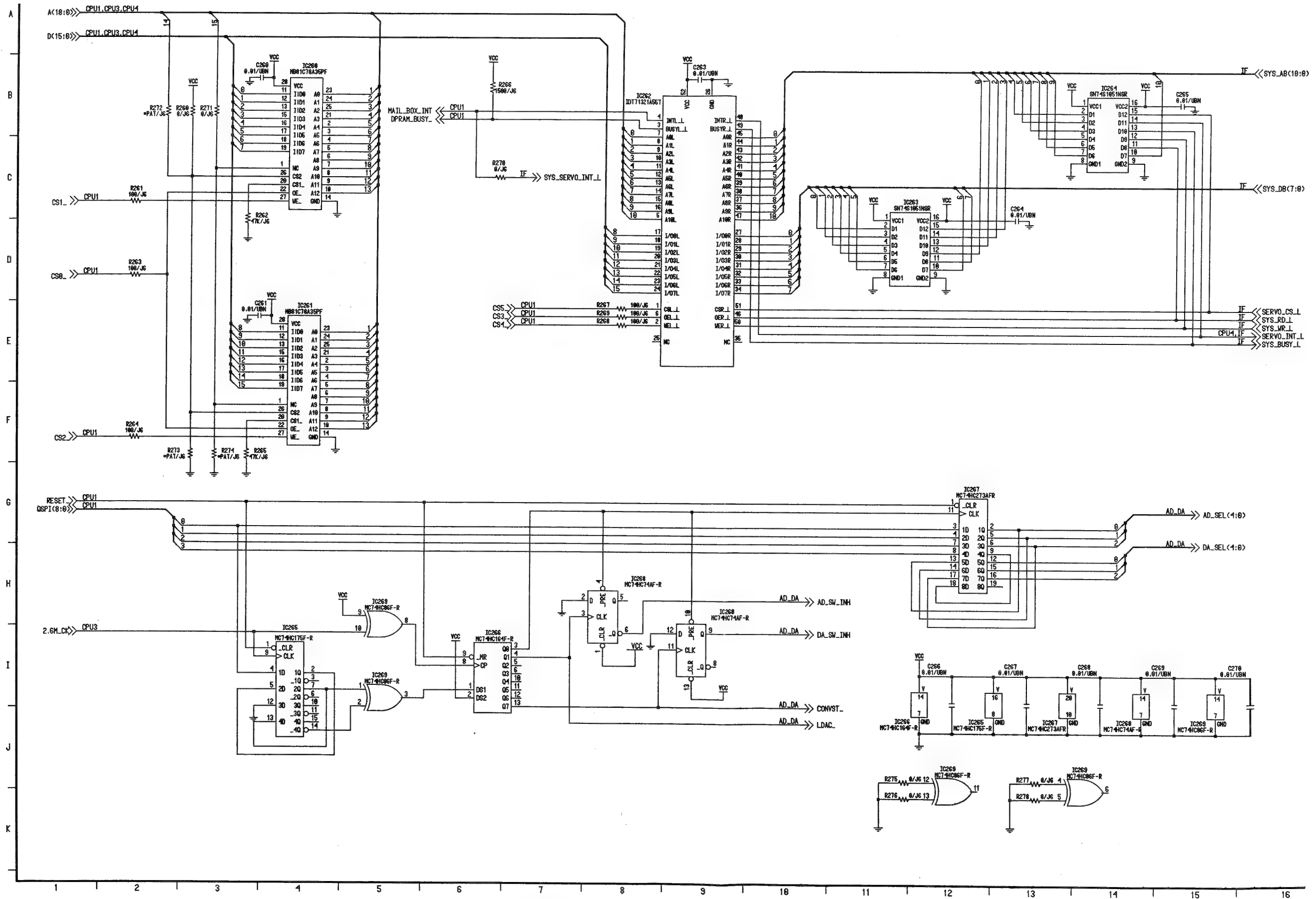
SERVO (F1 7/19) AD DA SCHEMATIC DIAGRAM



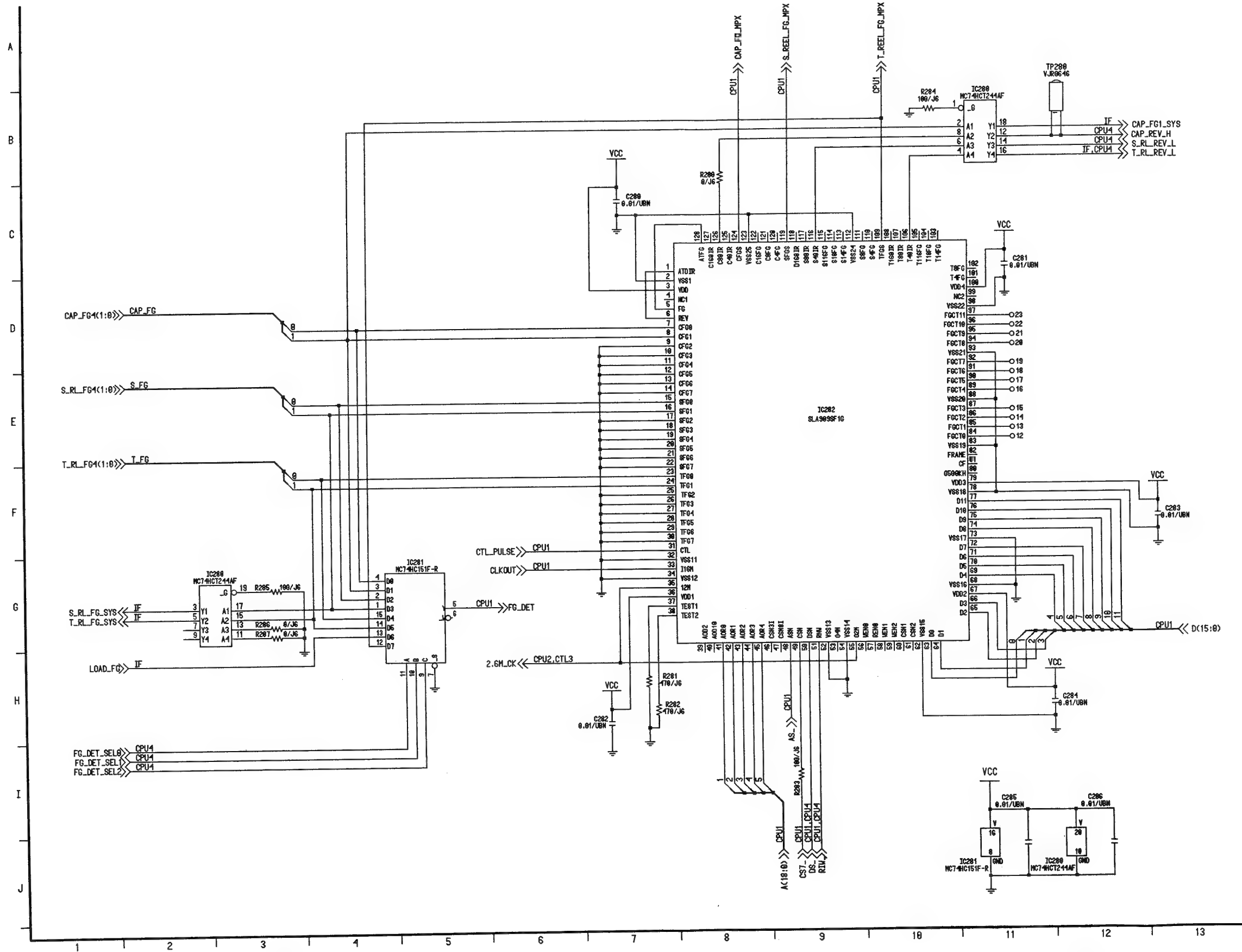
SERVO (F1 8/19) CPU1 SCHEMATIC DIAGRAM



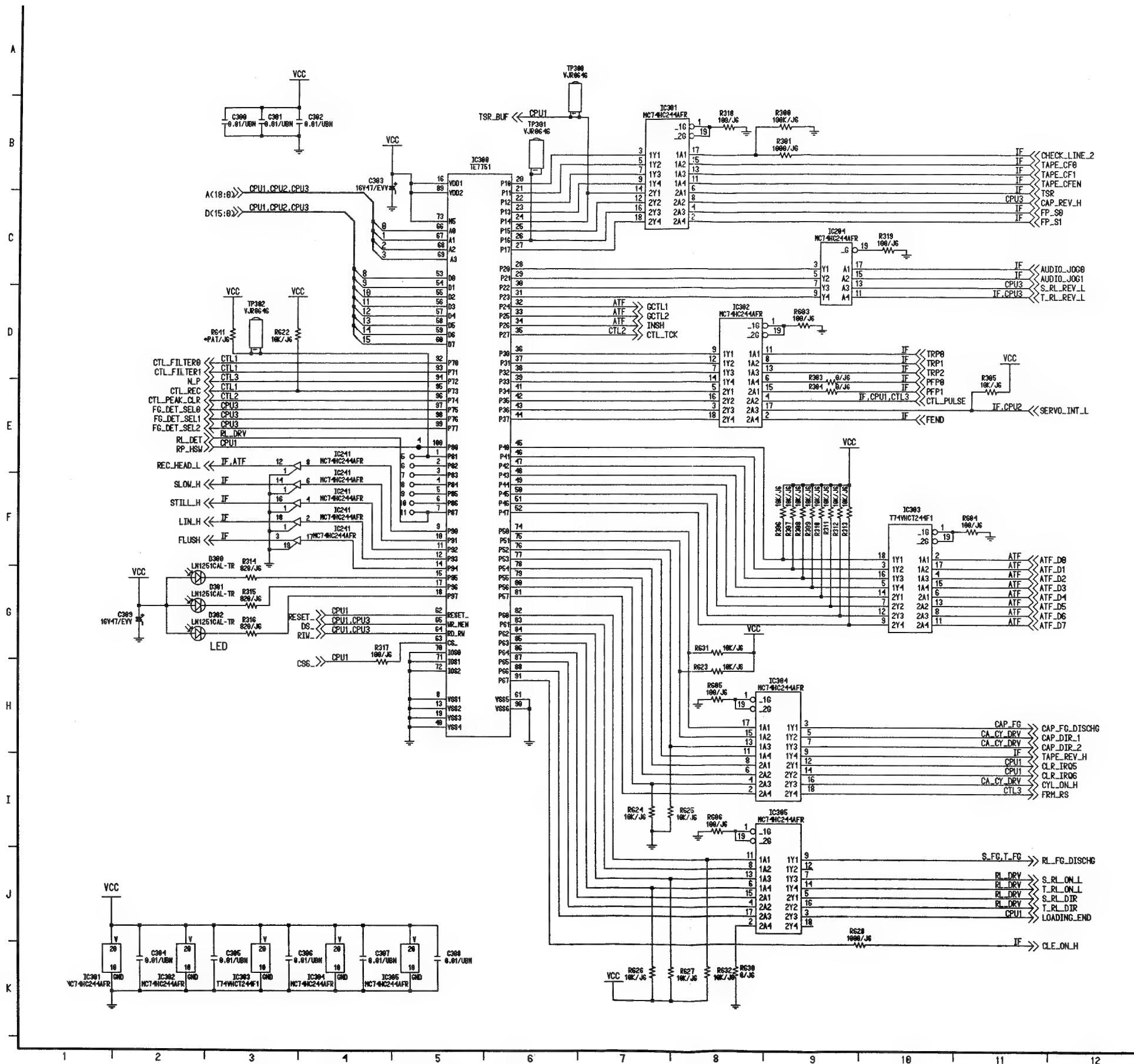
SERVO (F1 9/19) CPU2 SCHEMATIC DIAGRAM



SERVO (F1 10/19) CPU3 SCHEMATIC DIAGRAM



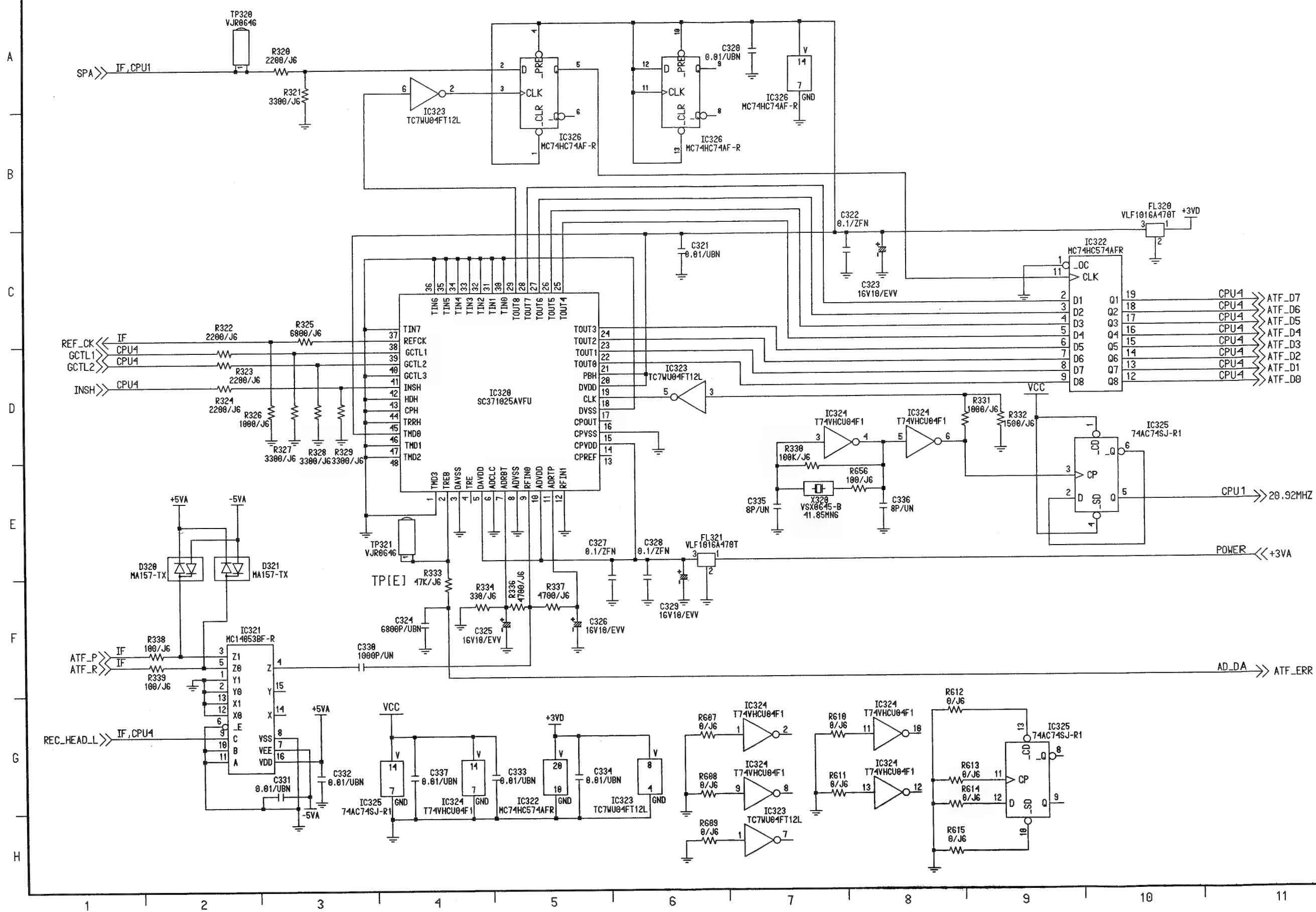
SERVO (F1 11/19) CPU4 SCHEMATIC DIAGRAM



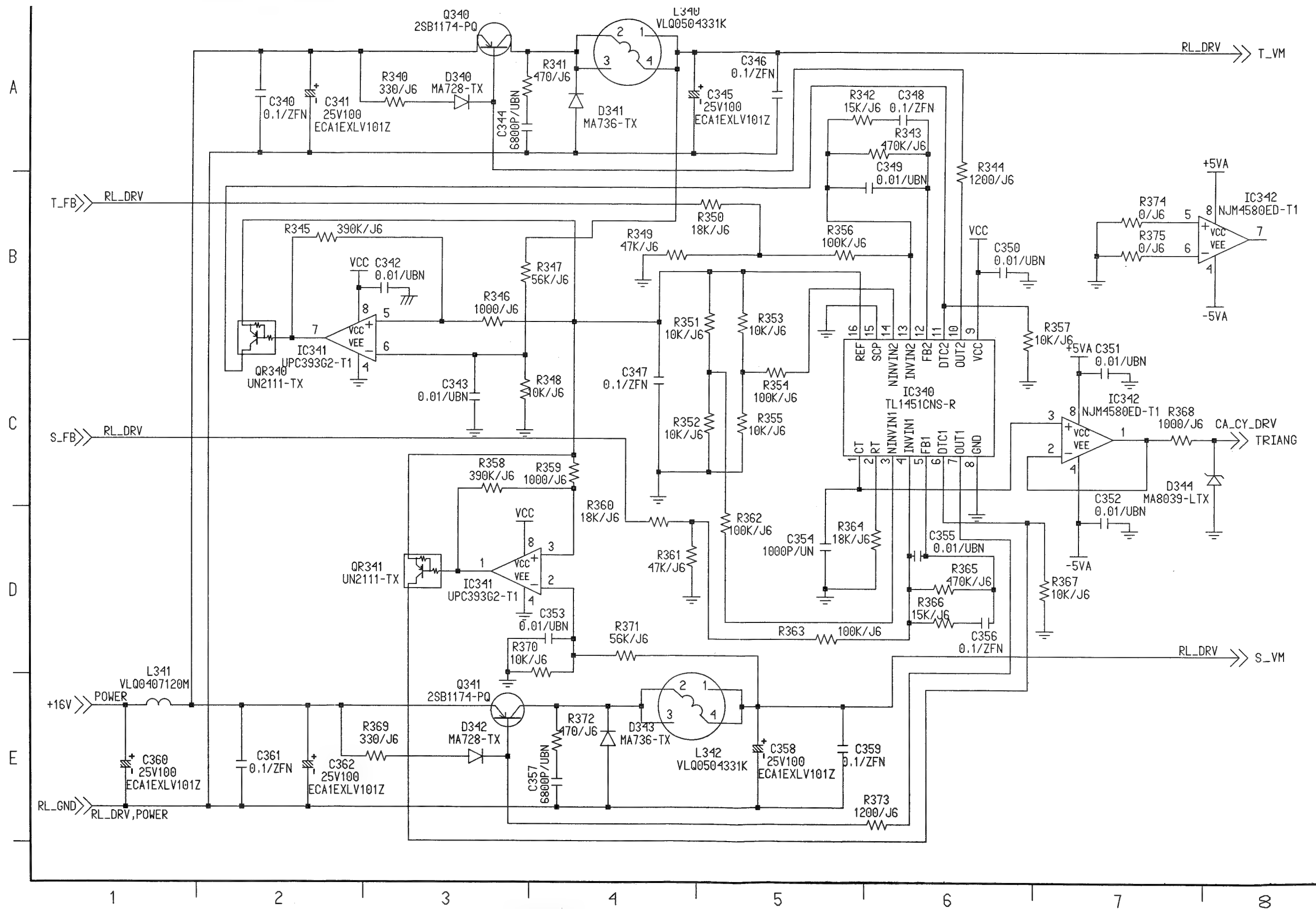
REVERSE SIDE

F1 SERVO 10/19

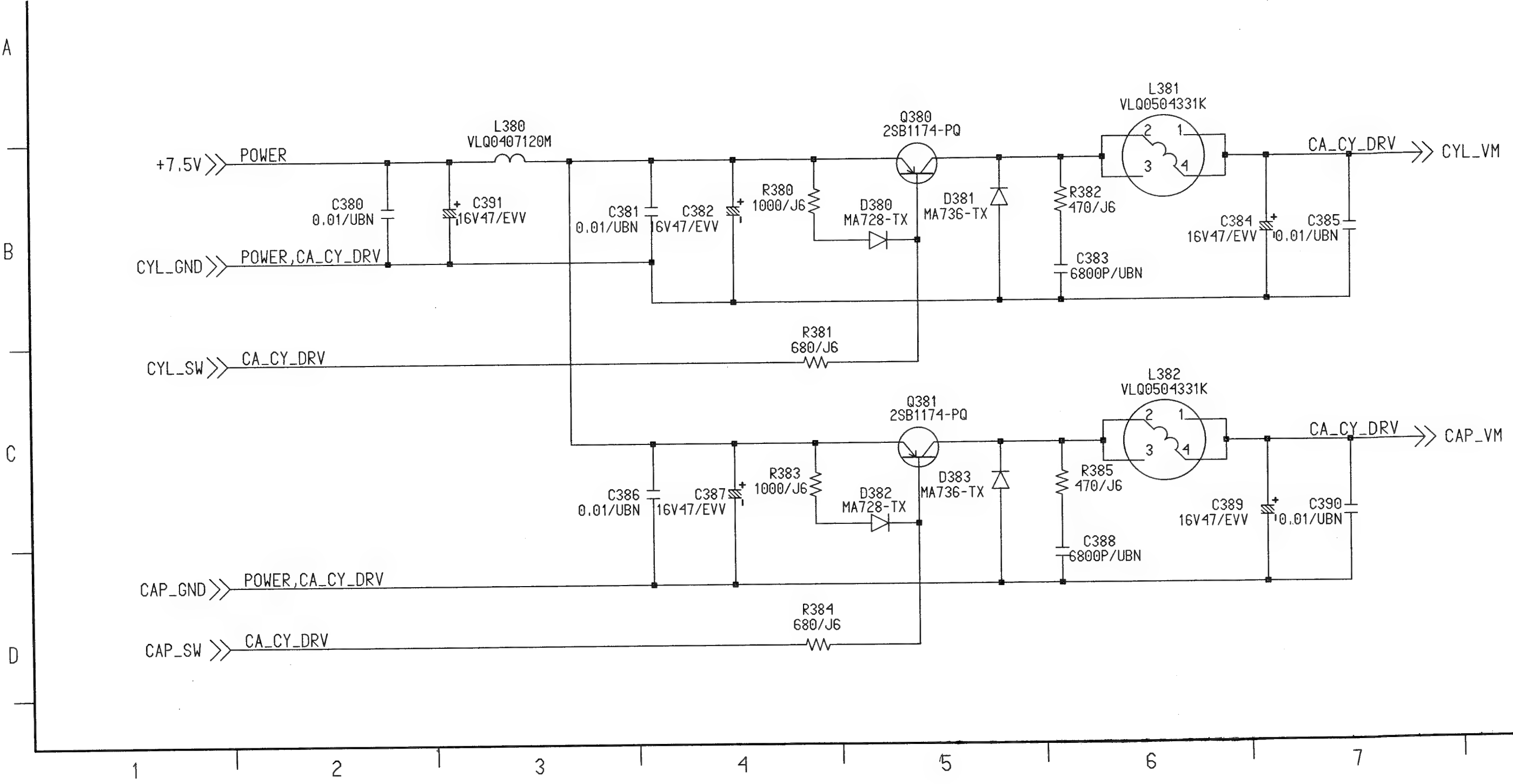
SERVO (F1 12/19) ATF SCHEMATIC DIAGRAM



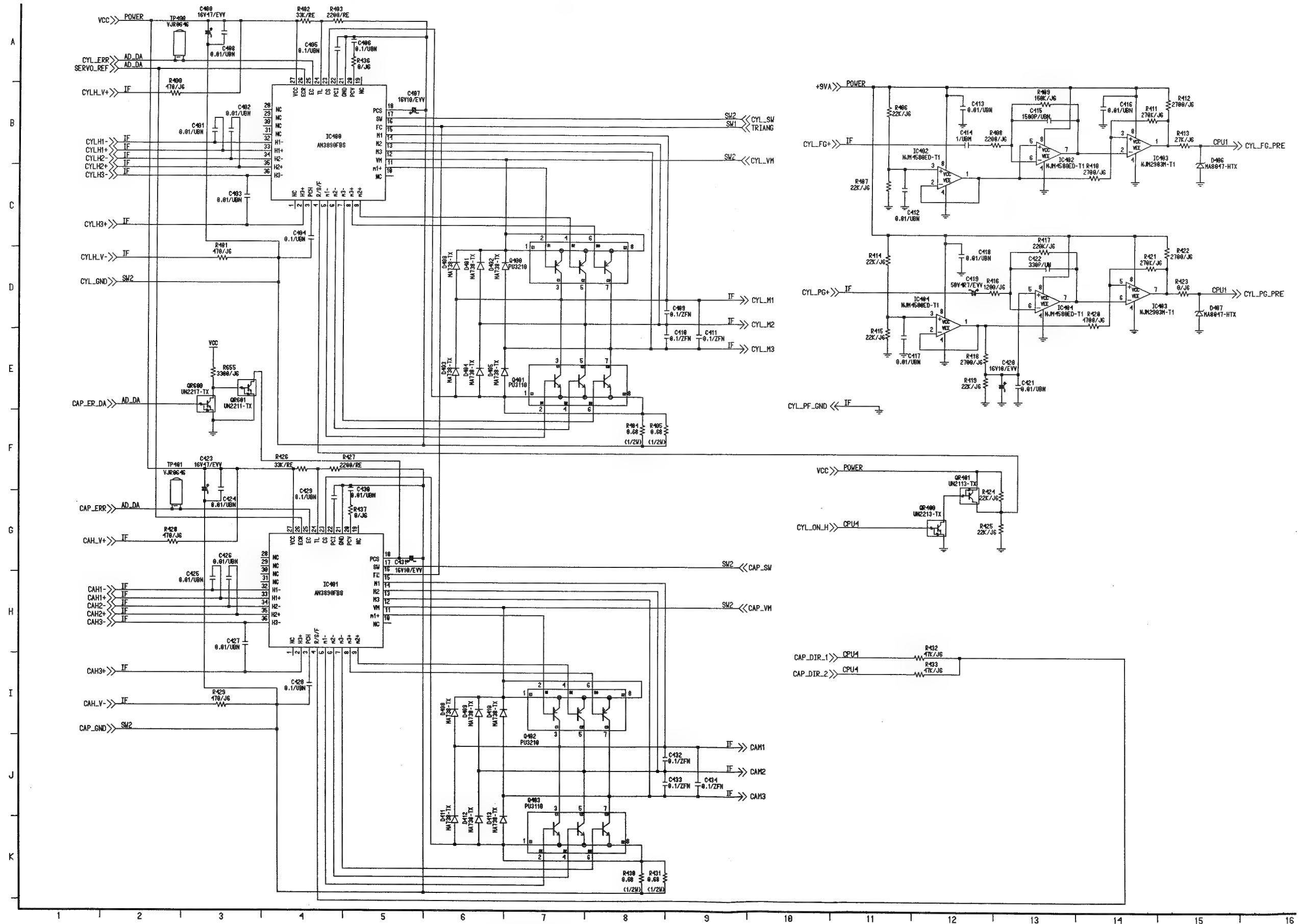
SERVO (F1 13/19) SW1 SCHEMATIC DIAGRAM



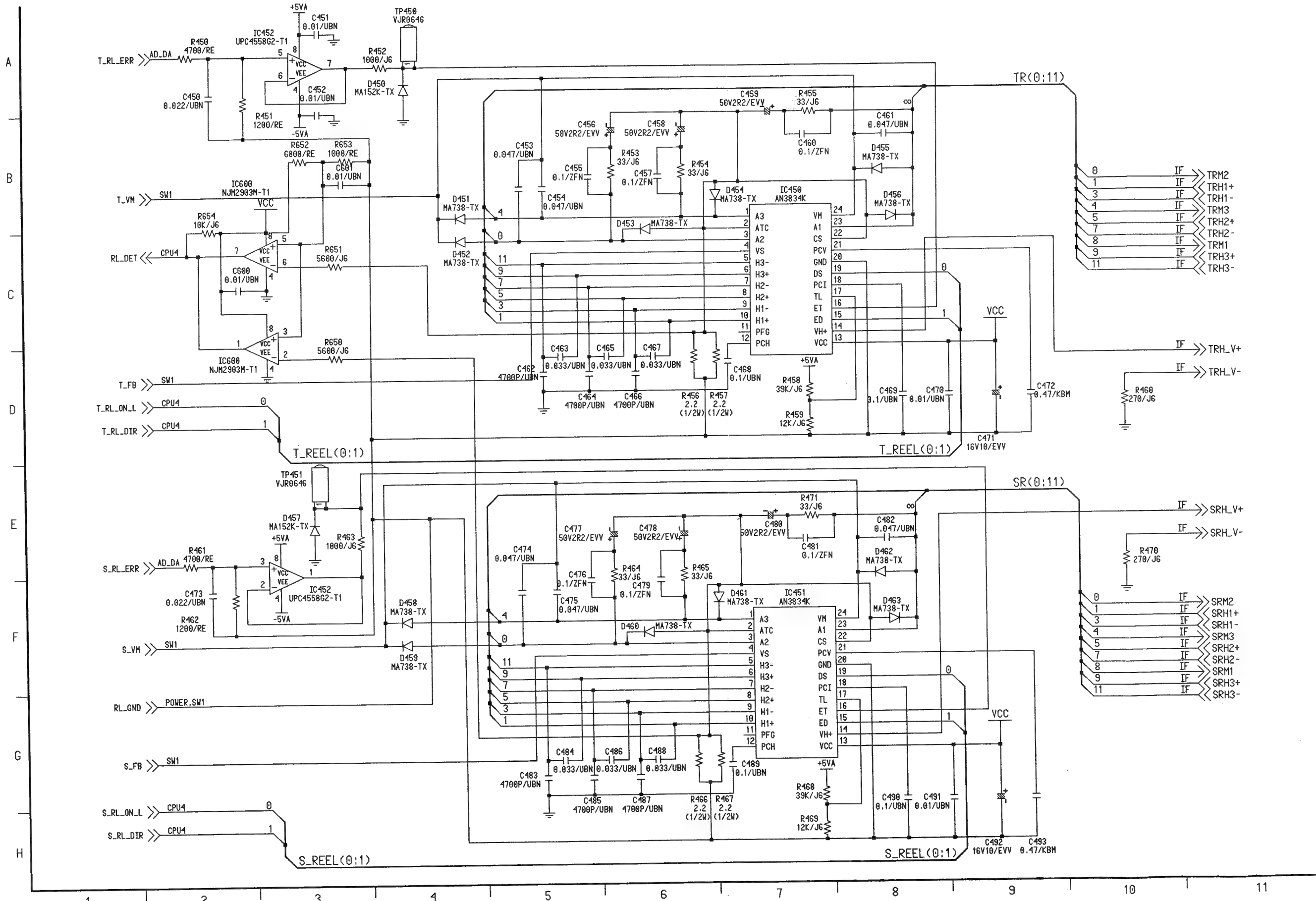
SERVO (F1 14/19) SW2 SCHEMATIC DIAGRAM



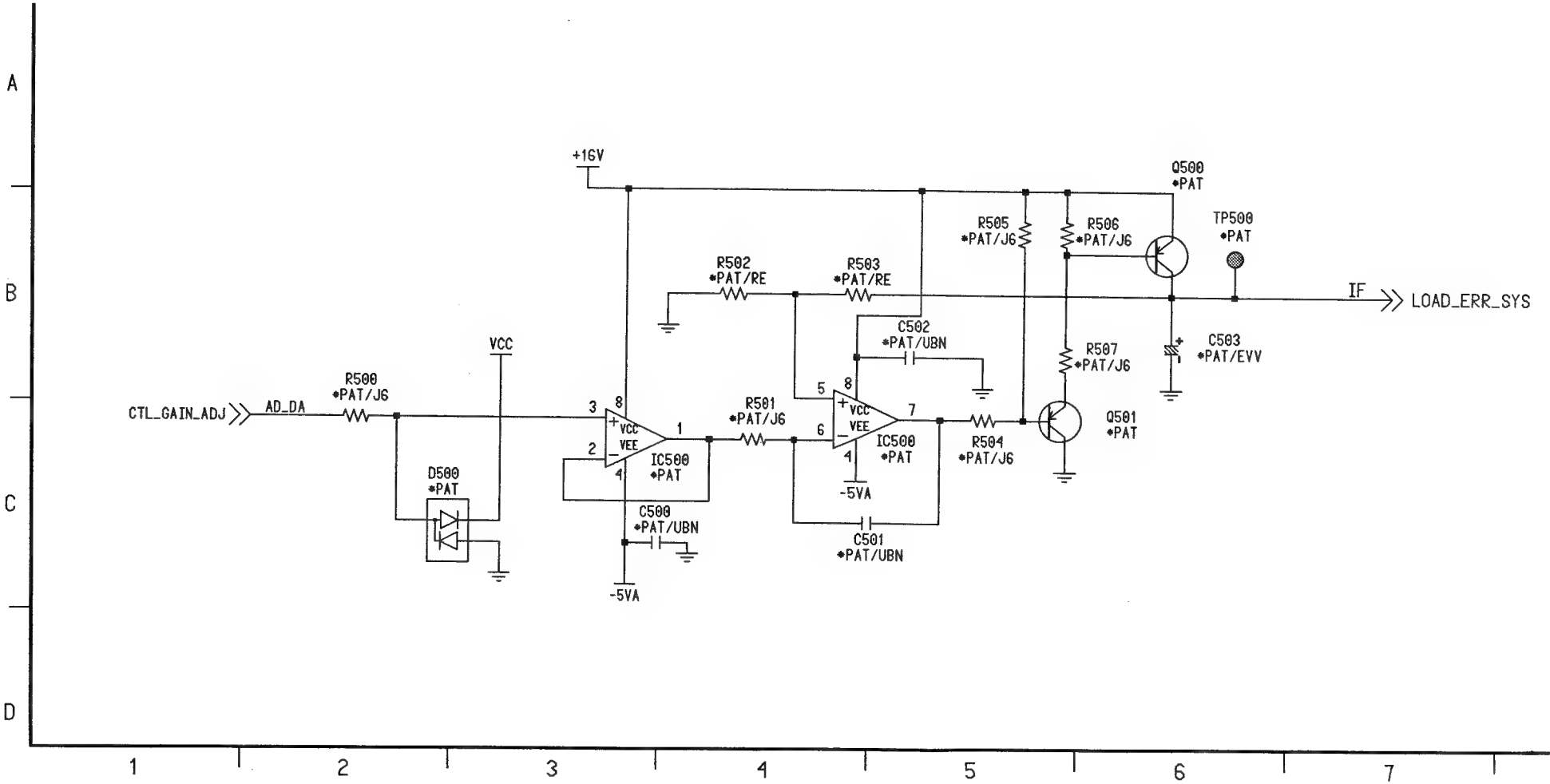
SERVO (F1 15/19) CA CY DRV SCHEMATIC DIAGRAM



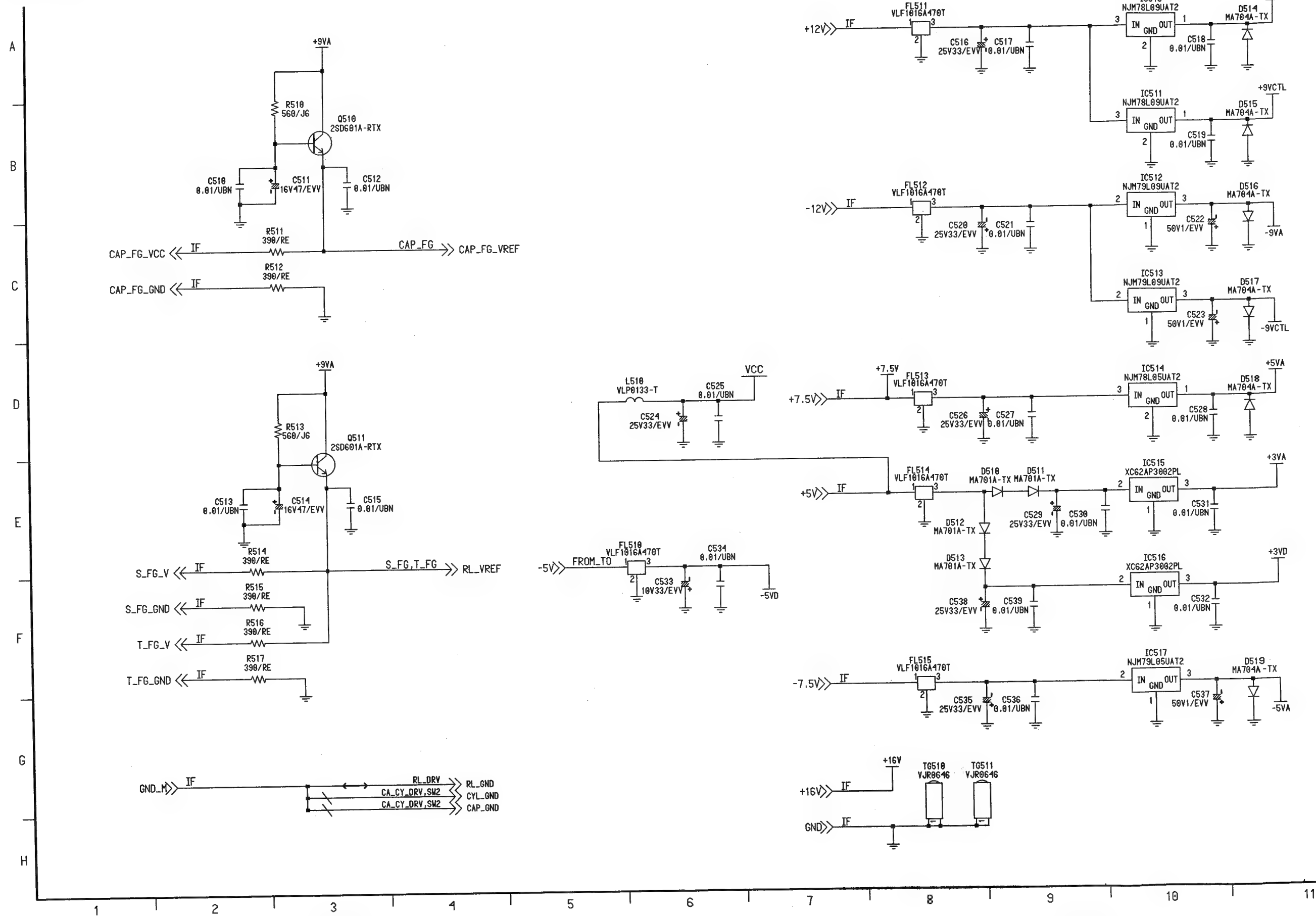
SERVO (F1 16/19) RL DRV SCHEMATIC DIAGRAM



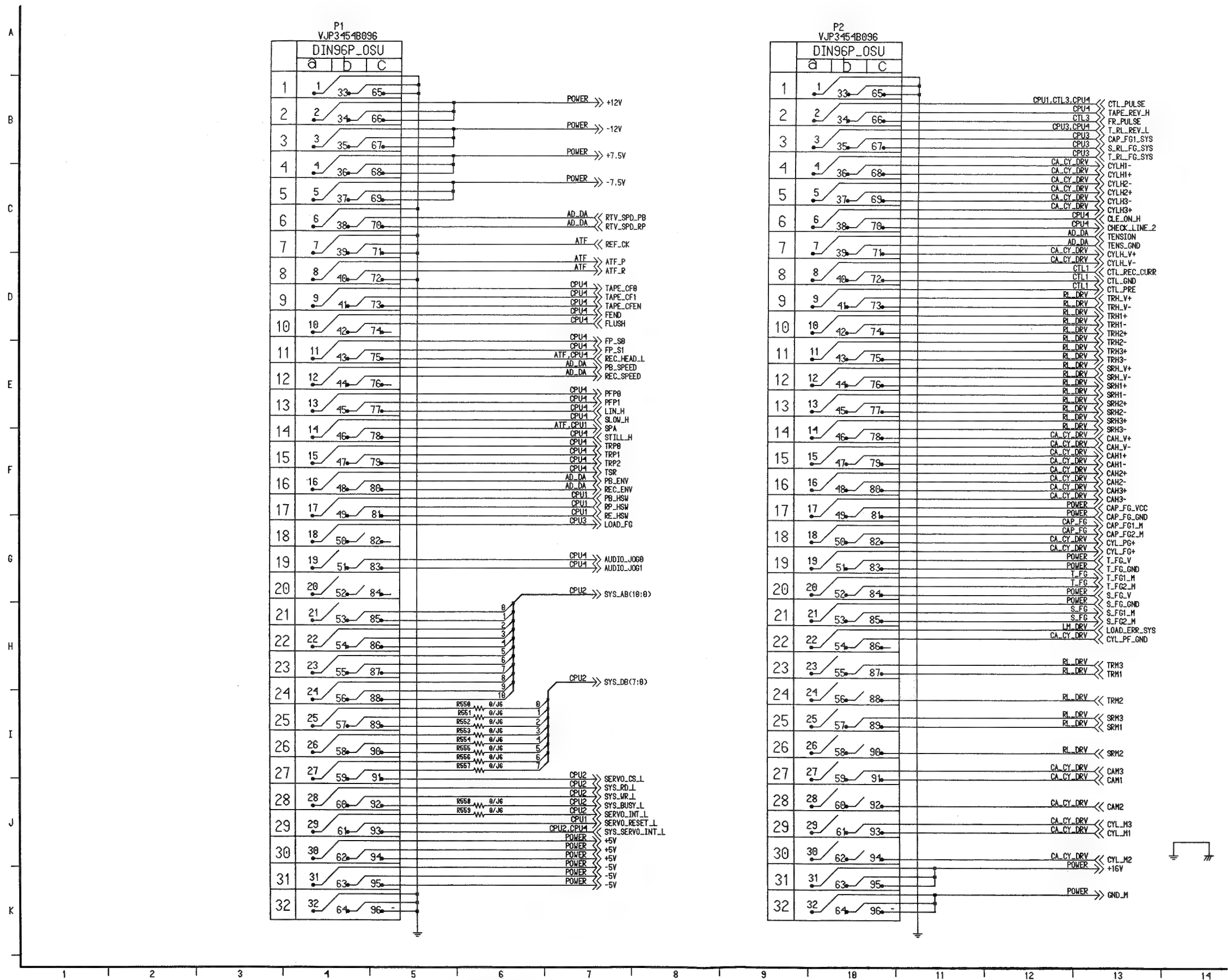
SERVO (F1 17/19) LM DRV SCHEMATIC DIAGRAM



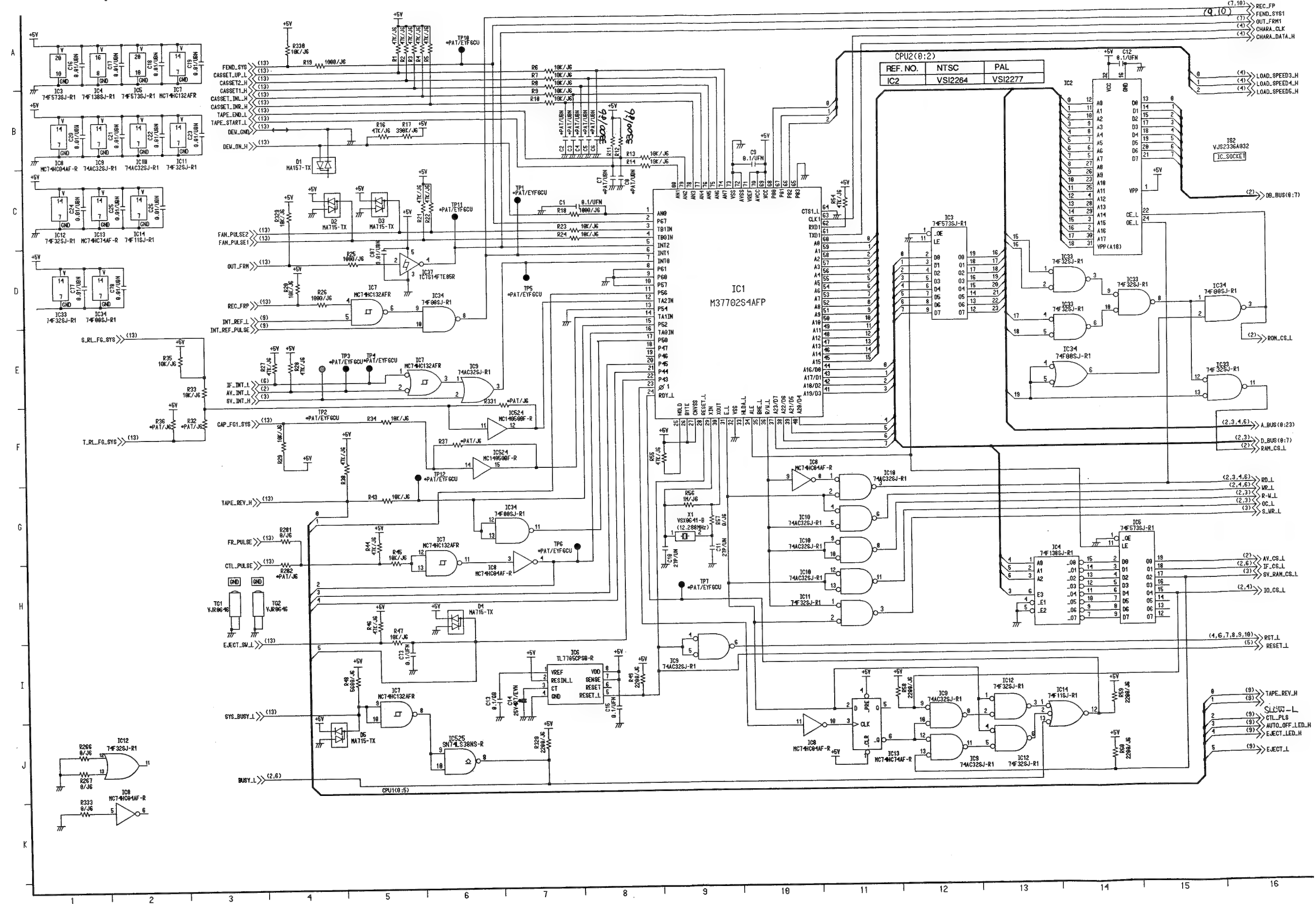
SERVO (F1 18/19) POWER SCHEMATIC DIAGRAM



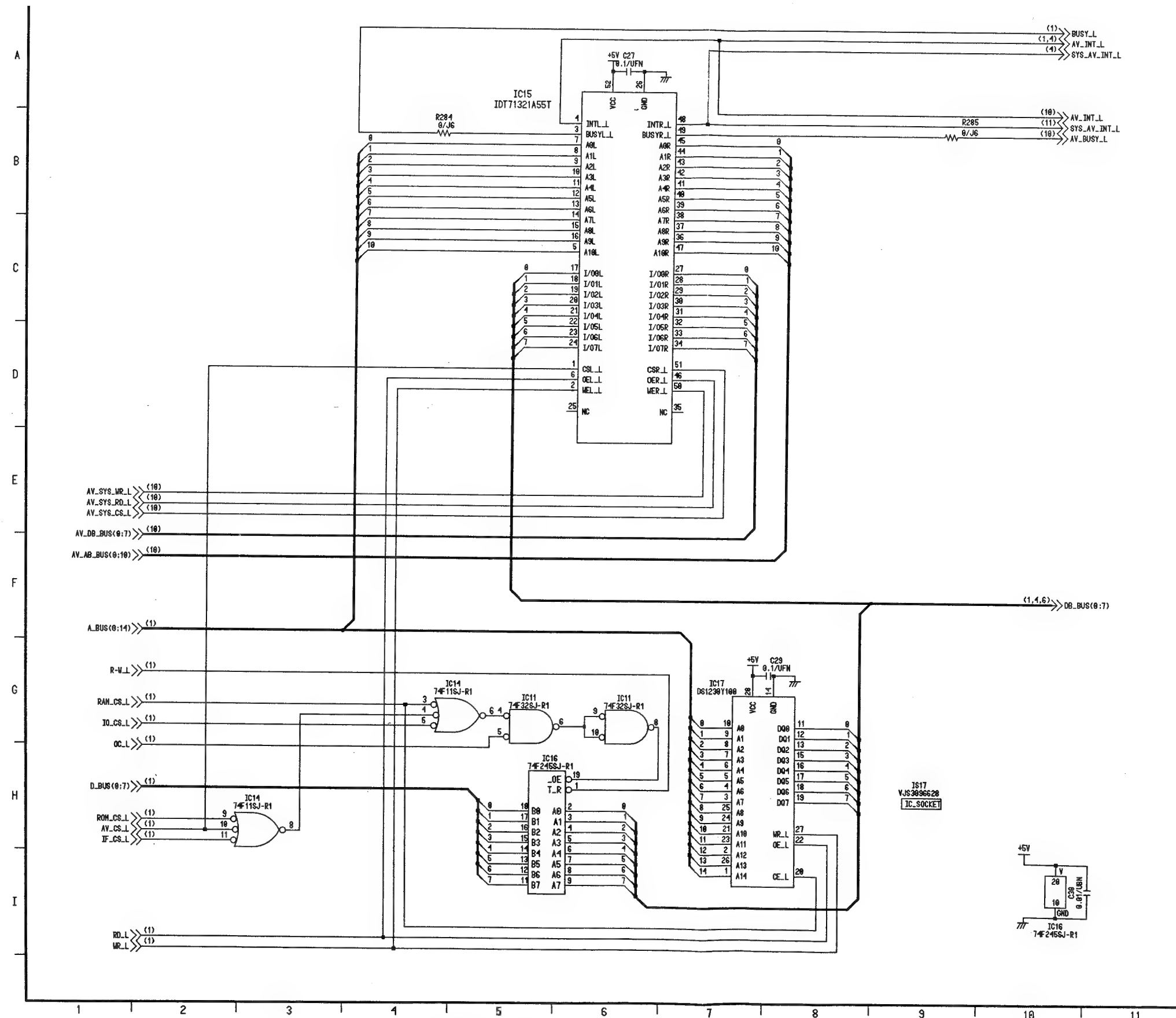
SERVO (F1 19/19) CONNECTOR SCHEMATIC DIAGRAM



SYSCON (F2 1/14) MAIN 1 SCHEMATIC DIAGRAM

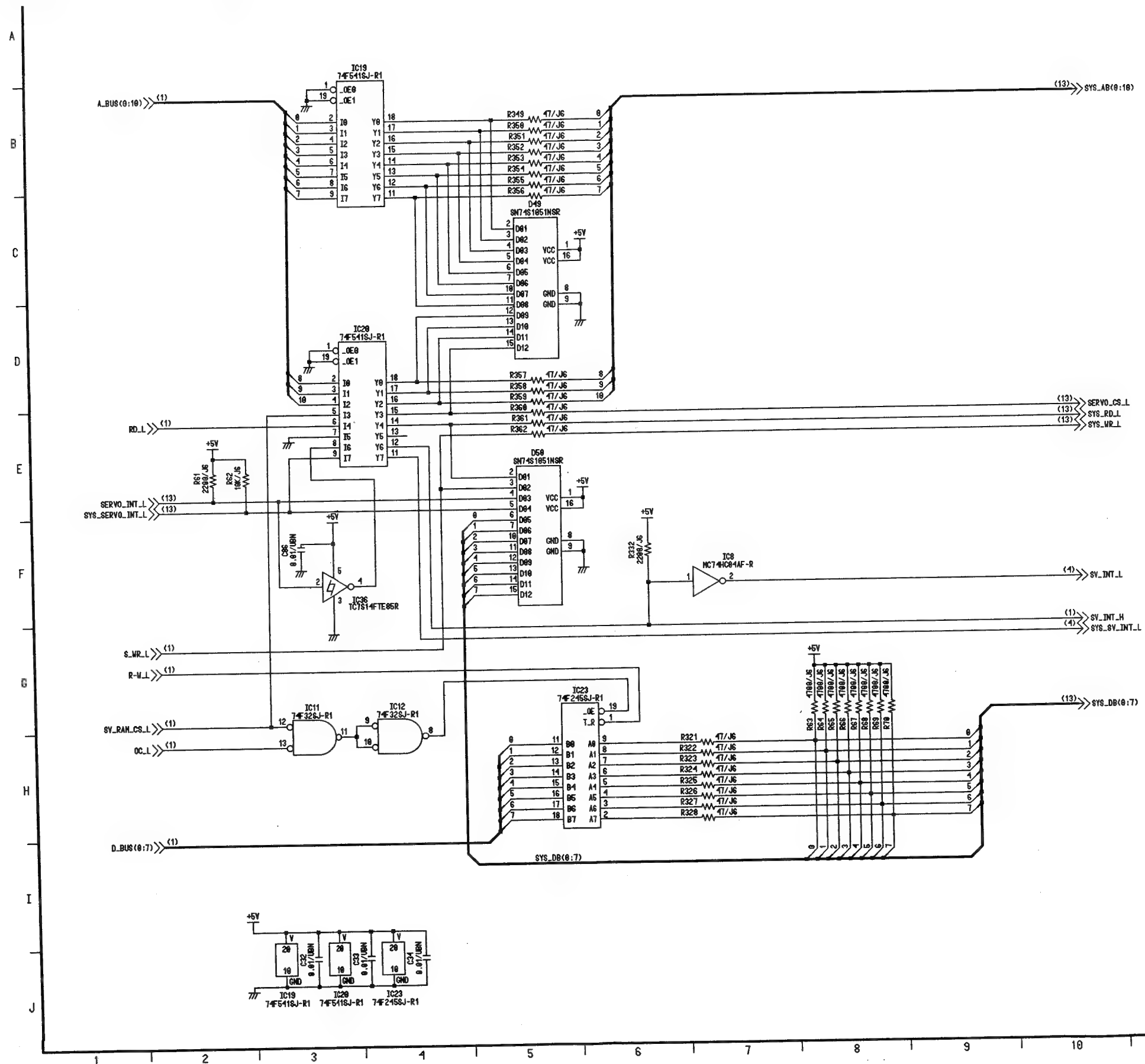


SYSCON (F2 2/14) MAIN 2 SCHEMATIC DIAGRAM

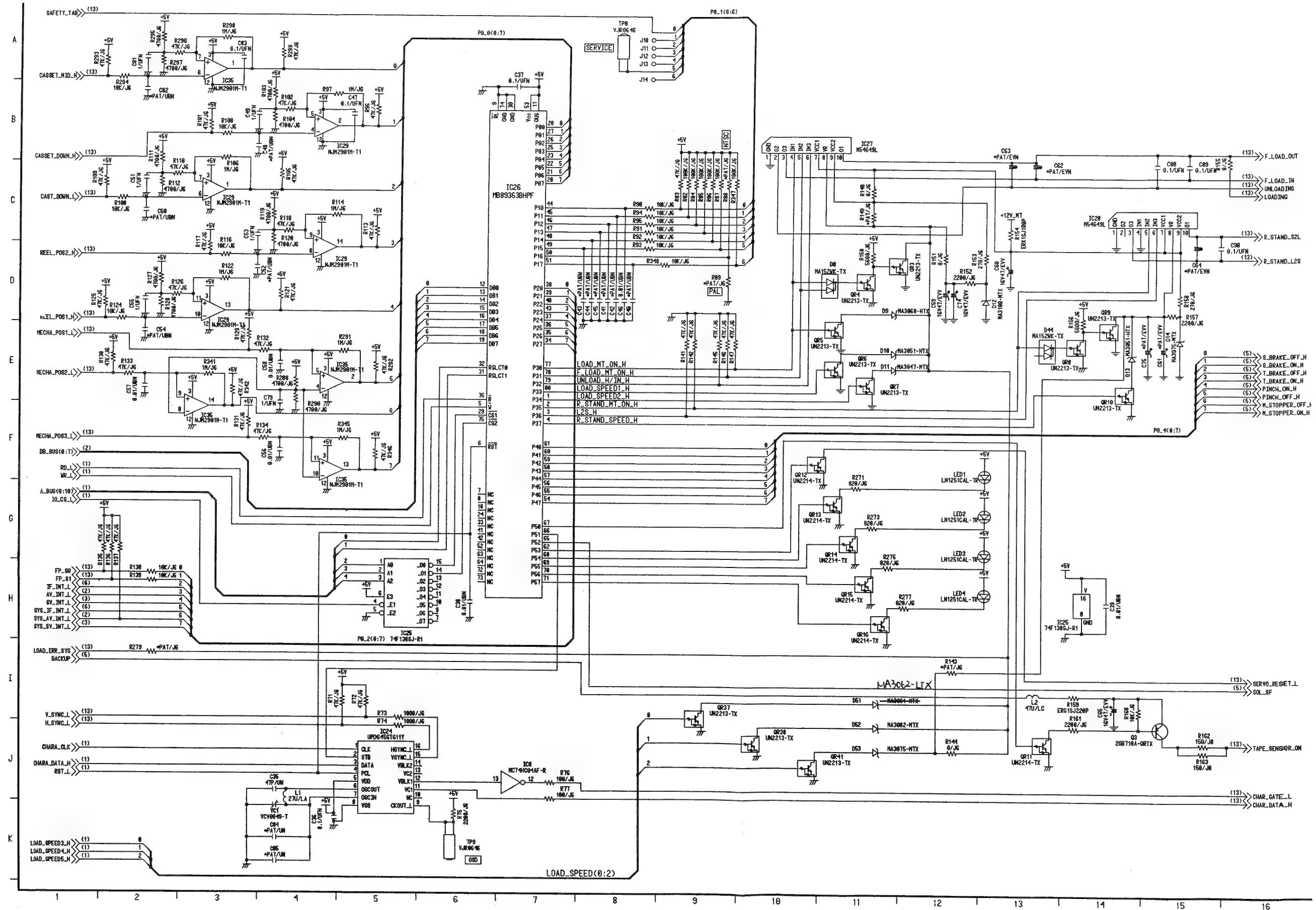


REVERSE SIDE
F2 SYSCON 1/14

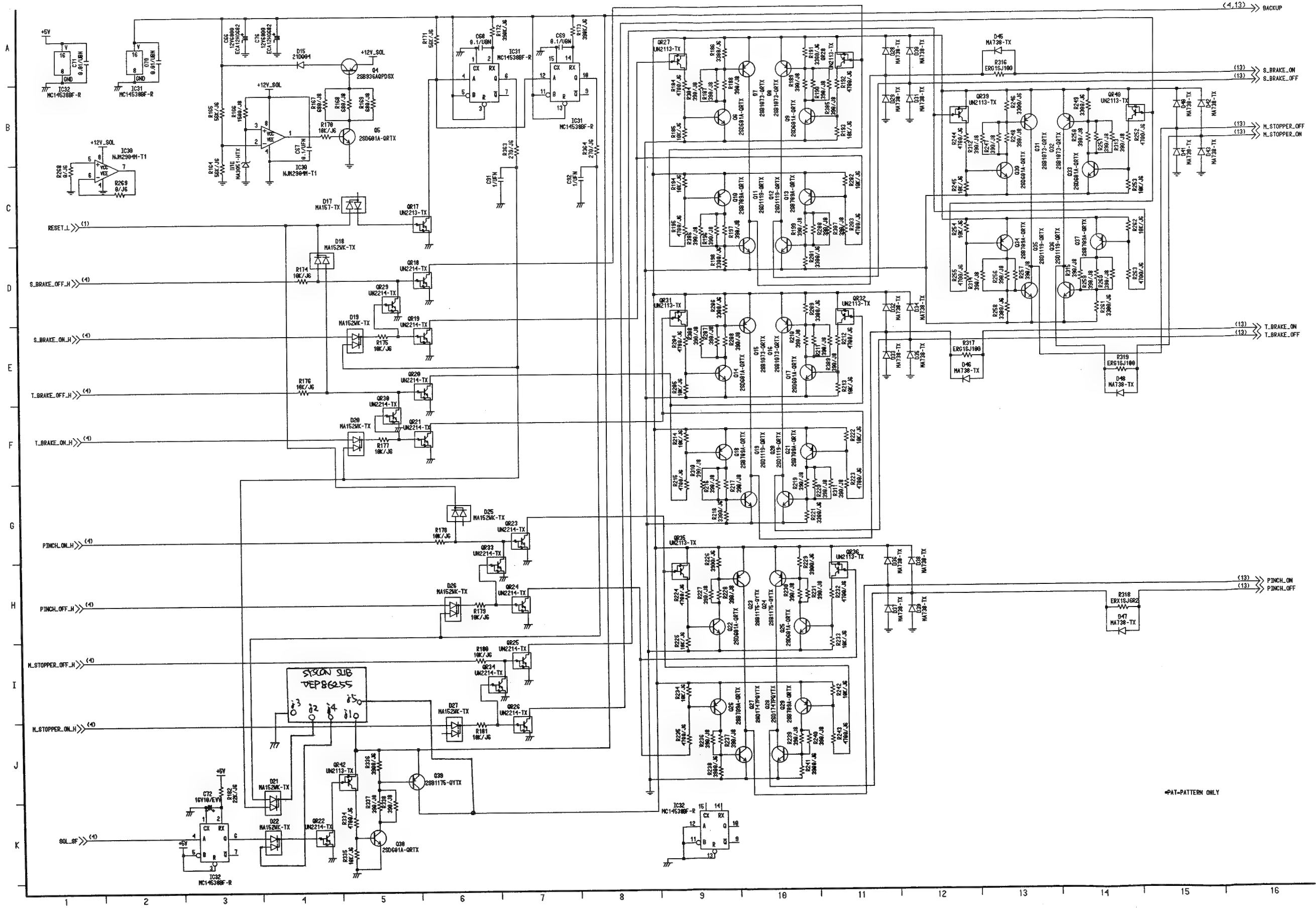
SYSCON (F2 3/14) MAIN 3 SCHEMATIC DIAGRAM



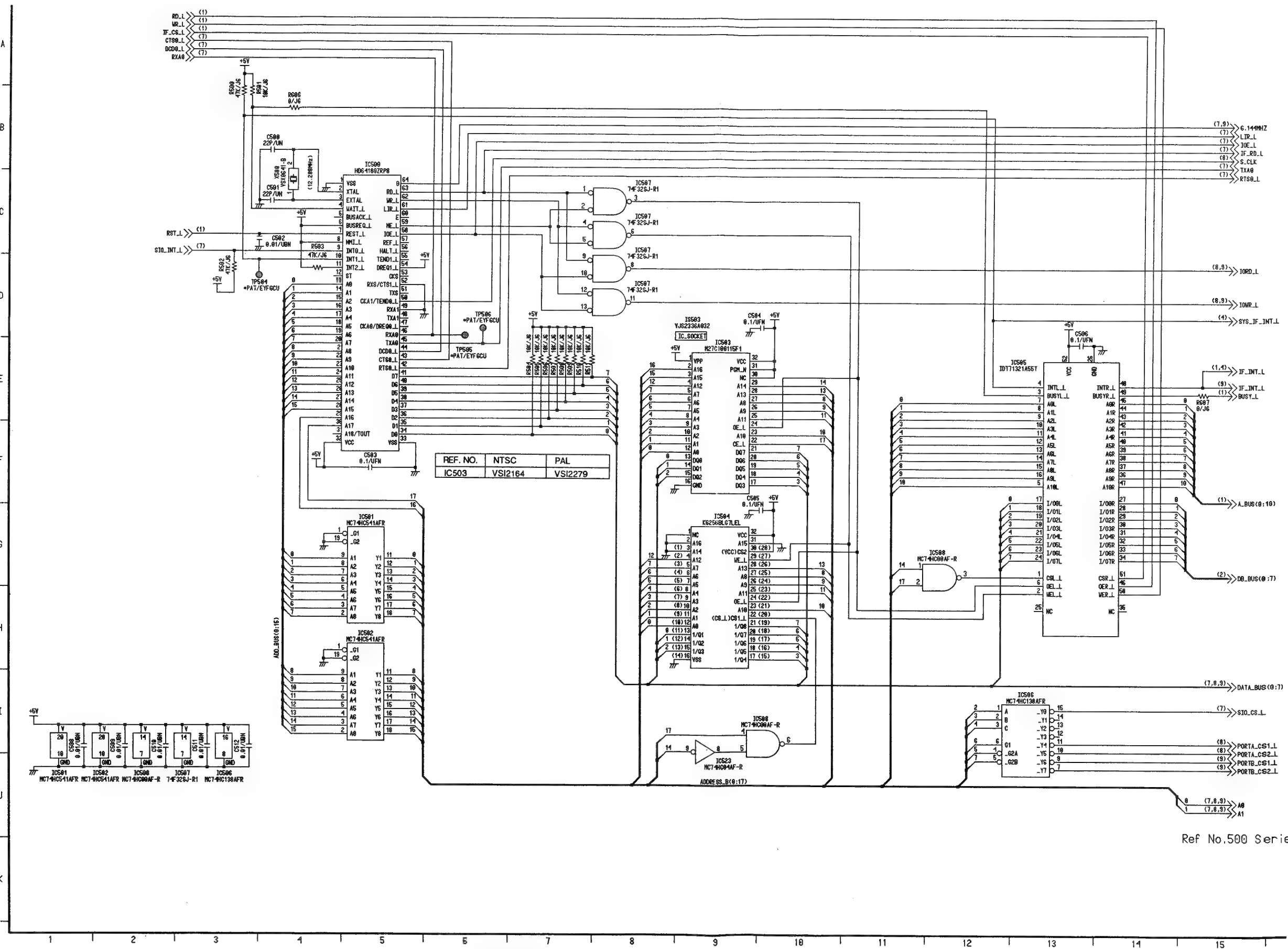
SYSCON (F2 4/14) MAIN 4 SCHEMATIC DIAGRAM



SYSNCON (F2 5/14) MAIN 5 SCHEMATIC DIAGRAM

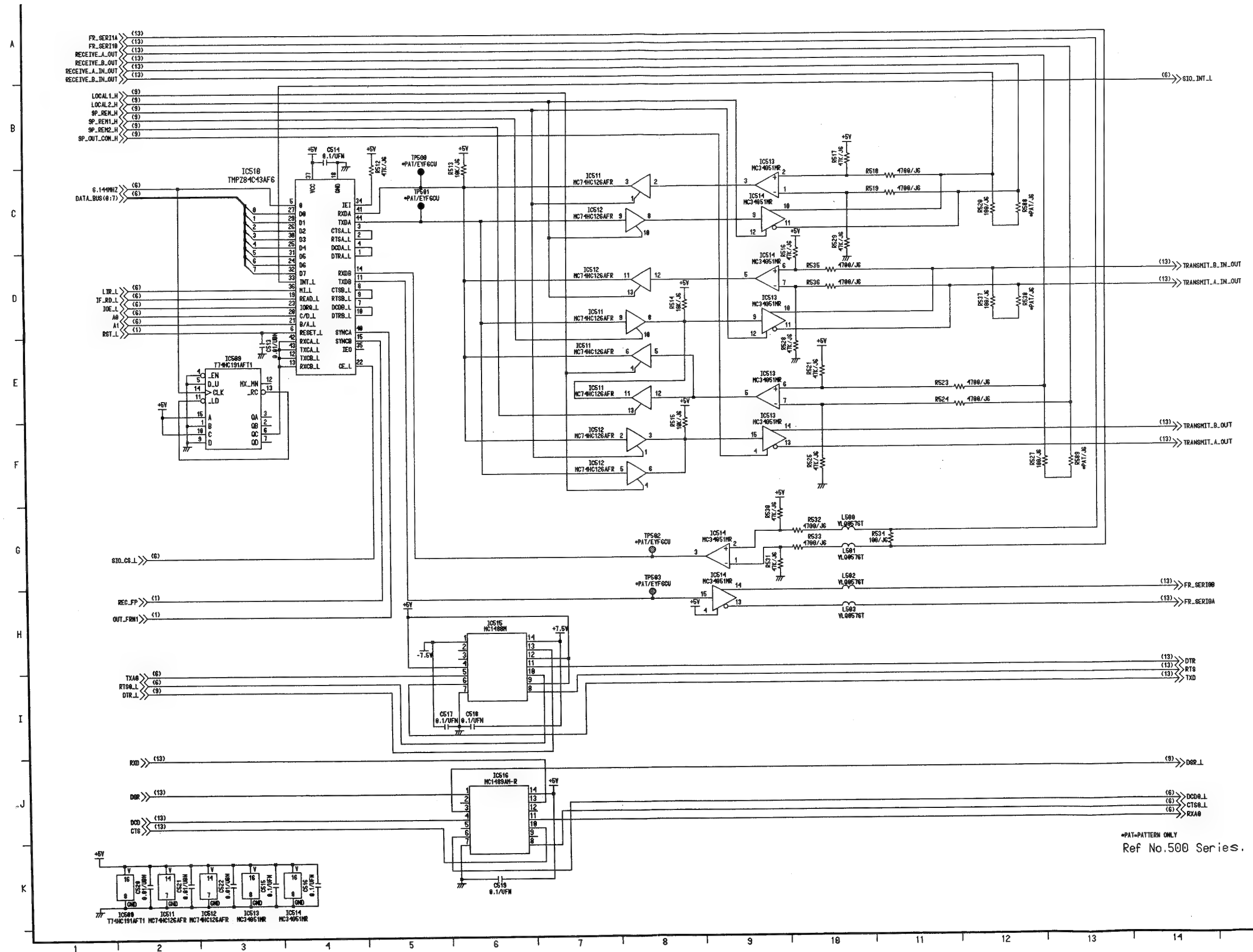


SYSCON (F2 6/14) I/F 1 SCHEMATIC DIAGRAM

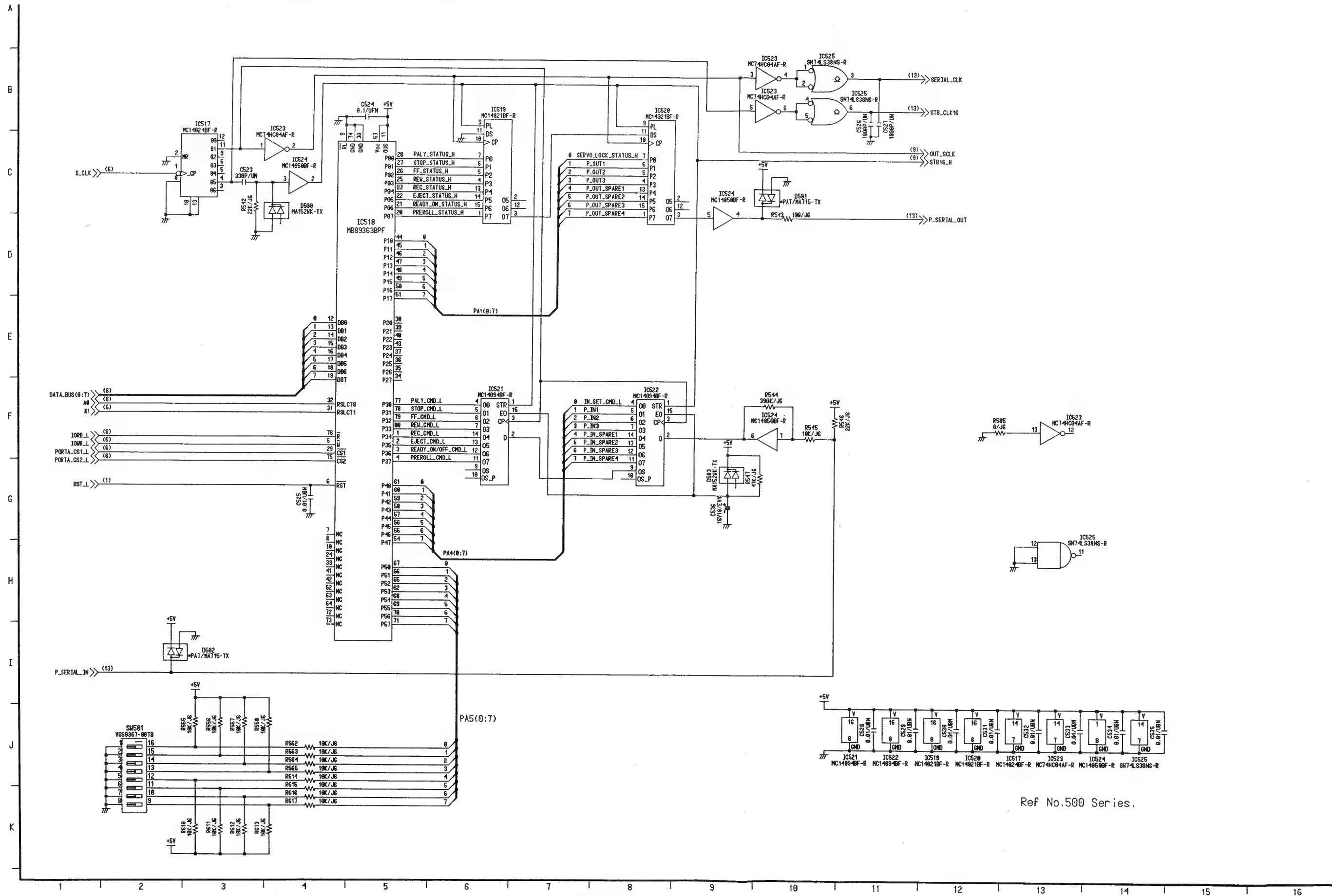


Ref No.500 Series.

SYSCON (F2 7/14) I/F 2 SCHEMATIC DIAGRAM

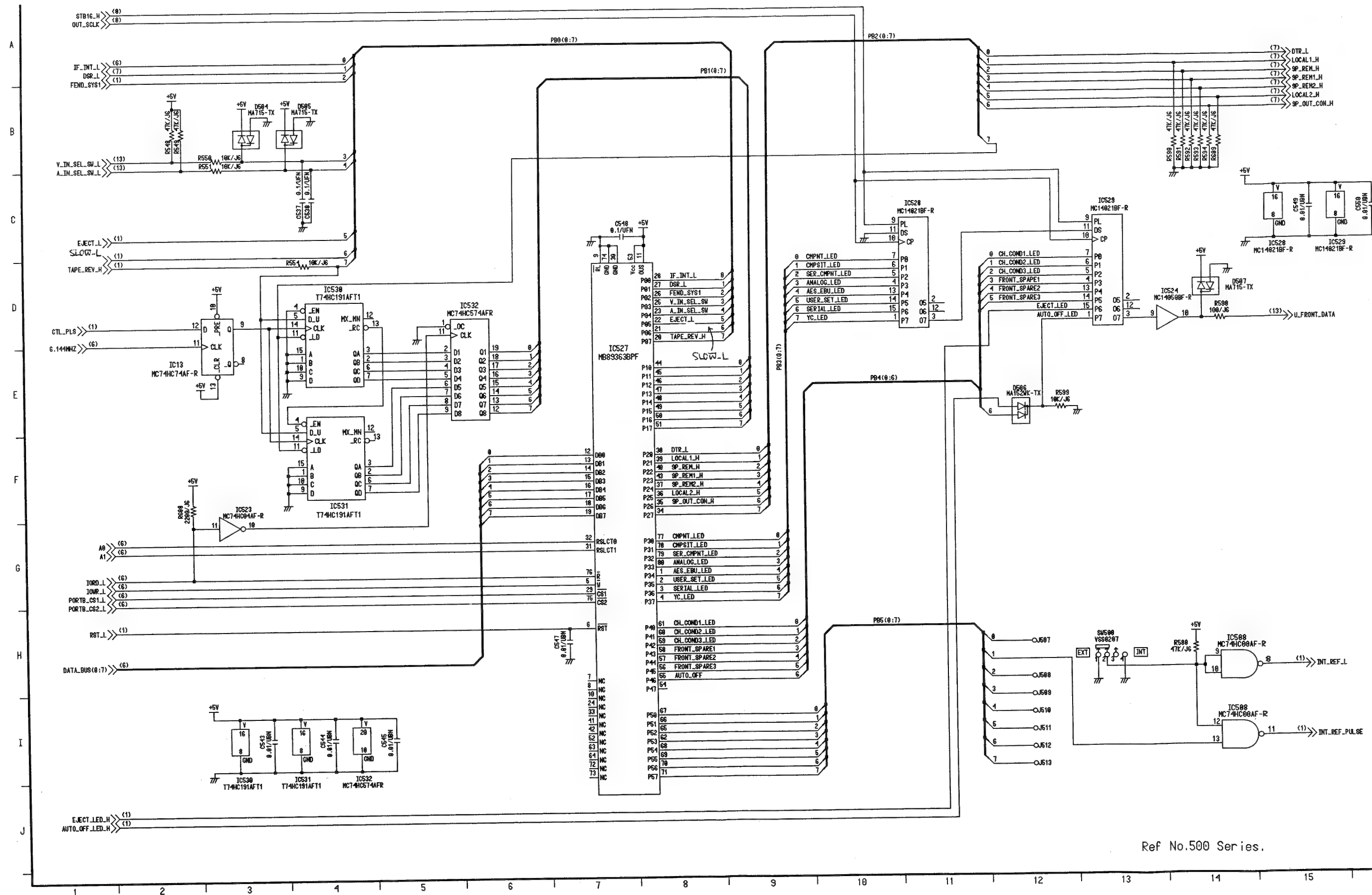


SYSCON (F2 8/14) I/F 3 SCHEMATIC DIAGRAM

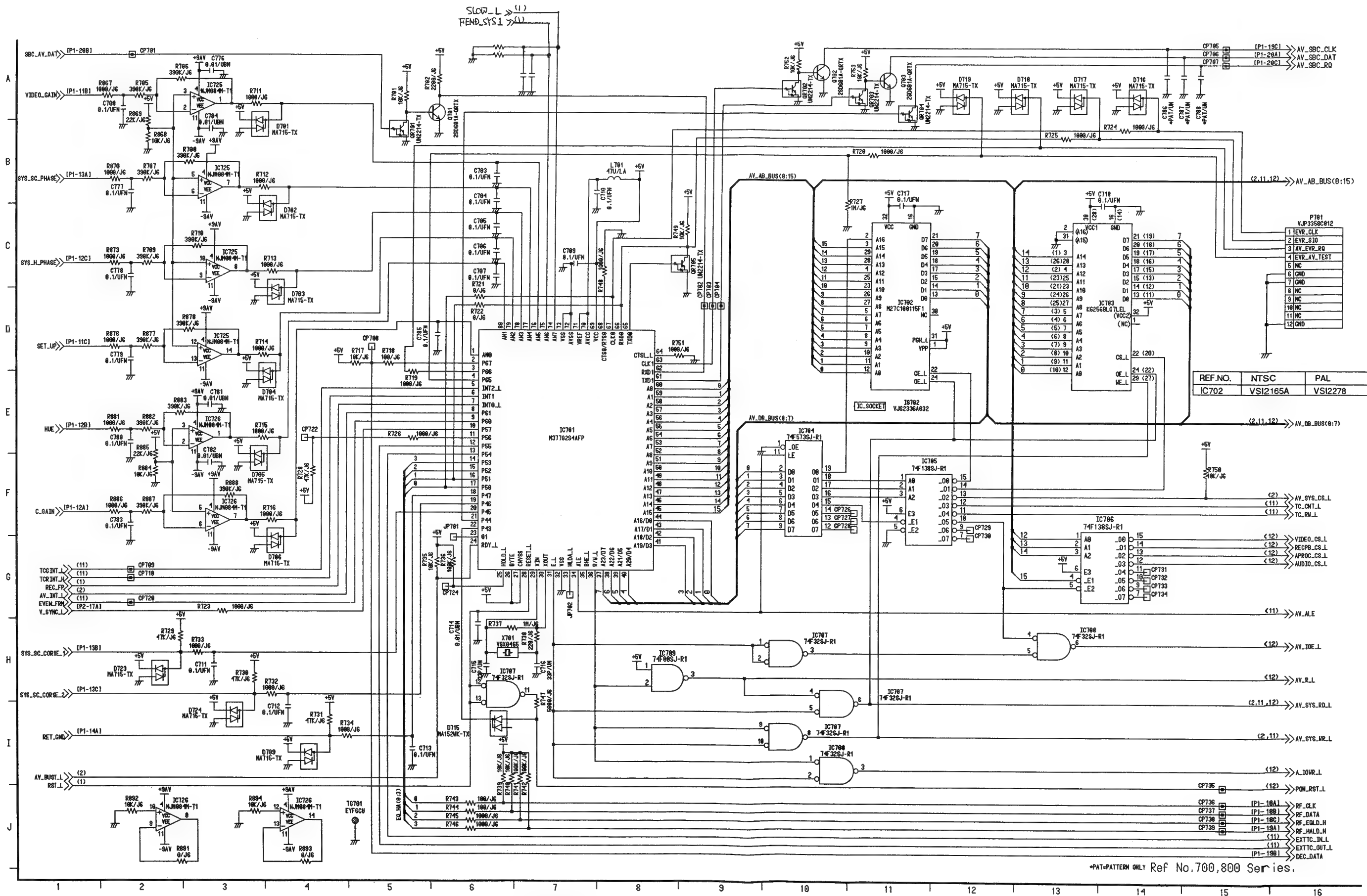


Ref No.500 Series.

SYSCON (F2 9/14) I/F 4 SCHEMATIC DIAGRAM

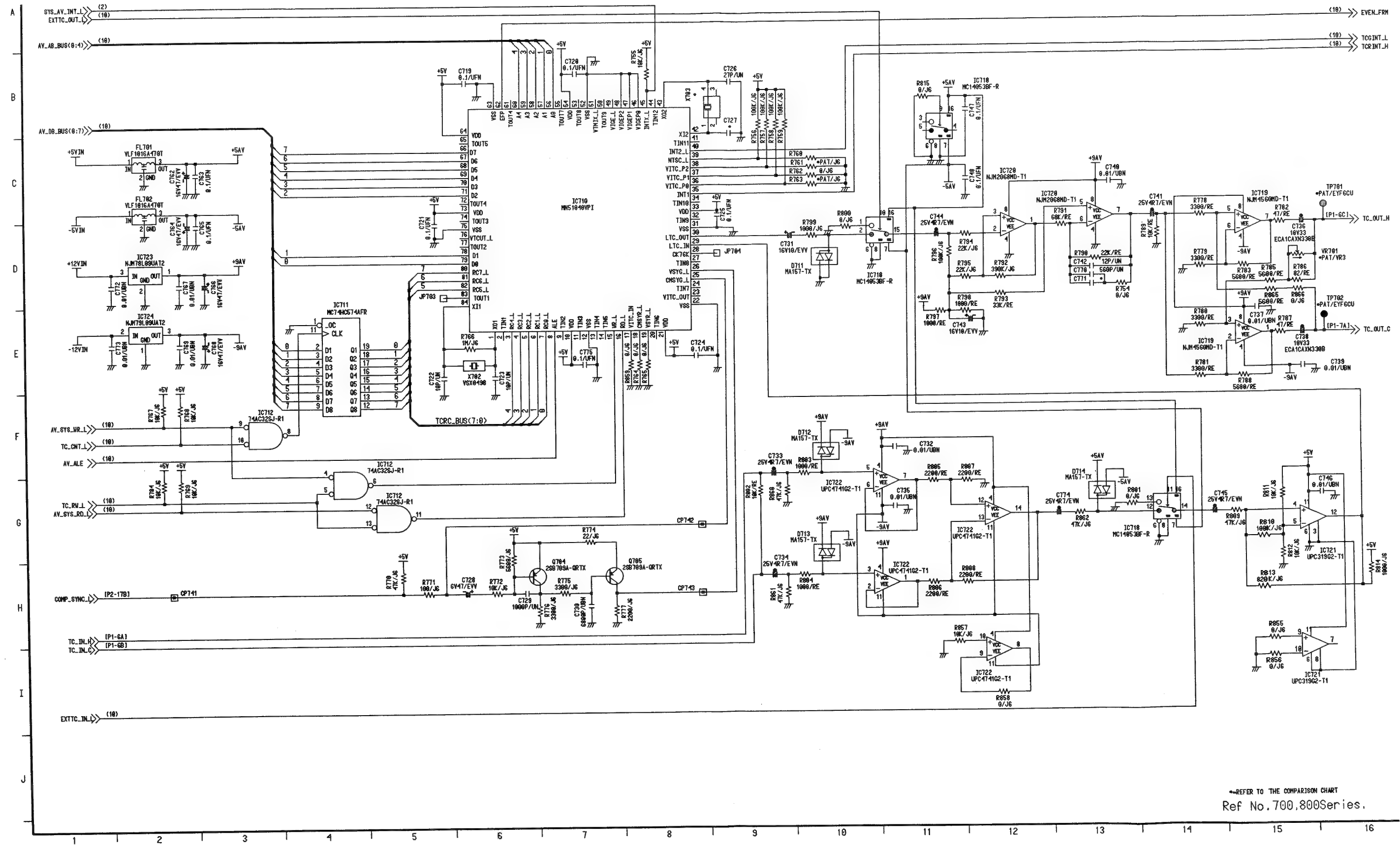


SYSCON (F2 10/14) AV I/F 1 SCHEMATIC DIAGRAM



*PAT=PATTERN ONLY Ref No.700,800 Series.

SYSN (F2 11/14) AV I/F 2 SCHEMATIC DIAGRAM

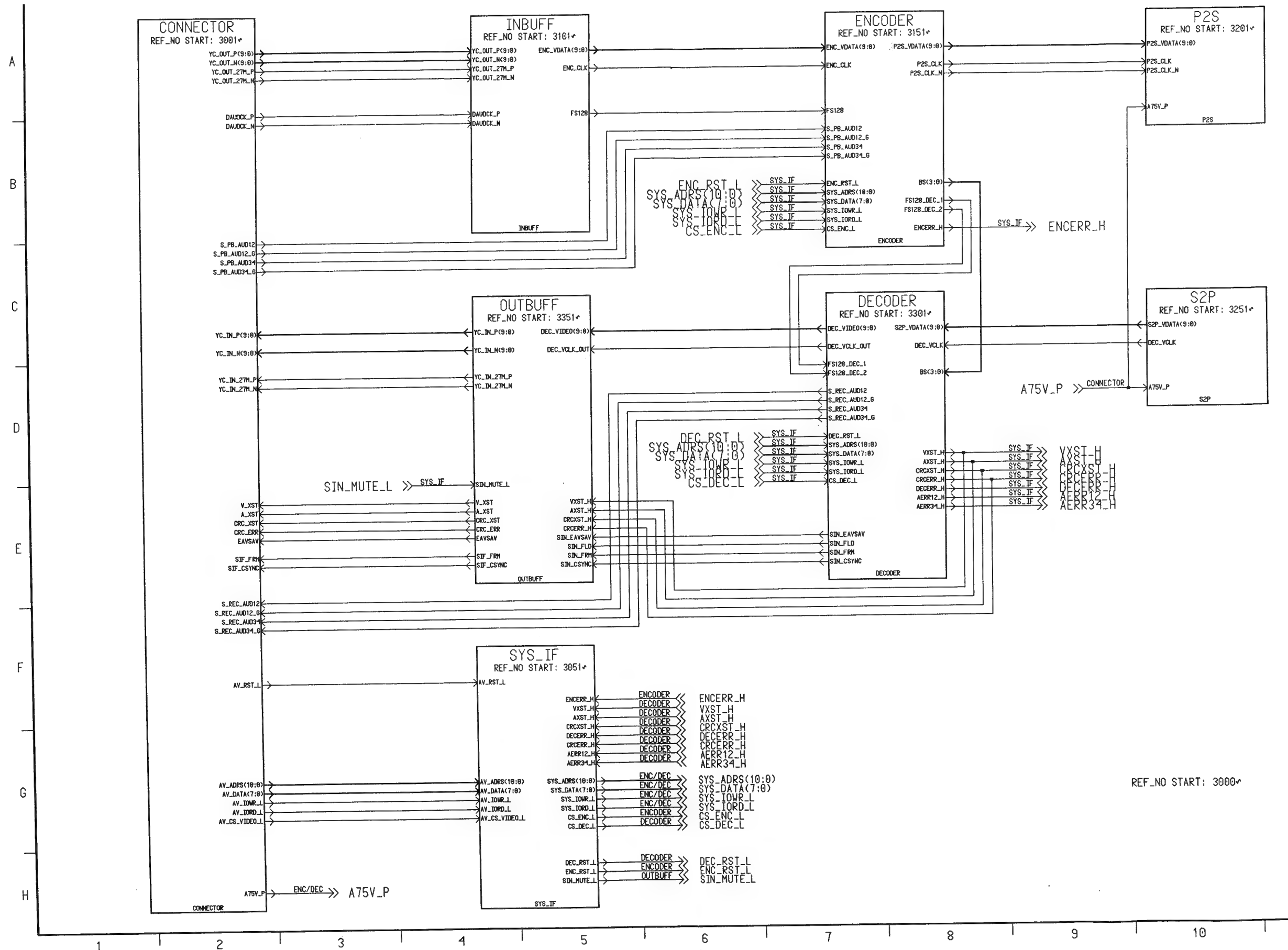


SYSCON (F2 14/14) COMPARISON CHART BETWEEN MODELS

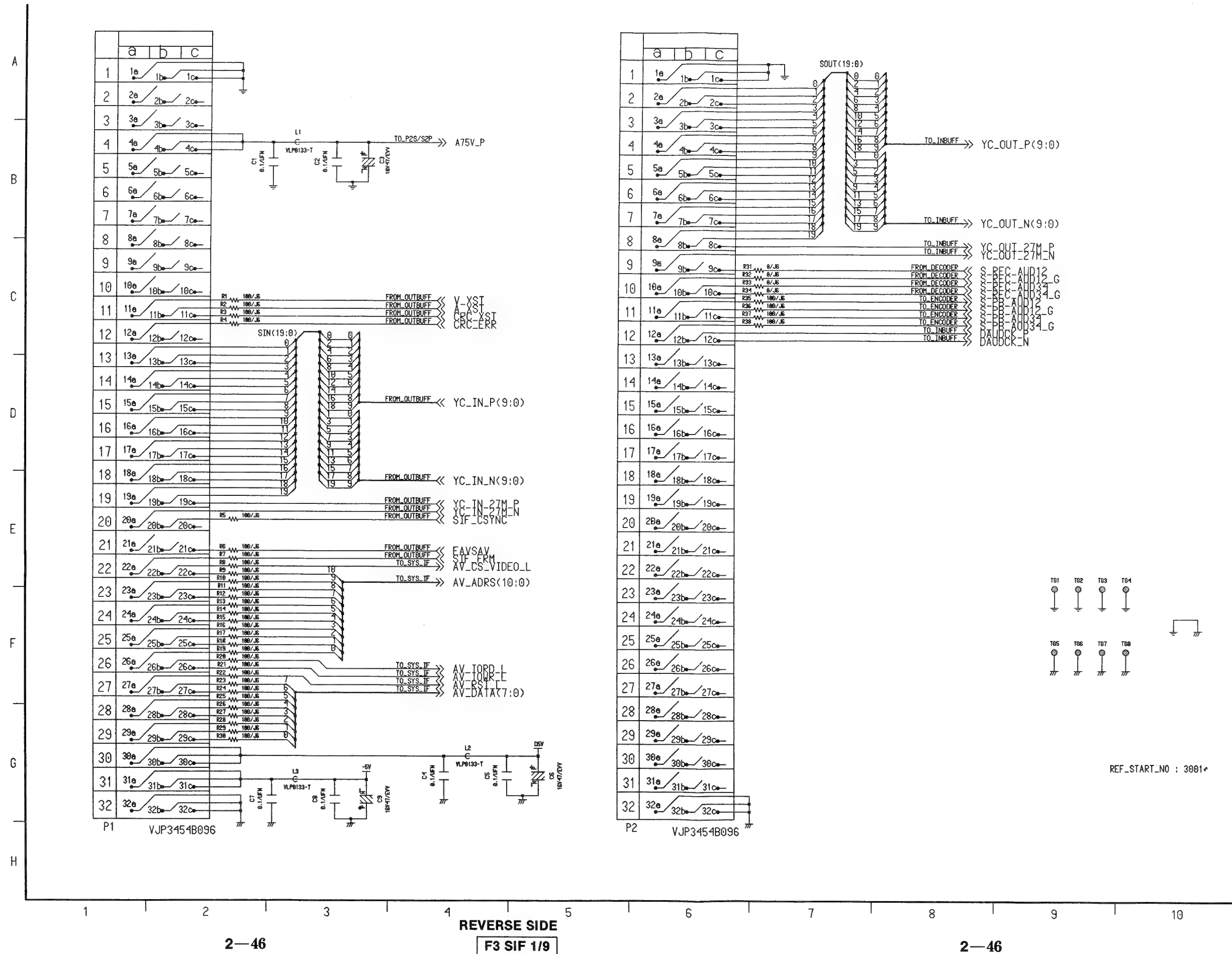
\$REF\$	NTSC	PAL	ON
C2	*PAT/UBN	*PAT/UBN	0.01/UBN
C3	*PAT/UBN	*PAT/UBN	0.01/UBN
C4	*PAT/UBN	*PAT/UBN	0.01/UBN
C40	*PAT/UBN	*PAT/UBN	0.01/UBN
C41	*PAT/UBN	*PAT/UBN	0.01/UBN
C42	*PAT/UBN	*PAT/UBN	0.01/UBN
C43	*PAT/UBN	*PAT/UBN	0.01/UBN
C44	*PAT/UBN	*PAT/UBN	0.01/UBN
C45	*PAT/UBN	*PAT/UBN	0.01/UBN
C48	*PAT/UBN	*PAT/UBN	0.01/UBN
C5	*PAT/UBN	*PAT/UBN	0.01/UBN
C50	*PAT/UBN	*PAT/UBN	0.01/UBN
C52	*PAT/UBN	*PAT/UBN	0.01/UBN
C54	*PAT/UBN	*PAT/UBN	0.01/UBN
C6	*PAT/UBN	*PAT/UBN	0.01/UBN
C61	*PAT/EVV	*PAT/EVV	16V22/EVV
C62	*PAT/EVN	*PAT/EVN	25V2R2/EVN
C63	*PAT/EVN	*PAT/EVN	25V2R2/EVN
C64	*PAT/EVN	*PAT/EVN	25V2R2/EVN
C7	*PAT/UBN	*PAT/UBN	0.01/UBN
C701	*PAT/UFN	*PAT/UFN	0.1/UFN
C702	*PAT/UFN	*PAT/UFN	0.1/UFN
C727	18P/UN	22P/UN	18P/UN
C75	*PAT/EVV	*PAT/EVV	16V22/EVV
C771	120P/UN	2200P/UBN	120P/UN
C786	*PAT/UN	*PAT/UN	12P/UN
C787	*PAT/UN	*PAT/UN	12P/UN
C788	*PAT/UN	*PAT/UN	12P/UN
C8	*PAT/UBN	*PAT/UBN	0.01/UBN
C82	*PAT/UBN	*PAT/UBN	0.01/UBN
C84	*PAT/UN	*PAT/UN	22P/UN
C85	*PAT/UN	*PAT/UN	12P/UN
D501	*PAT	*PAT	MA715-TX
D502	*PAT	*PAT	MA715-TX
R143	*PAT/J6	*PAT/J6	0/J6
R149	*PAT/J6	*PAT/J6	0/J6
R279	*PAT/J6	*PAT/J6	0/J6
R282	*PAT/J6	*PAT/J6	0/J6
R32	*PAT/J6	*PAT/J6	10K/J6
R331	*PAT/J6	*PAT/J6	390K/J6
R36	*PAT/J6	*PAT/J6	10K/J6
R37	*PAT/J6	*PAT/J6	390K/J6
R538	*PAT/J6	*PAT/J6	0/J6

\$REF\$	NTSC	PAL	ON
R588	*PAT/J6	*PAT/J6	0/J6
R589	*PAT/J6	*PAT/J6	0/J6
R760	0/J6	*PAT/J6	0/J6
R761	*PAT/J6	*PAT/J6	0/J6
R763	*PAT/J6	*PAT/J6	0/J6
R88	100K/J6	*PAT/J6	100K/J6
R89	*PAT/J6	100K/J6	100K/J6
TP1	*PAT	*PAT	EYF6CU
TP10	*PAT	*PAT	EYF6CU
TP11	*PAT	*PAT	EYF6CU
TP12	*PAT	*PAT	EYF6CU
TP2	*PAT	*PAT	EYF6CU
TP3	*PAT	*PAT	EYF6CU
TP4	*PAT	*PAT	EYF6CU
TP5	*PAT	*PAT	EYF6CU
TP500	*PAT	*PAT	EYF6CU
TP501	*PAT	*PAT	EYF6CU
TP502	*PAT	*PAT	EYF6CU
TP503	*PAT	*PAT	EYF6CU
TP504	*PAT	*PAT	EYF6CU
TP505	*PAT	*PAT	EYF6CU
TP506	*PAT	*PAT	EYF6CU
TP6	*PAT	*PAT	EYF6CU
TP7	*PAT	*PAT	EYF6CU
TP701	*PAT	*PAT	EYF6CU
TP702	*PAT	*PAT	EYF6CU
VR701	*PAT/VR3	*PAT/VR3	100/VR3
X703	VSX0614-T	VSX0615-T	VSX0614-T

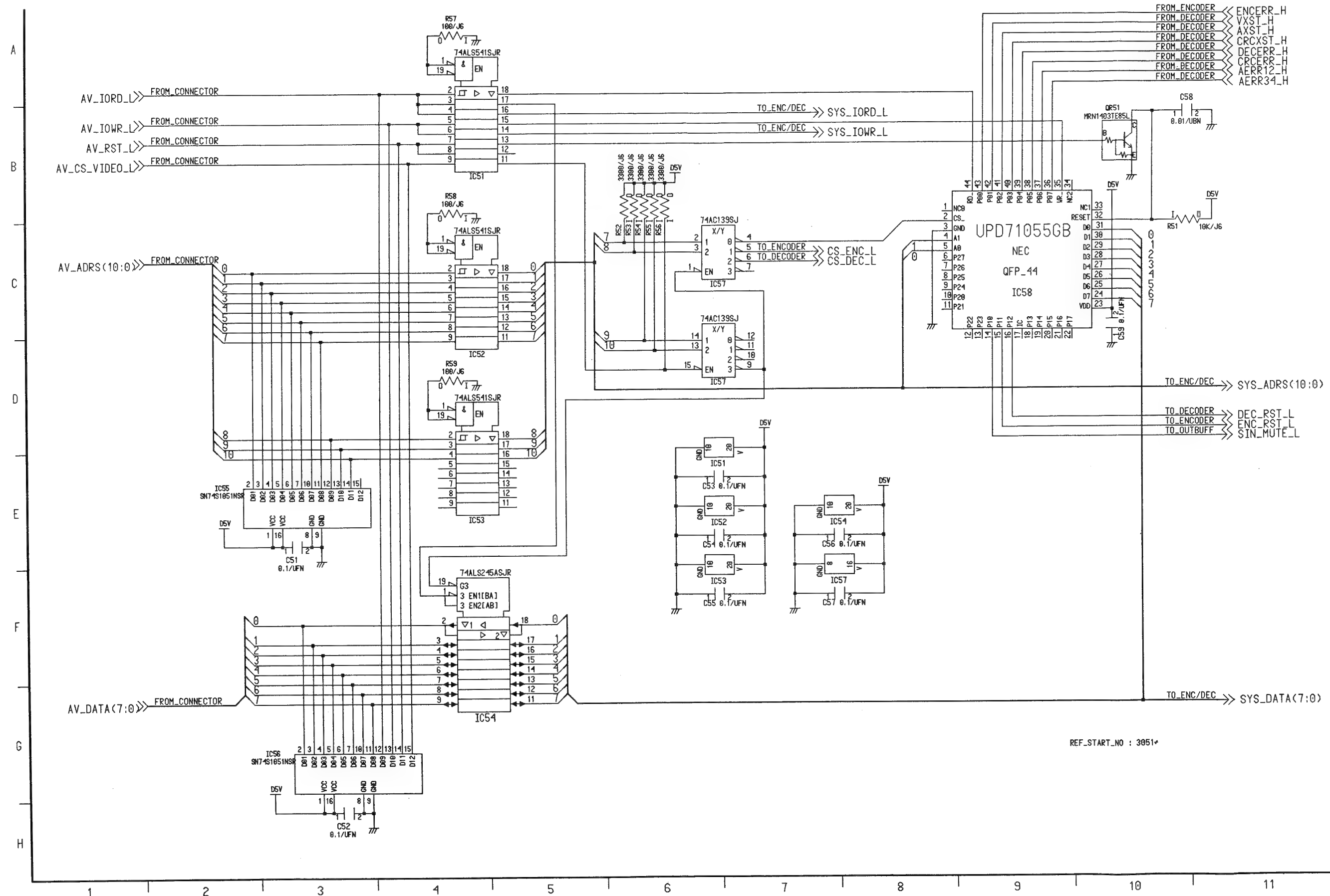
[AJ-YA750] SIF (F3 1/9) OVERALL SCHEMATIC DIAGRAM



[AJ-YA750] SIF (F3 2/9) CONNECTOR SCHEMATIC DIAGRAM

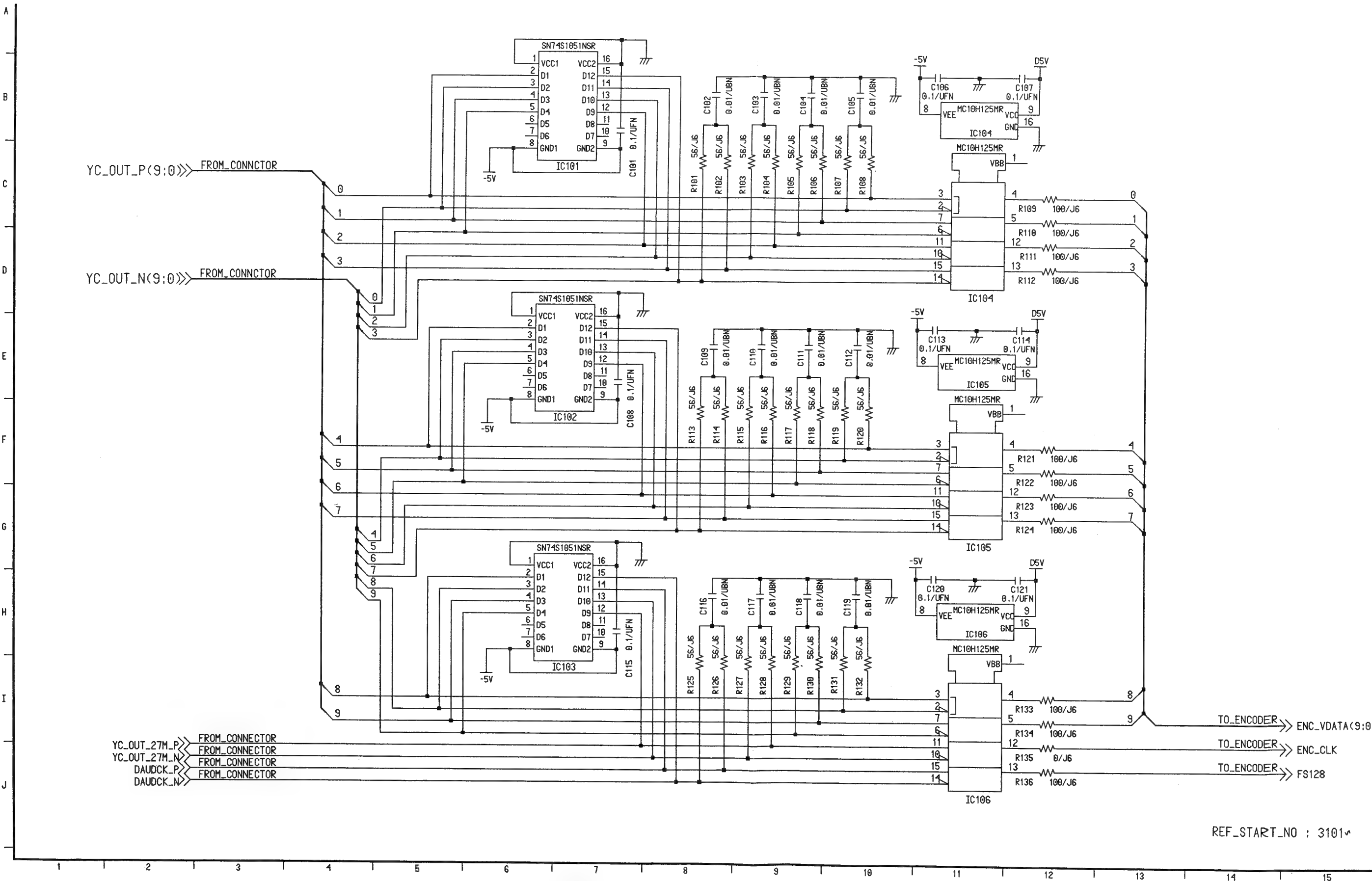


[AJ-YA750] SIF (F3 3/9) SYS IF SCHEMATIC DIAGRAM



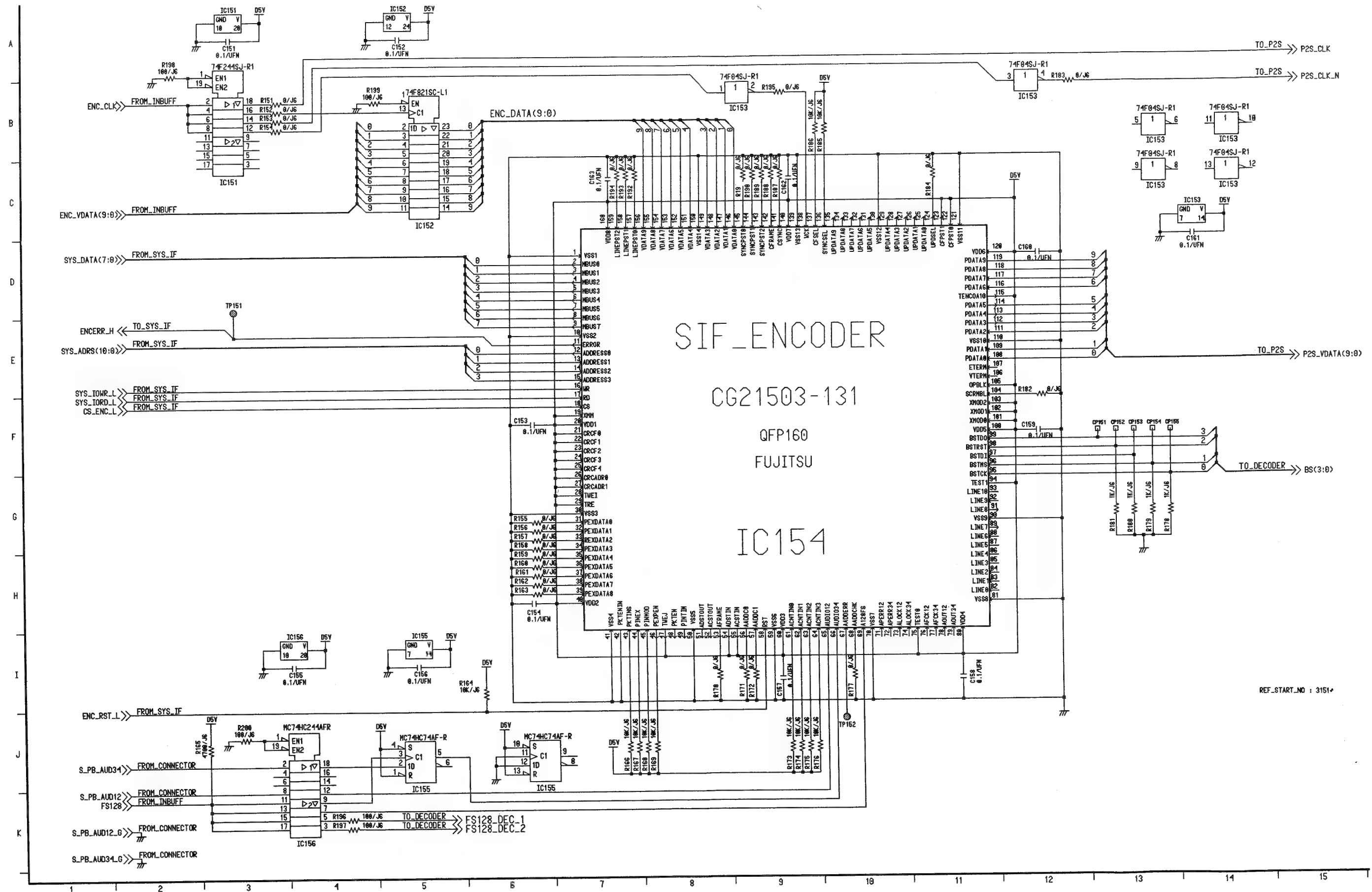
REF_START_NO : 3051*

[AJ-YA750] SIF (F3 4/9) IN BUFF SCHEMATIC DIAGRAM

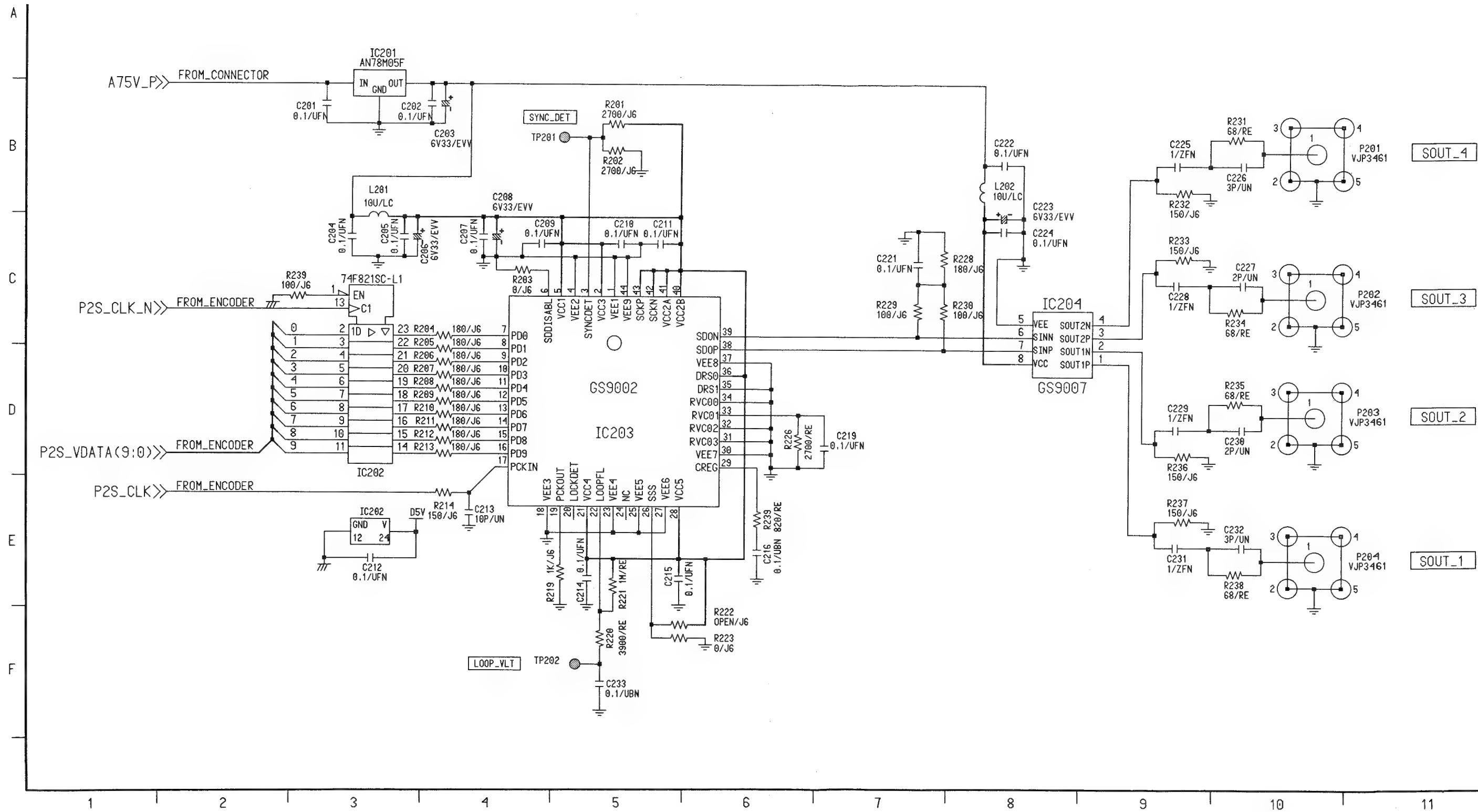


REF_START_NO : 3101

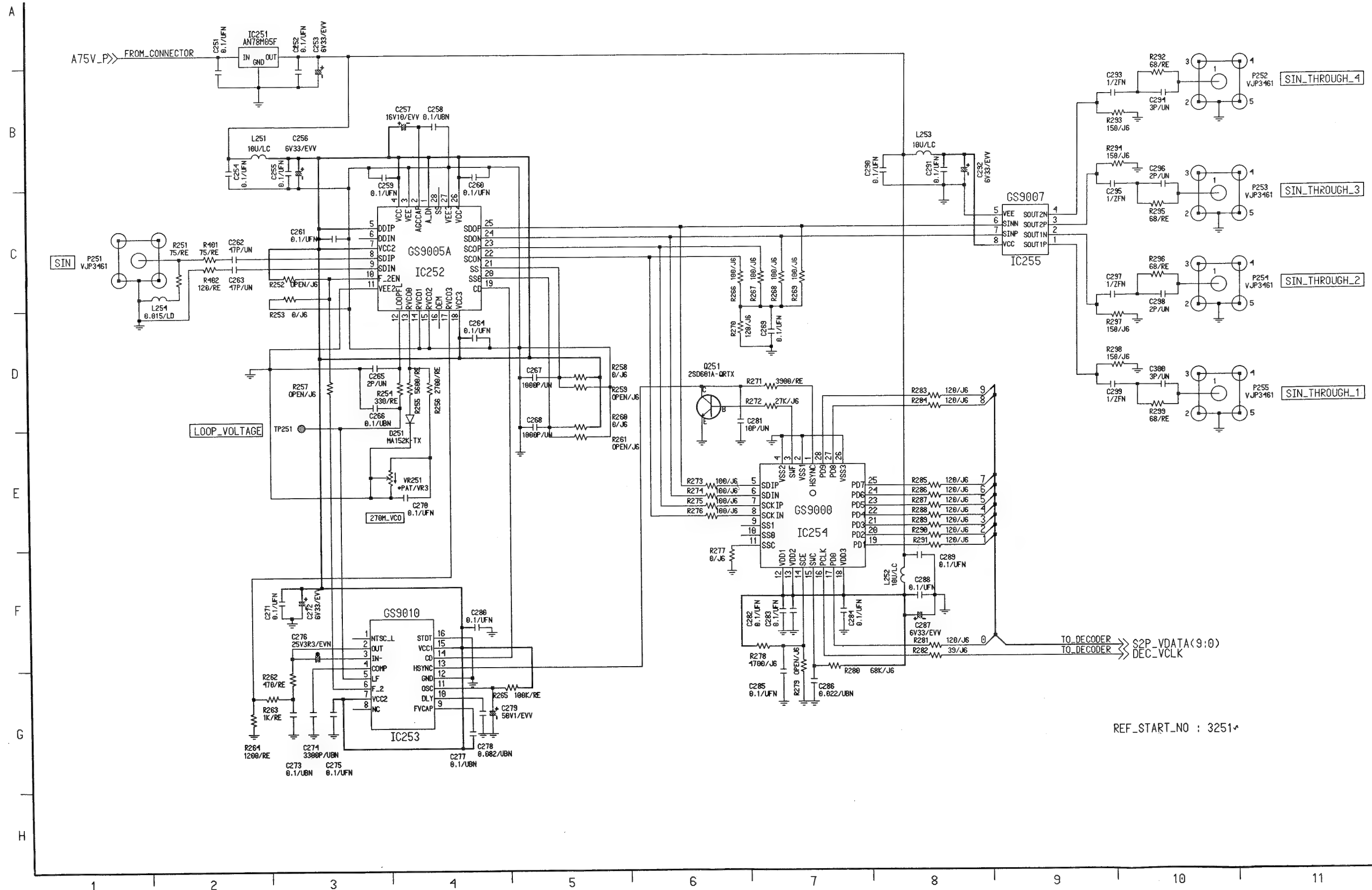
[AJ-YA750] SIF (F3 5/9) ENCODER SCHEMATIC DIAGRAM



[AJ-YA750] SIF (F3 6/9) P2S SCHEMATIC DIAGRAM

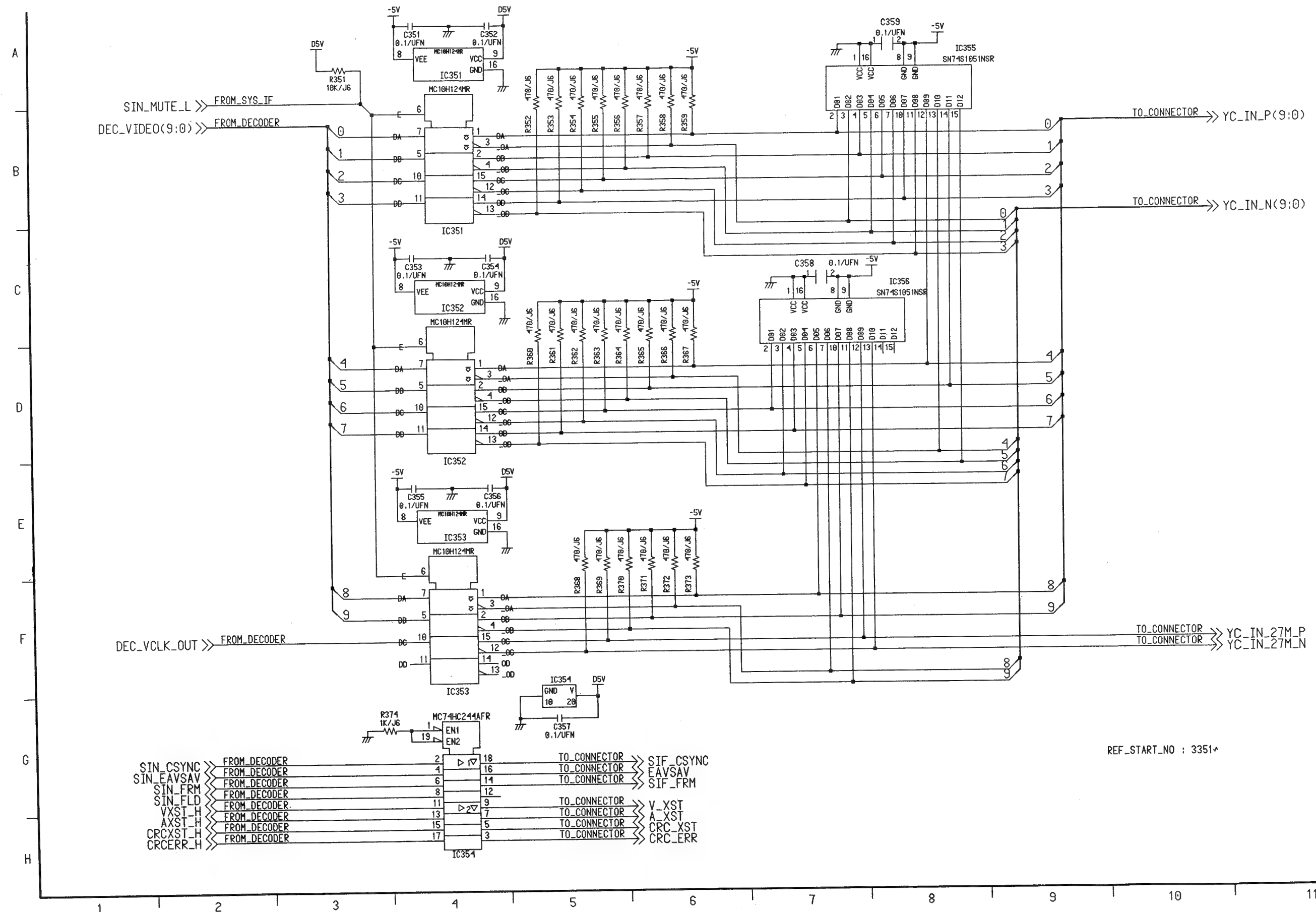


[AJ-YA750] SIF (F3 7/9) S2P SCHEMATIC DIAGRAM



A —
B —
C —
D —
E —
F —
G —
H —
I —
J —

[AJ-YA750] SIF (F3 9/9) OUT BUFF SCHEMATIC DIAGRAM



REF_START_NO : 3351*

V OUT (F4) COMPARISON CHART BETWEEN MODELS

REF.NO.	NTSC	PAL
	VEP83221A	VEP83221B
C8107	ECUV1H102JV	ECUV1H181JCV
C8150	---	ECUV1E104ZFV
C8151	---	ECUV1E104ZFV
C8152	---	ECUV1H103KBV
C8153	---	ECUV1H103KBV
C8154	---	ECEV1HN010QR
C8155	---	ECUV1H102JV
C8156	---	ECUV1E104ZFV
C8157	---	ECUV1E104ZFV
C8166	ECUV1H470JCV	ECUV1H270JCV
C8167	ECUV1H470JCV	ECUV1H270JCV
C8204	ECUV1H102JV	ECUV1H181JCV
C8250	---	ECUV1E104ZFV
C8251	---	ECUV1E104ZFV
C8252	---	ECUV1H103KBV
C8253	---	ECUV1H103KBV
C8254	---	ECEV1HN100QR
C8255	---	ECUV1H102JV
C8256	---	ECUV1E104ZFV
C8725	ECUV1H120JCV	---
C8729	ECUV1H100DCV	---
C8810	ECUV1H391JVC	ECUV1H151JCV
C8811	ECUV1H151JCV	ECUV1H471JCV
C8852	---	ECUV1E104ZFV
C8853	---	ECUV1H330JCV
C8854	---	ECUV1E104ZFV
C8855	---	ECUV1E104ZFV
C8856	---	ECUV1E104KBN
C8878	ECUV1H330JCV	ECUV1H270JCV
C8879	ECUV1H271JCV	ECUV1H221JCV
C8880	ECUV1H220JCV	---
C8881	ECUV1H680JCV	ECUV1H270JCV
C8882	ECUV1H070DCV	---
C8883	ECUV1H121JCV	ECUV1H101JCV
C8884	---	ECUV1H100DCV
C8885	ECUV1H100DCV	ECUV1H470JCV
C8886	---	ECUV1H330JCV
C8906	ECUV1H220JCV	ECUV1H390JCV
C8907	ECUV1H220JCV	ECUV1H390JCV
C8946	ECUV1H180JCV	ECUV1H330JCV
C8947	ECUV1H121JCV	ECUV1H271JCV
C8953	ECUV1H120JCV	---
C8960	ECUV1H330JCV	ECUV1H270JCV
C8970	ECUV1H330JCV	ECUV1H270JCV
D8150	---	MA152K-TX

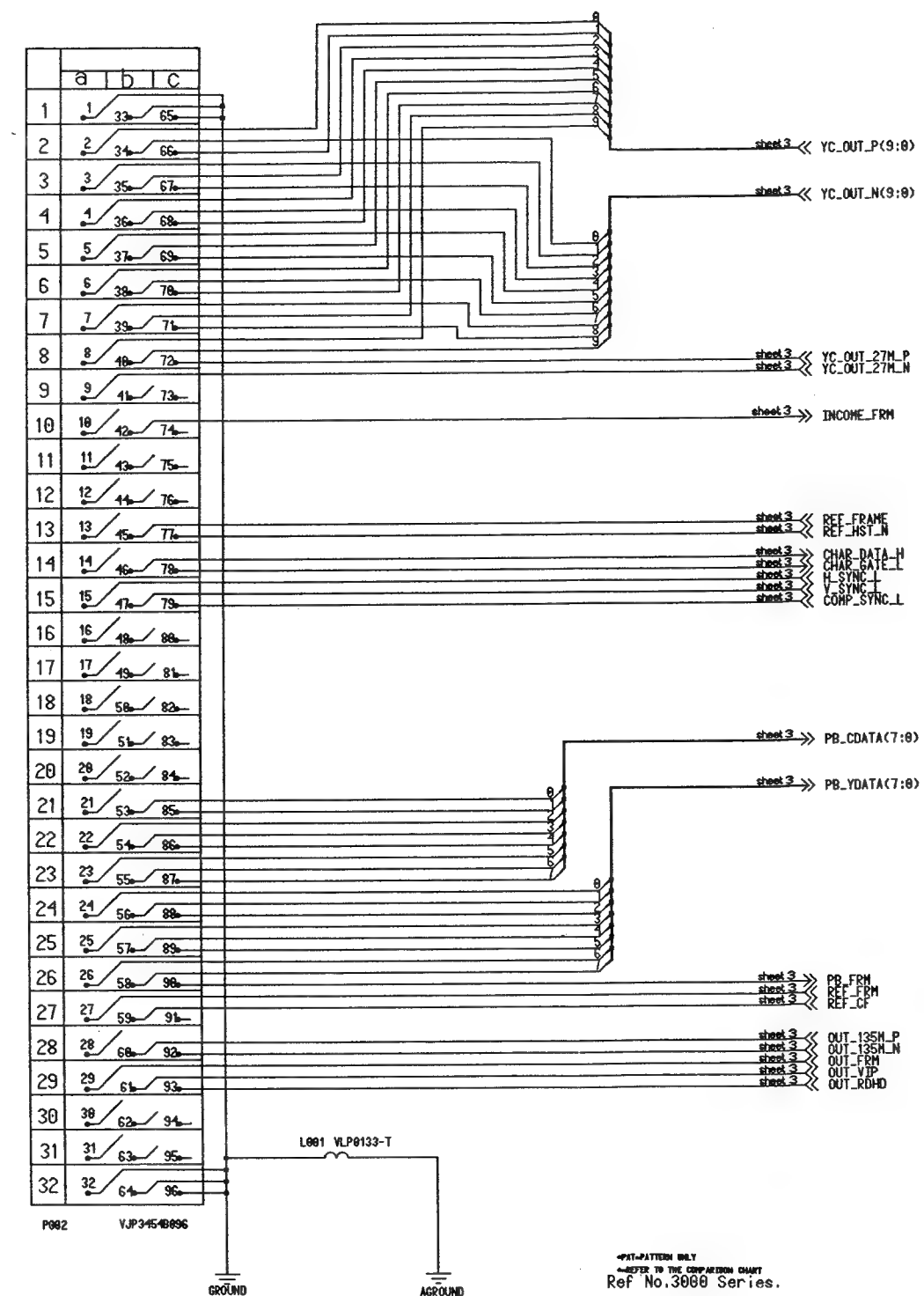
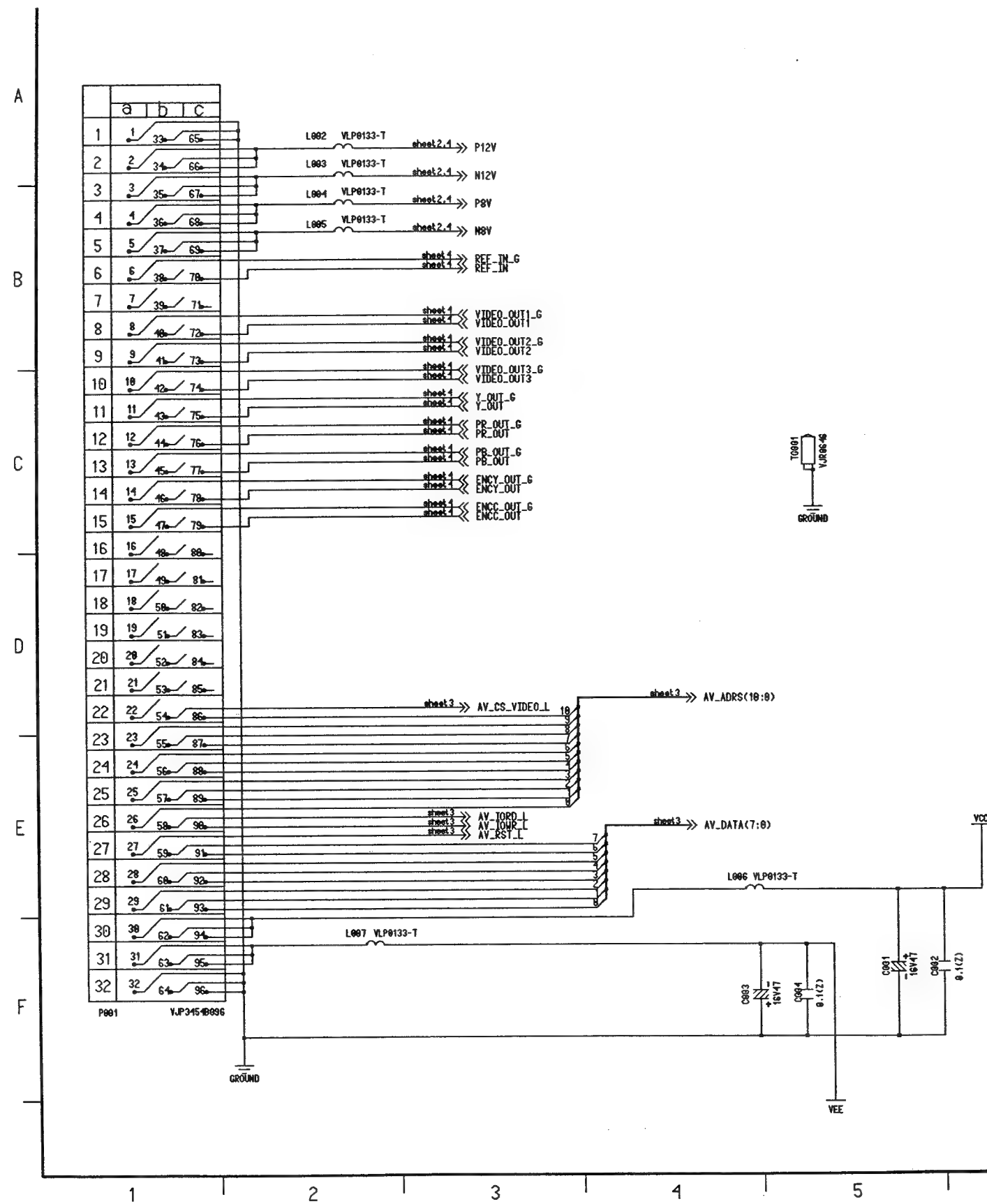
REF.NO.	NTSC	PAL
D8250	---	MA152K-TX
IC8150	---	MC74HC125AFR
IC8151	---	NJM082BM-T1
IC8251	---	NJM082BM-T1
IC8340	VSI2272	VSI2273A
L8650	VLQ0163J680	VLQ0163J390
L8803	VLQ0163J181	VLQ0163J180
L8808	VLQ0163J270	VLQ0163J150
L8809	VLQ0163J6R8	VLQ0163J5R6
L8810	VLQ0163J5R6	VLQ0163J6R8
L8940	VLQ0163J470	VLQ0163J101
L8960	VLQ0163J560	VLQ0163J470
L8970	VLQ0163J560	VLQ0163J470
Q8810	---	XN6501-TX
Q8811	---	MSC2295-BT1
Q8812	---	MSC2295-BT1
Q8813	---	MSB709-RT2
R8057	ERJ3GEYJ101V	---
R8059	ERJ3GEYJ101V	---
R8070	ERJ3GEYJ153V	ERJ3GEYJ183V
R8076	ERJ3GEYJ821V	ERJ3GEYJ471V
R8077	ERJ3GEYJ223V	ERJ3GEYJ153V
R8094	---	ERJ3GEYJ333V
R8095	---	ERJ3GEYJ102V
R8096	---	ERJ3GEYJ102V
R8097	---	ERJ3GEYJ102V
R8099	---	ERDS2TJ222
R8131	ERJ3GEYJ822V	ERJ3GEYJ562V
R8132	ERJ3GEYJ222V	ERJ3GEYJ332V
R8140	ERJ3GEY0R00V	---
R8141	---	ERJ3GEY0R00V
R8150	---	ERJ3GEYJ471V
R8151	---	ERJ3GEYJ333V
R8152	---	ERJ3GEYJ103V
R8153	---	ERJ3GEYJ103V
R8154	---	ERJ3GEYJ223V
R8155	---	ERJ3GEYJ105V
R8156	---	ERJ3GEYJ102V
R8157	---	ERJ3GEYJ102V
R8158	ERJ3GEYJ102V	---
R8242	VRE0034E822	VRE0034E682
R8243	ERJ3GEYJ102V	ERJ3GEYJ222V
R8250	---	ERJ3GEYJ471V
R8251	---	ERJ3GEYJ333V
R8252	---	ERJ3GEYJ103V
R8253	---	ERJ3GEYJ103V

REVERSE SIDE

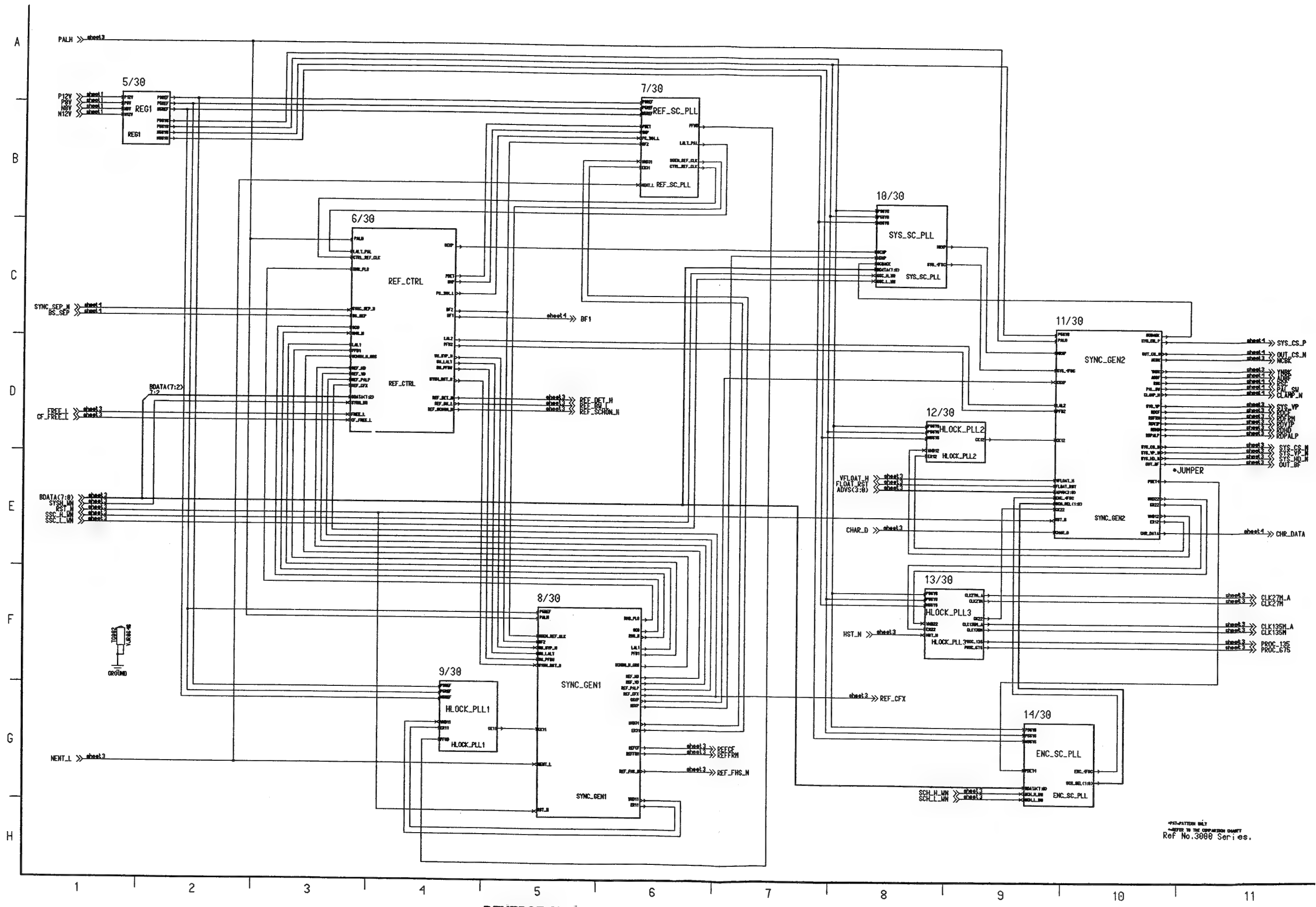
F3 SIF 9/9

REF. NO.	NTSC	PAL
R8254	---	ERJ3GEYJ223V
R8255	---	ERJ3GEYJ105V
R8256	---	ERJ3GEYJ102V
R8258	ERJ3GEYJ102V	---
R8285	ERJ3GEYJ333V	ERJ3GEYJ223V
R8718	ERJ3GEYJ151V	ERJ3GEYJ271V
R8739	ERJ3GEYJ101V	ERJ3GEYJ331V
R8770	ERJ3GEYJ101V	ERJ3GEYJ181V
R8799	VRE0034E752	---
R8839	ERJ3GEY0R00V	---
R8843	ERJ3GEYJ181V	ERJ3GEYJ101V
R8845	ERJ3GEYJ102V	---
R8849	ERJ3GEYJ102V	---
R8853	---	ERJ3GEYJ103V
R8854	---	ERJ3GEYJ391V
R8855	---	ERJ3GEYJ391V
R8856	---	ERJ3GEYJ103V
R8857	---	ERJ3GEYJ181V
R8858	---	ERJ3GEYJ331V
R8859	---	ERJ3GEYJ181V
R8860	---	ERJ3GEYJ562V
R8861	---	ERJ3GEYJ562V
R8862	---	ERJ3GEYJ223V
R8863	---	ERJ3GEYJ223V
R8864	---	ERJ3GEYJ223V
R8865	---	ERJ3GEYJ152V
R8866	---	ERJ3GEYJ470V
R8876	ERJ3GEY0R00	---
R8877	---	ERJ3GEYJ221V
R8890	---	ERJ3GEYJ102V
R8891	---	ERJ3GEYJ102V
R8902	ERJ3GEYJ821V	ERJ3GEYJ221V
R8903	ERJ3GEYJ563V	ERJ3GEYJ221V
R8924	ERJ3GEYJ181V	ERJ3GEYJ271V
R8941	VRE0034E752	---
R8960	VRE0034E102	---
R8961	VRE0034E560	---
R8965	VRE0034E271	---
R8970	VRE0034E271	---
SW8940	VSS0372	---
VC8800	---	ECV1ZW20X53T
VR8808	---	VRV0161B102T
X8070	VSX0081	VSX0363
X8150	---	VSX0567A
X8160	VSX0338	VSX0270
X8250	---	VSX0567A
X8280	VSX0338	VSX0270

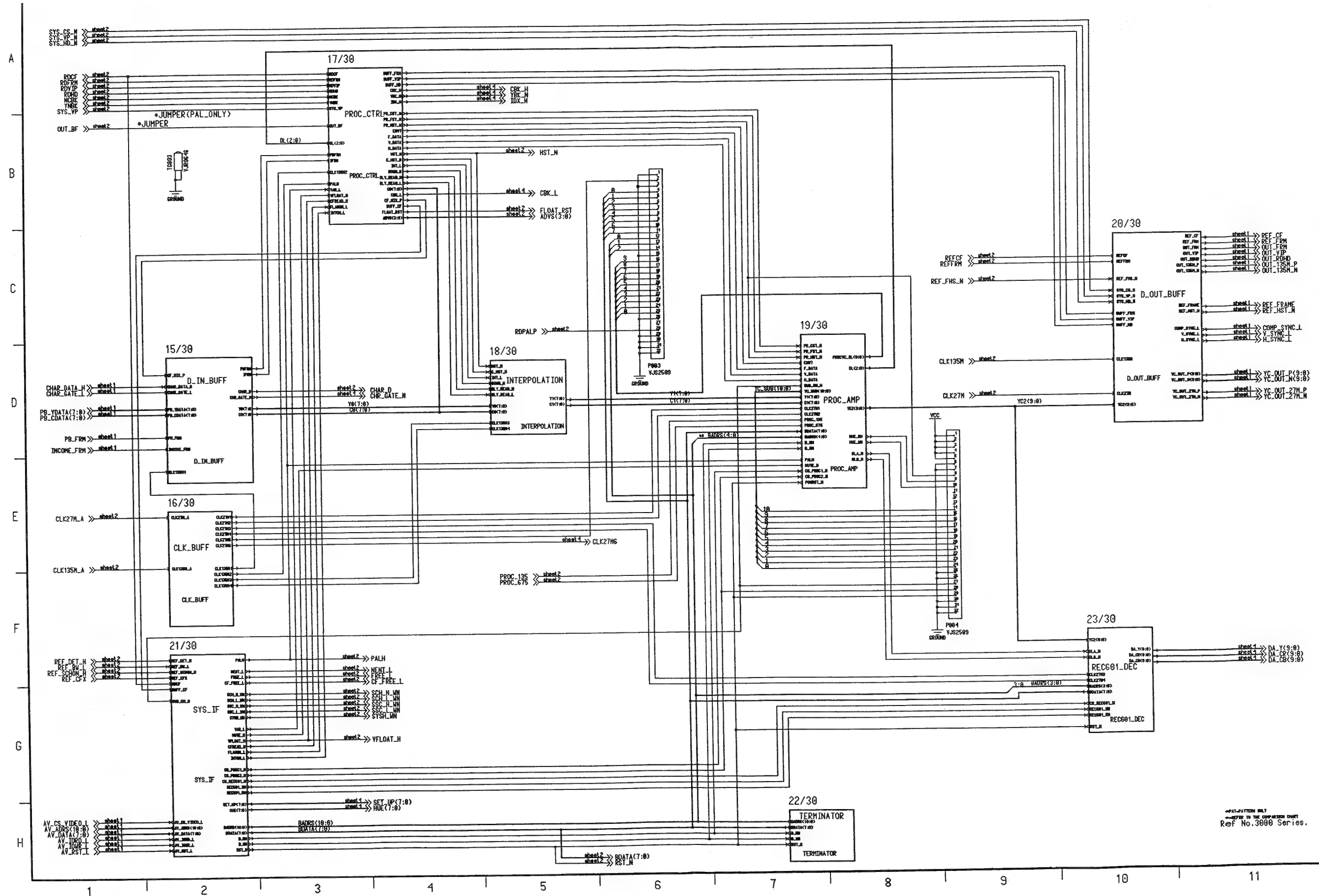
V OUT (F4 1/30) CONNECTOR SCHEMATIC DIAGRAM



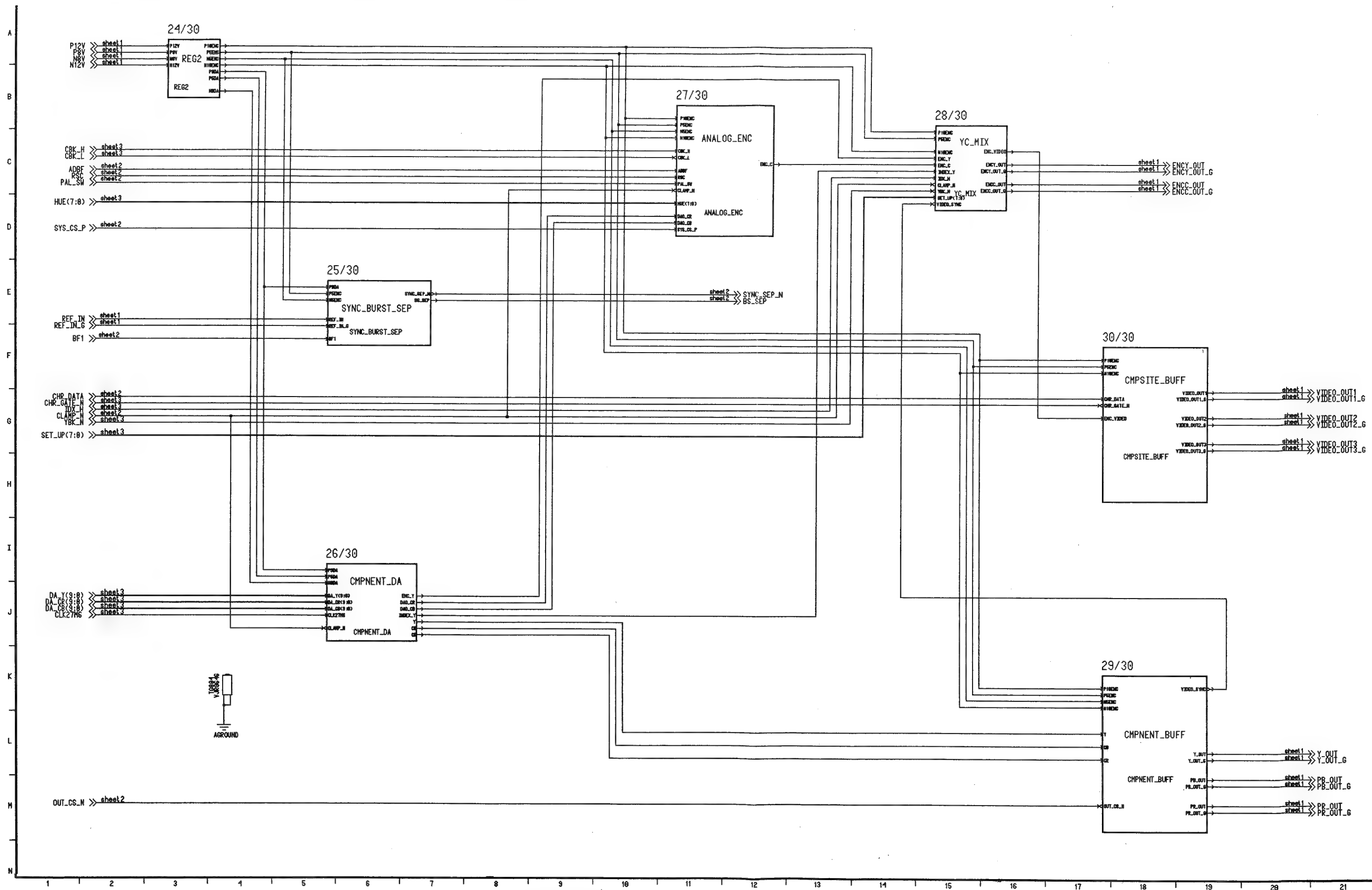
V OUT (F4 2/30) OVERALL 1 SCHEMATIC DIAGRAM



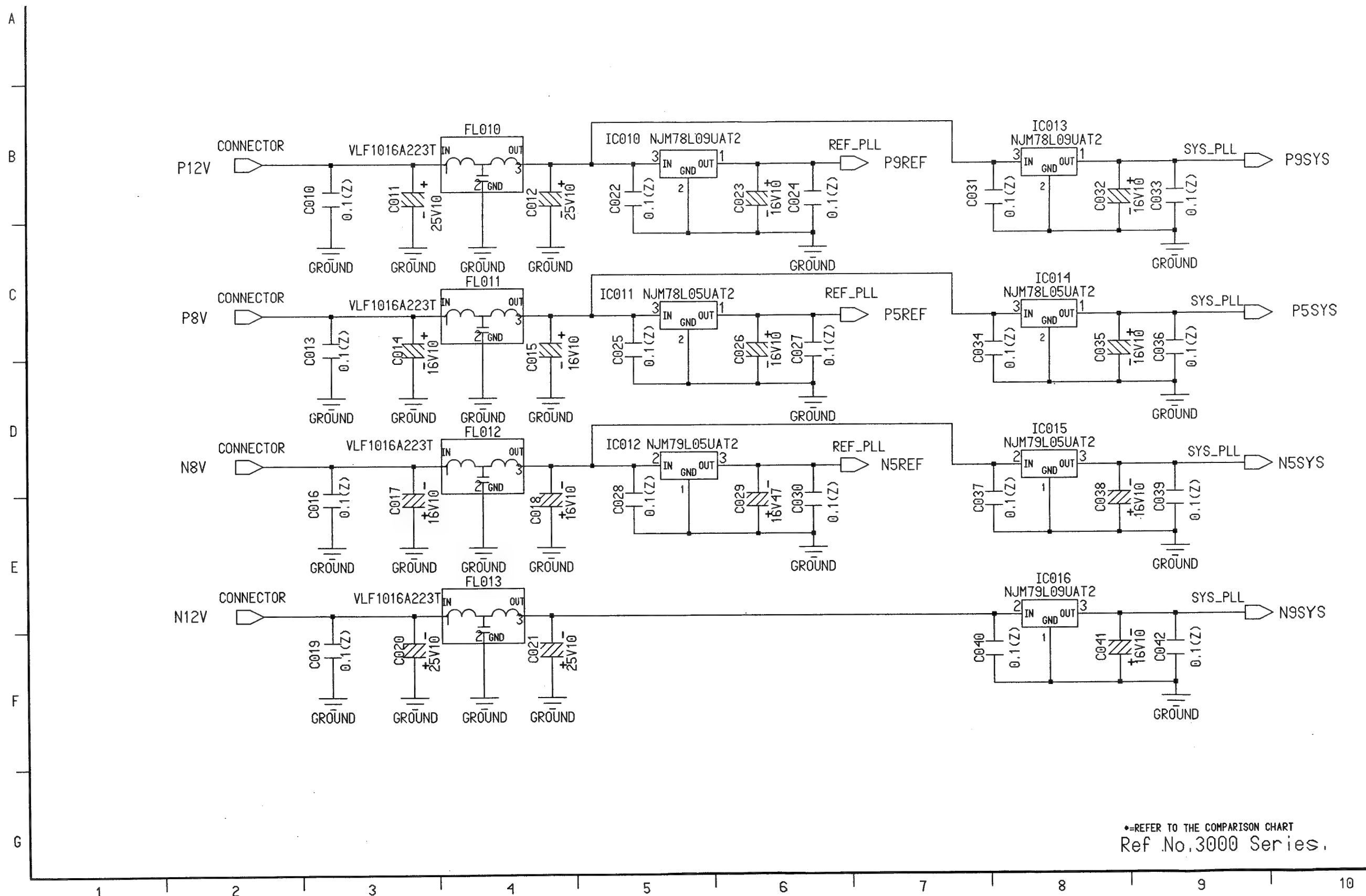
V OUT (F4 3/30) OVERALL 2 SCHEMATIC DIAGRAM



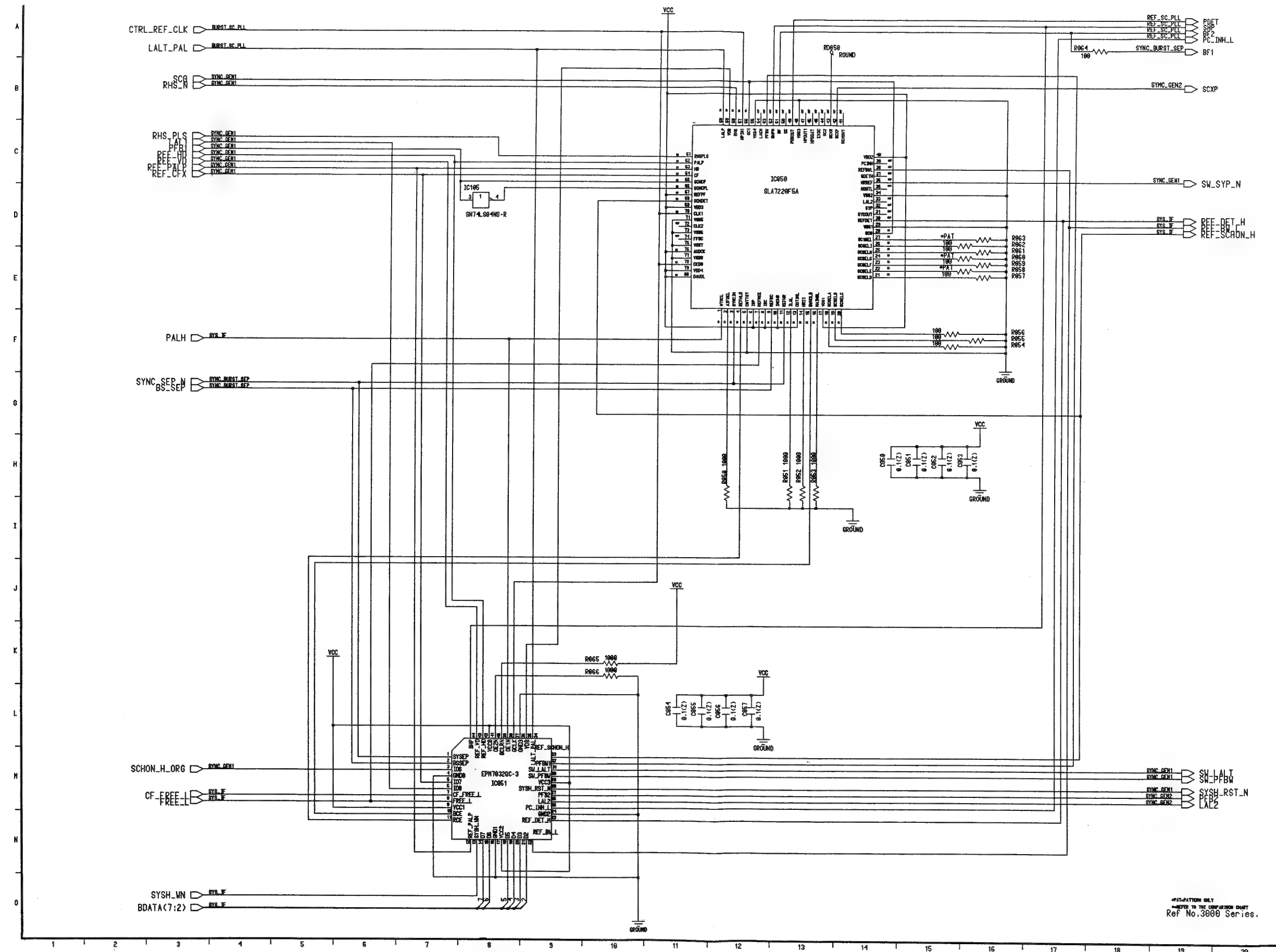
V OUT (F4 4/30) OVERALL 3 SCHEMATIC DIAGRAM



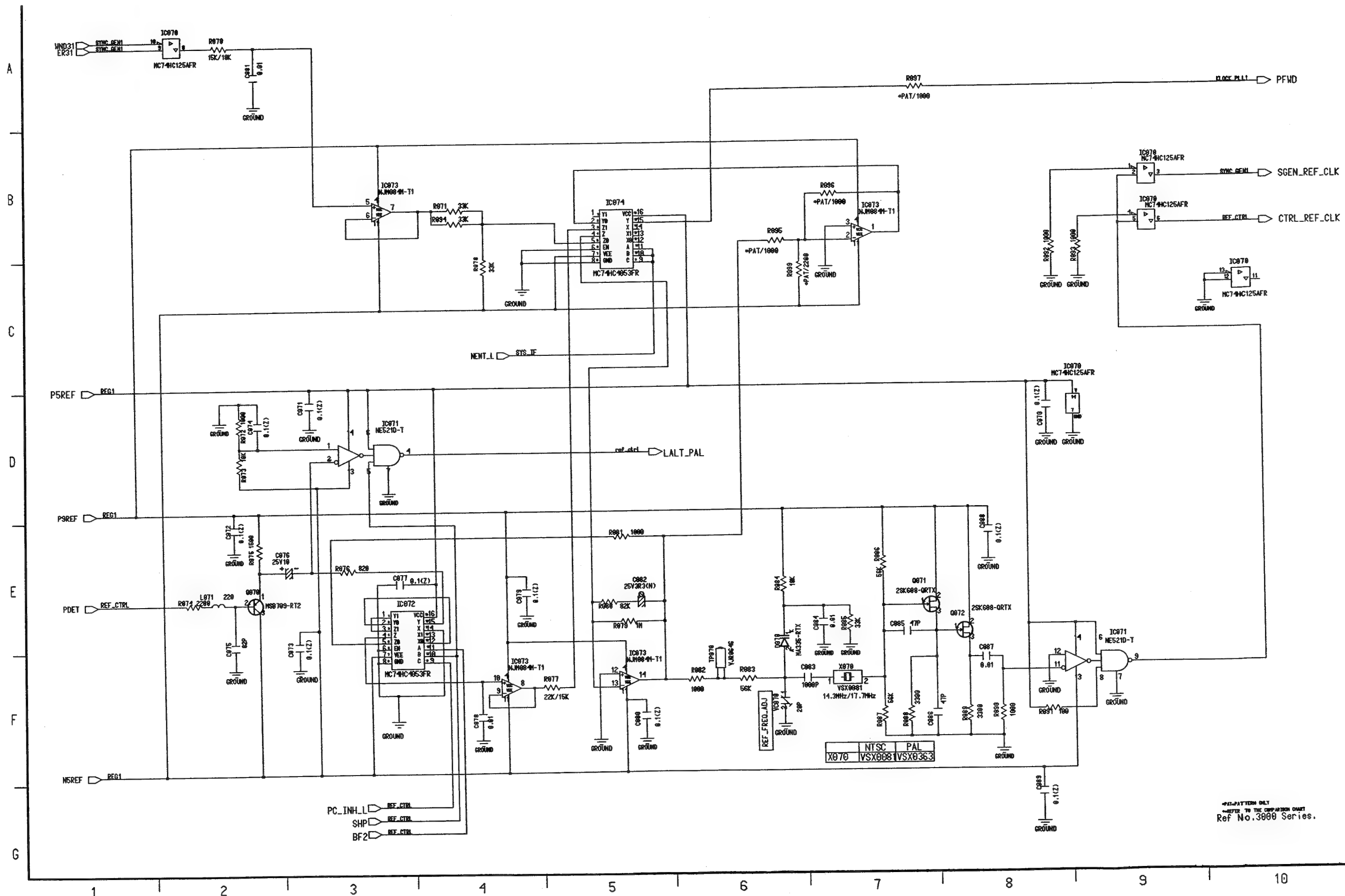
V OUT (F4 5/30) REG 1 SCHEMATIC DIAGRAM



V OUT (F4 6/30) REF CTRL SCHEMATIC DIAGRAM



V OUT (F4 7/30) REF SC PLL SCHEMATIC DIAGRAM



A



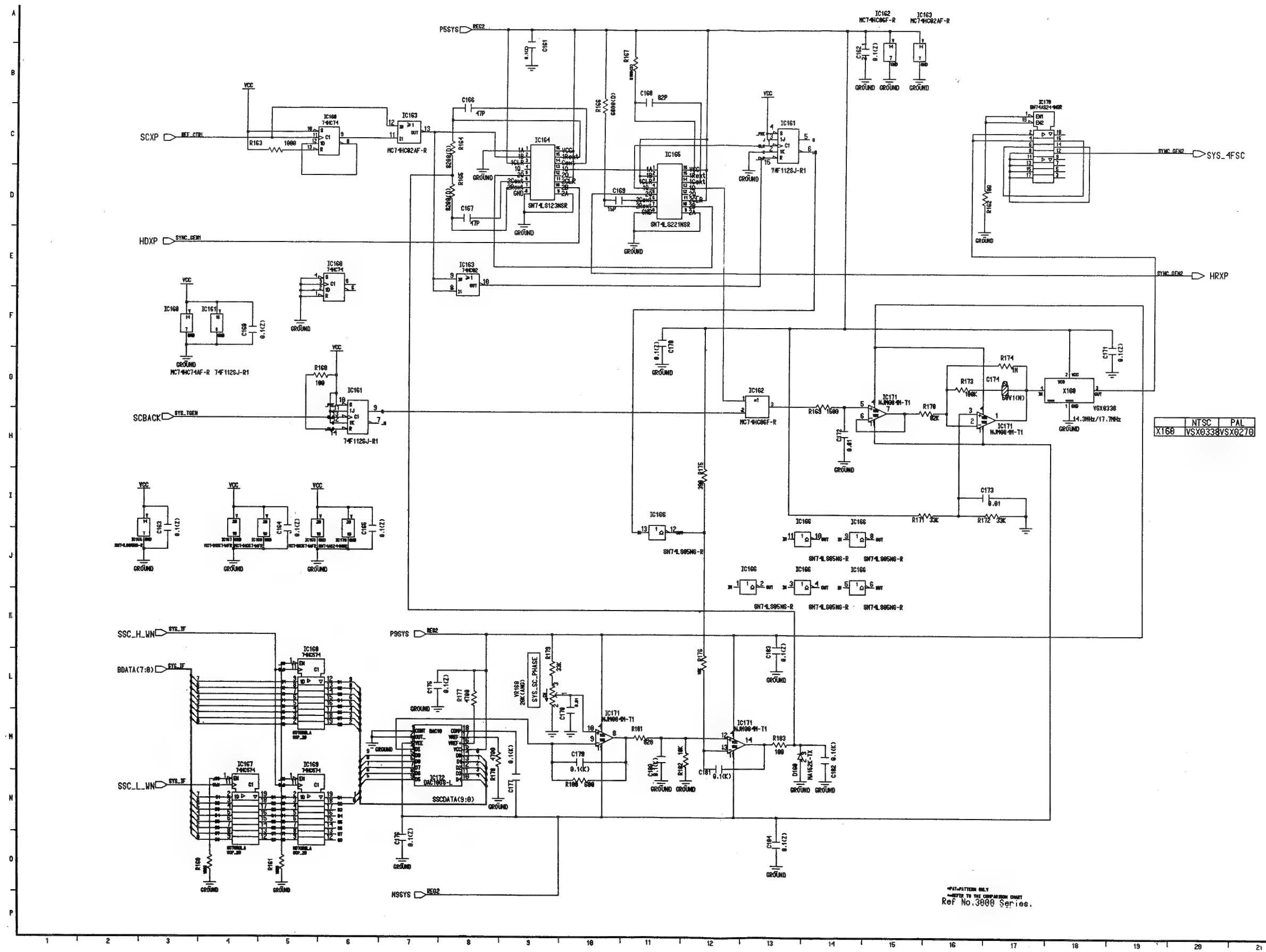
C

D

F

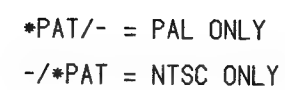
F

V OUT (F4 10/30) SYS SC PLL SCHEMATIC DIAGRAM

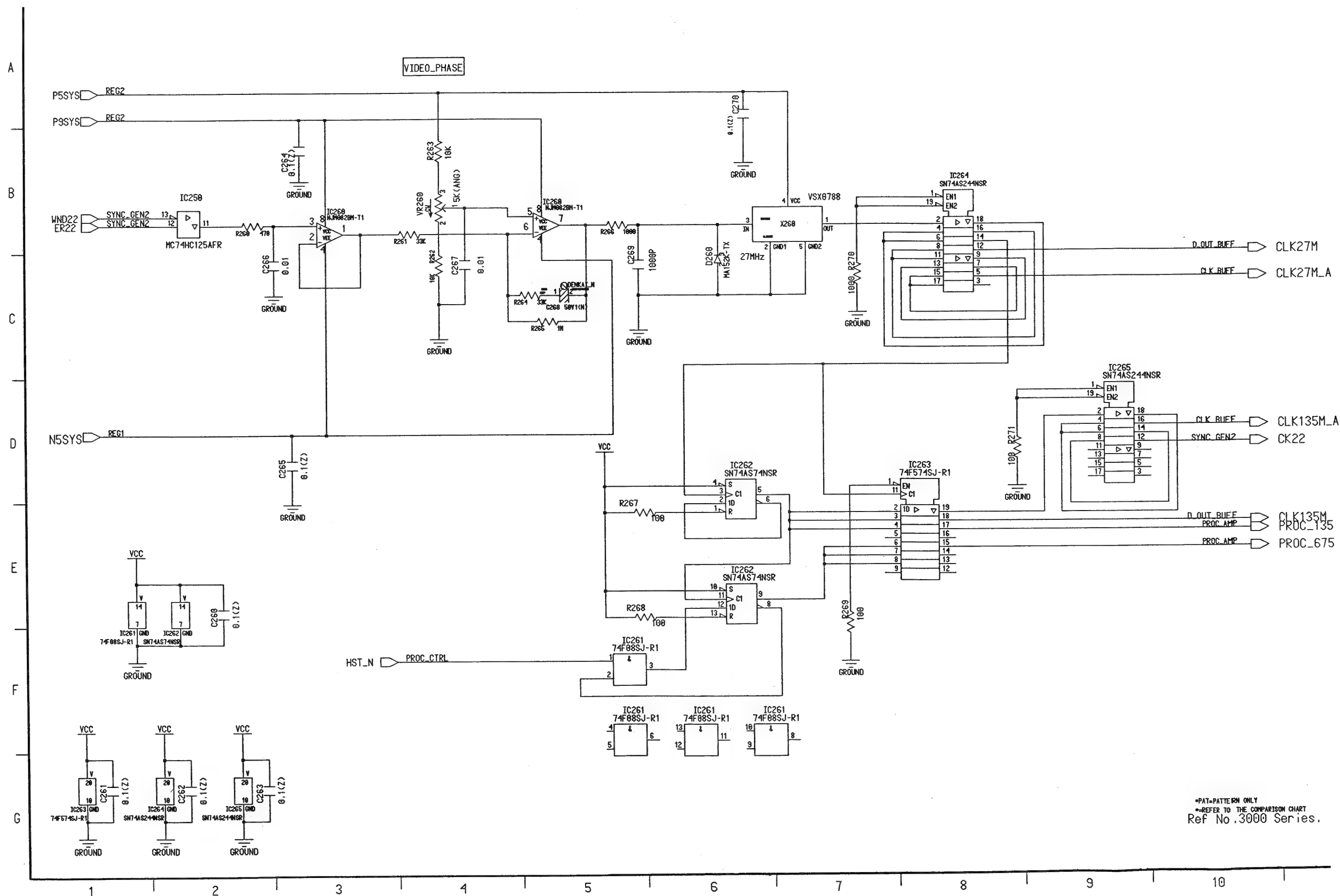


*PATTERN ONLY
REFER TO THE COMPARISON CHART
Ref No.3000 Series.

A vertical scale with labels A, B, C, D, E, F, G, H, and T from top to bottom. The scale is represented by a vertical line with horizontal tick marks corresponding to each label.

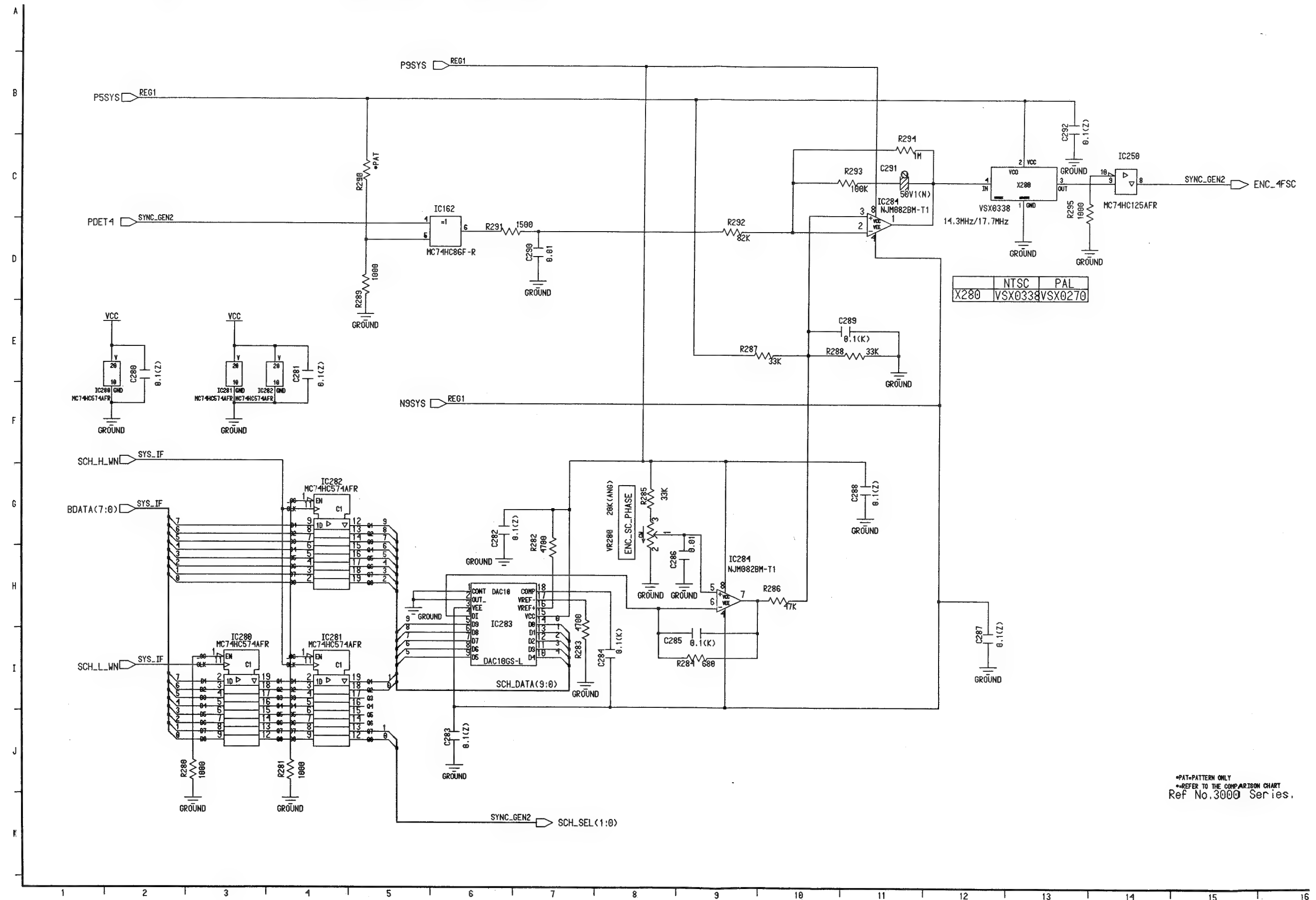


V OUT (F4 13/30) H LOCK PLL 3 SCHEMATIC DIAGRAM



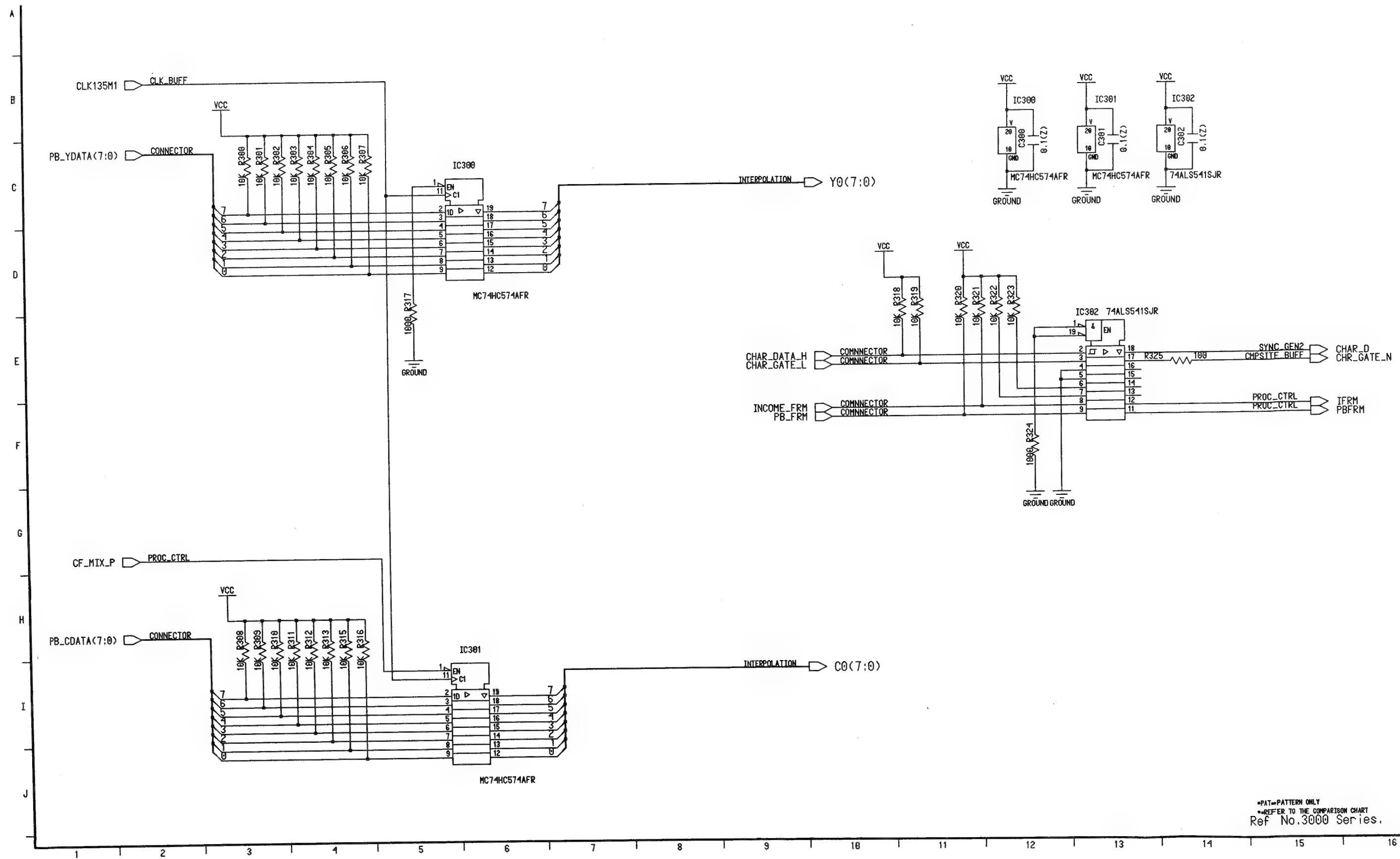
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•REFER TO THE COMPARISON CHART
Ref No.3000 Series.

V OUT (F4 14/30) ENC SC PLL SCHEMATIC DIAGRAM

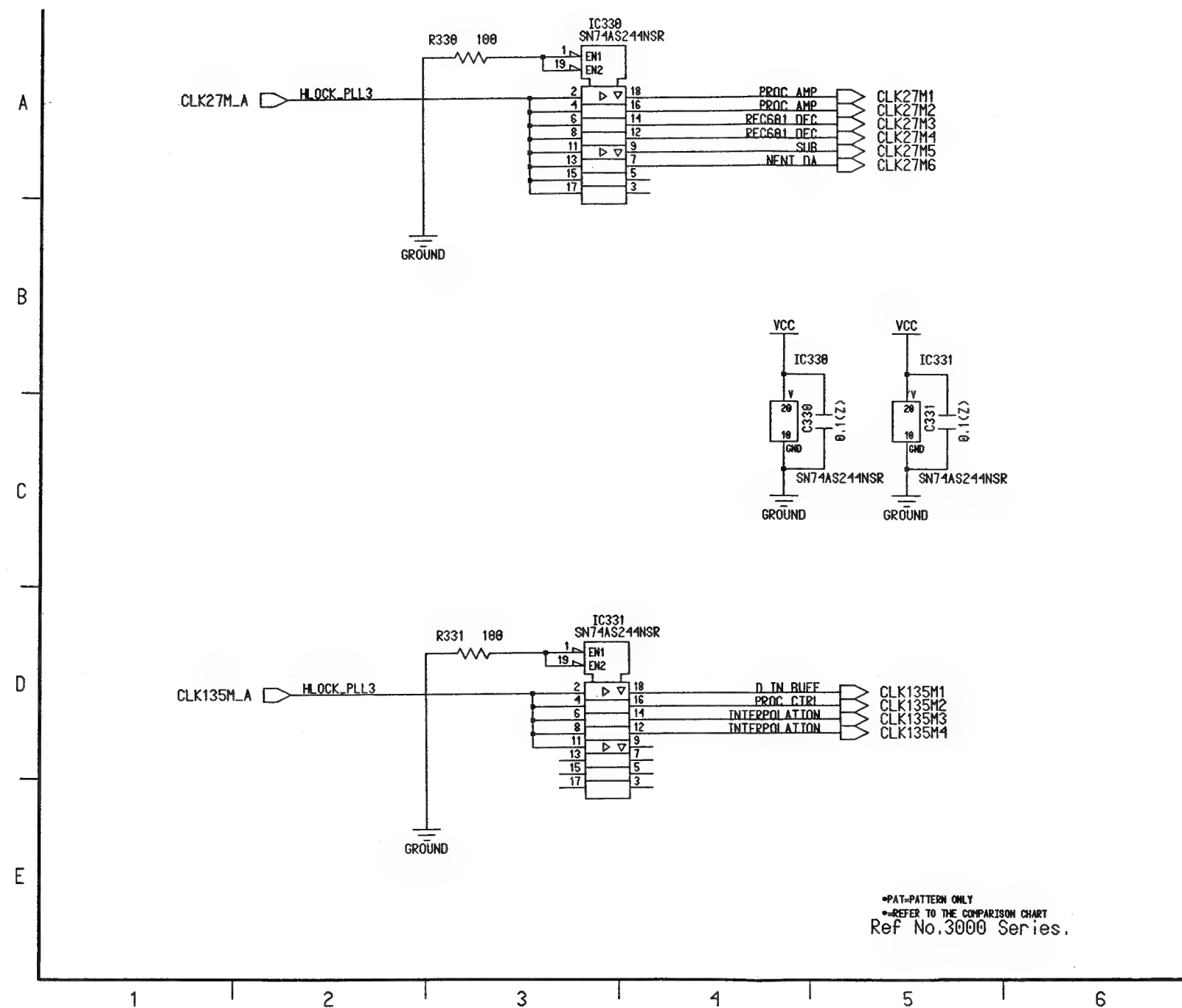


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*REFER TO THE COMPARISON CHART
Ref No.3000 Series.

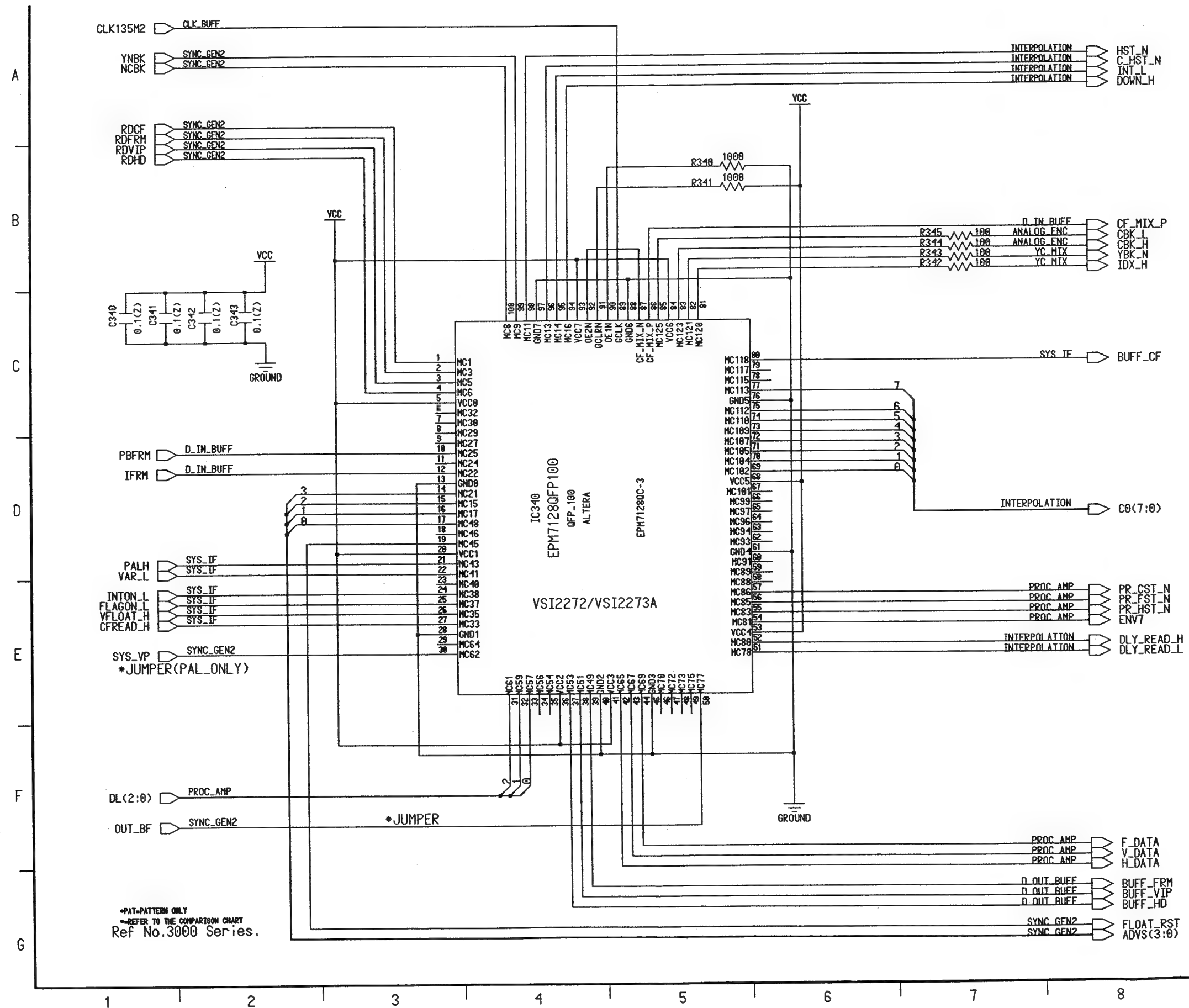
V OUT (F4 15/30) D IN BUFF SCHEMATIC DIAGRAM



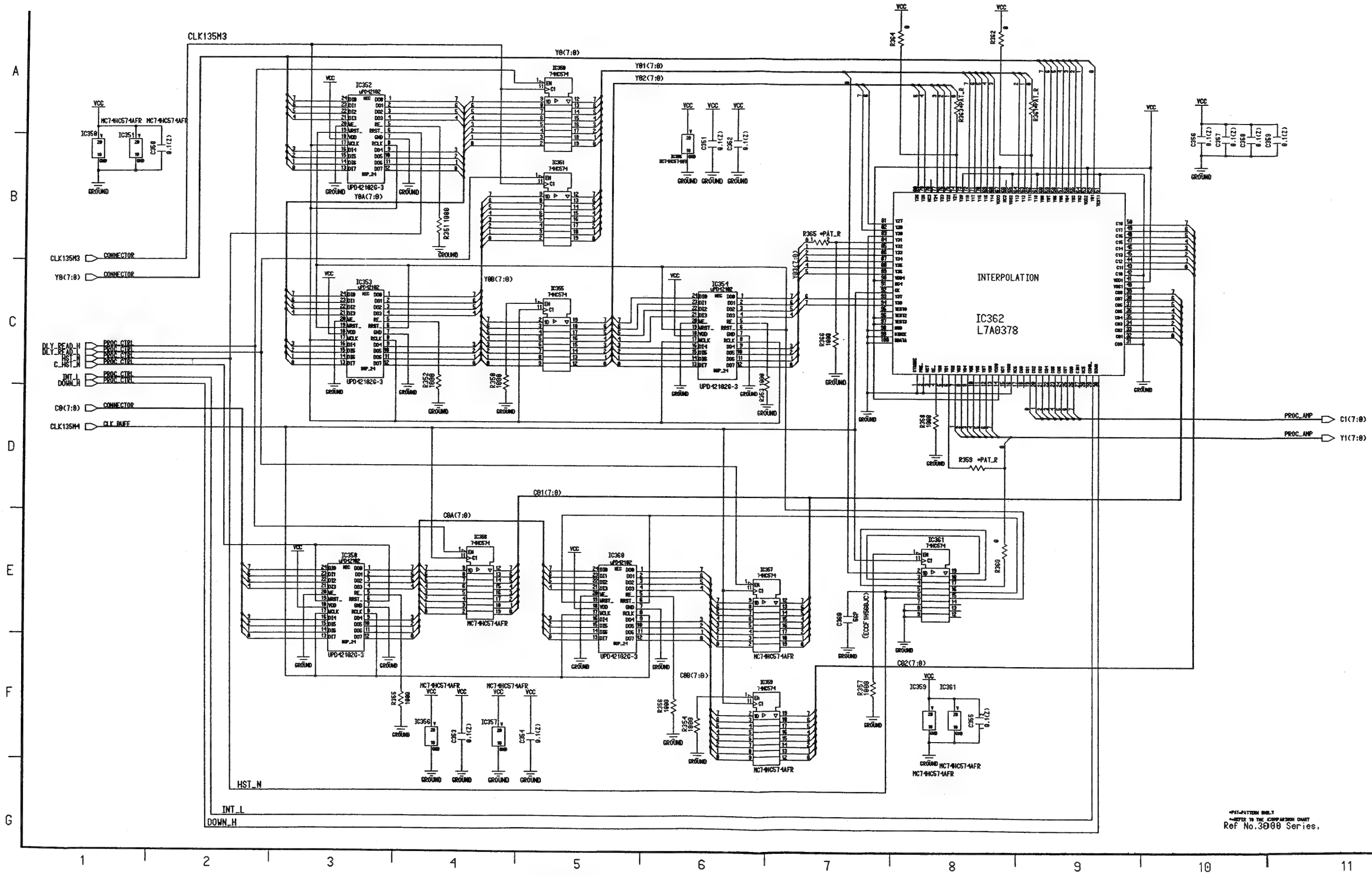
V OUT (F4 16/30) CLK BUFF SCHEMATIC DIAGRAM



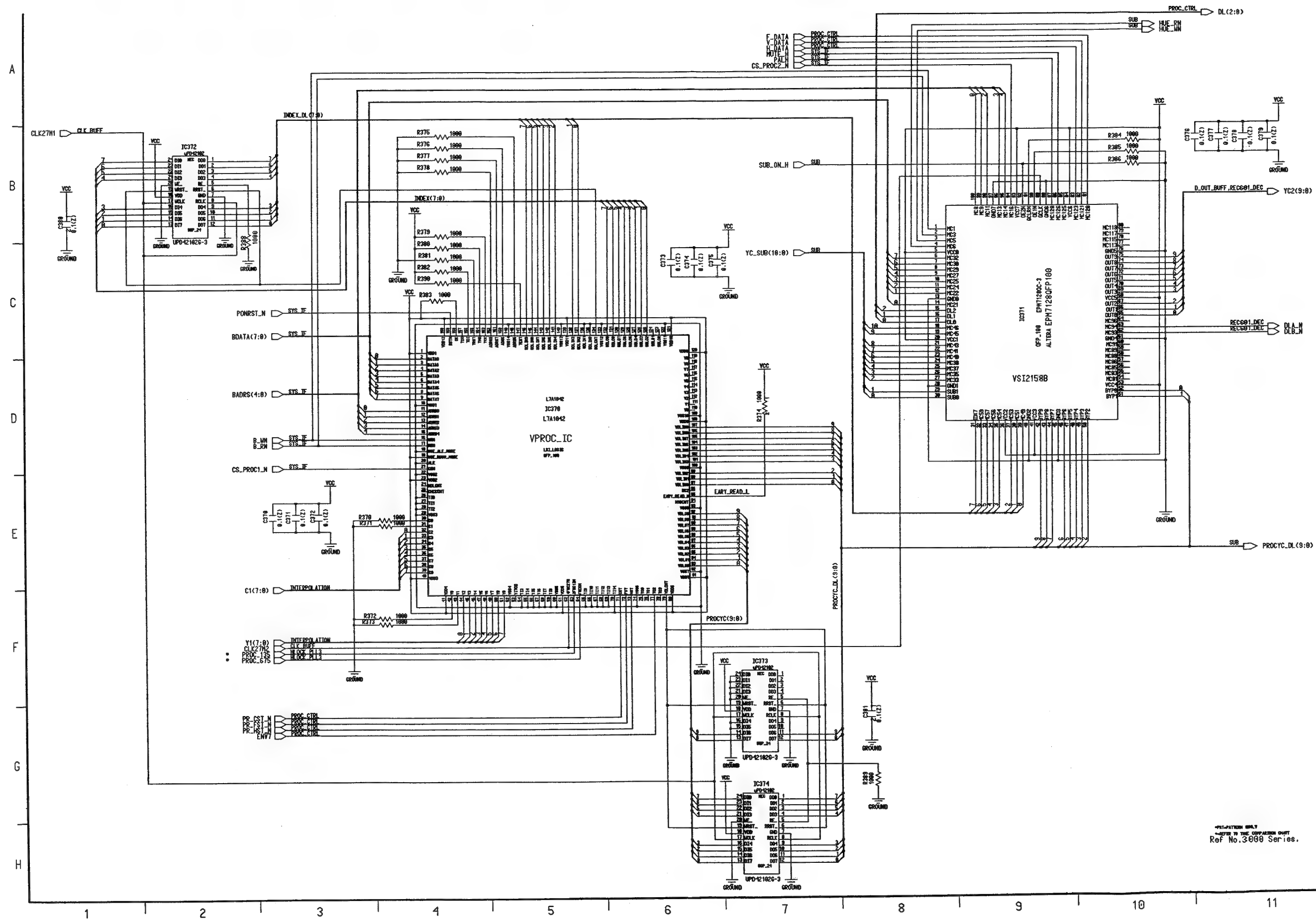
V OUT (F4 17/30) PROC CTRL SCHEMATIC DIAGRAM



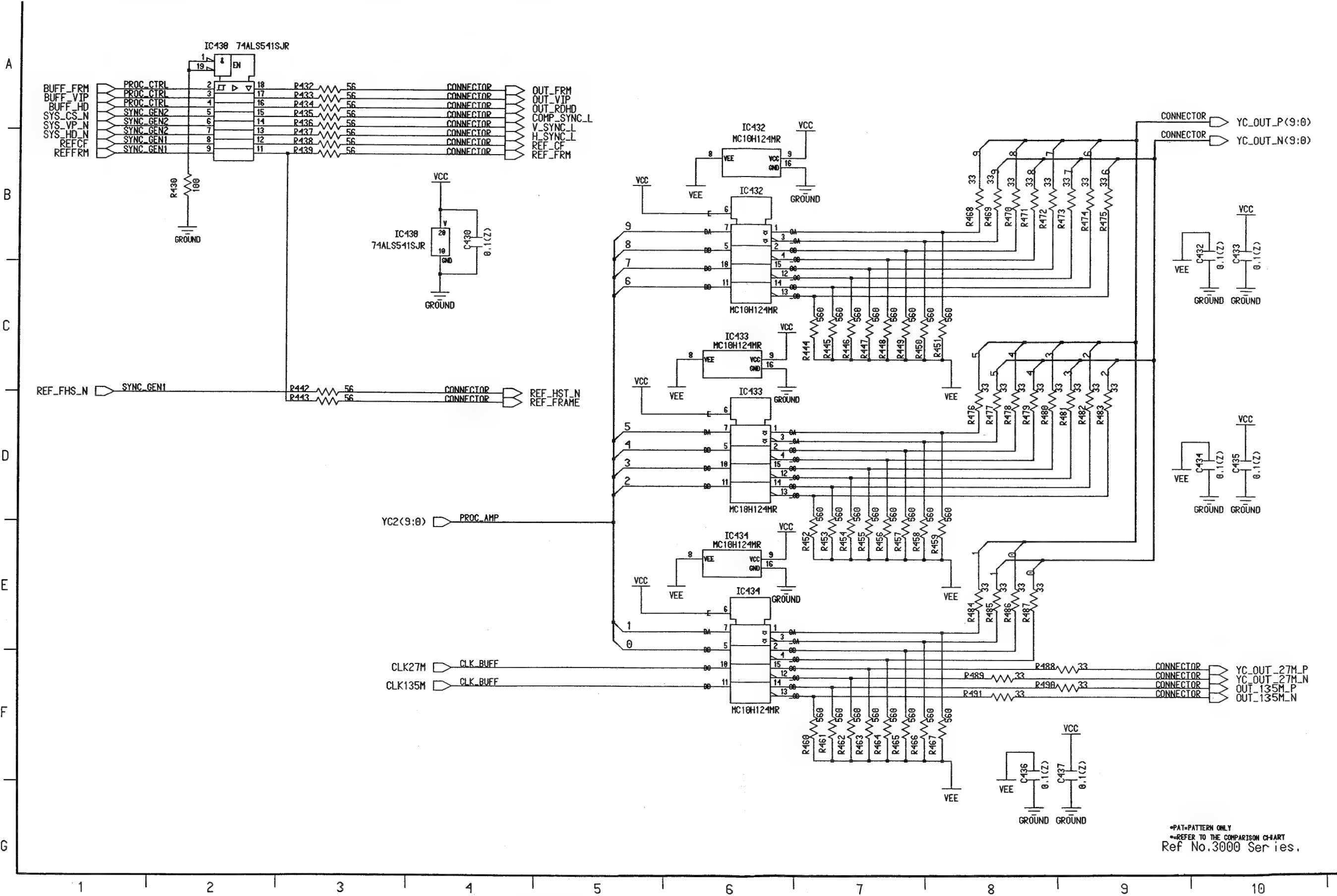
V OUT (F4 18/30) INTERPOLATION SCHEMATIC DIAGRAM



V OUT (F4 19/30) PROC AMP SCHEMATIC DIAGRAM

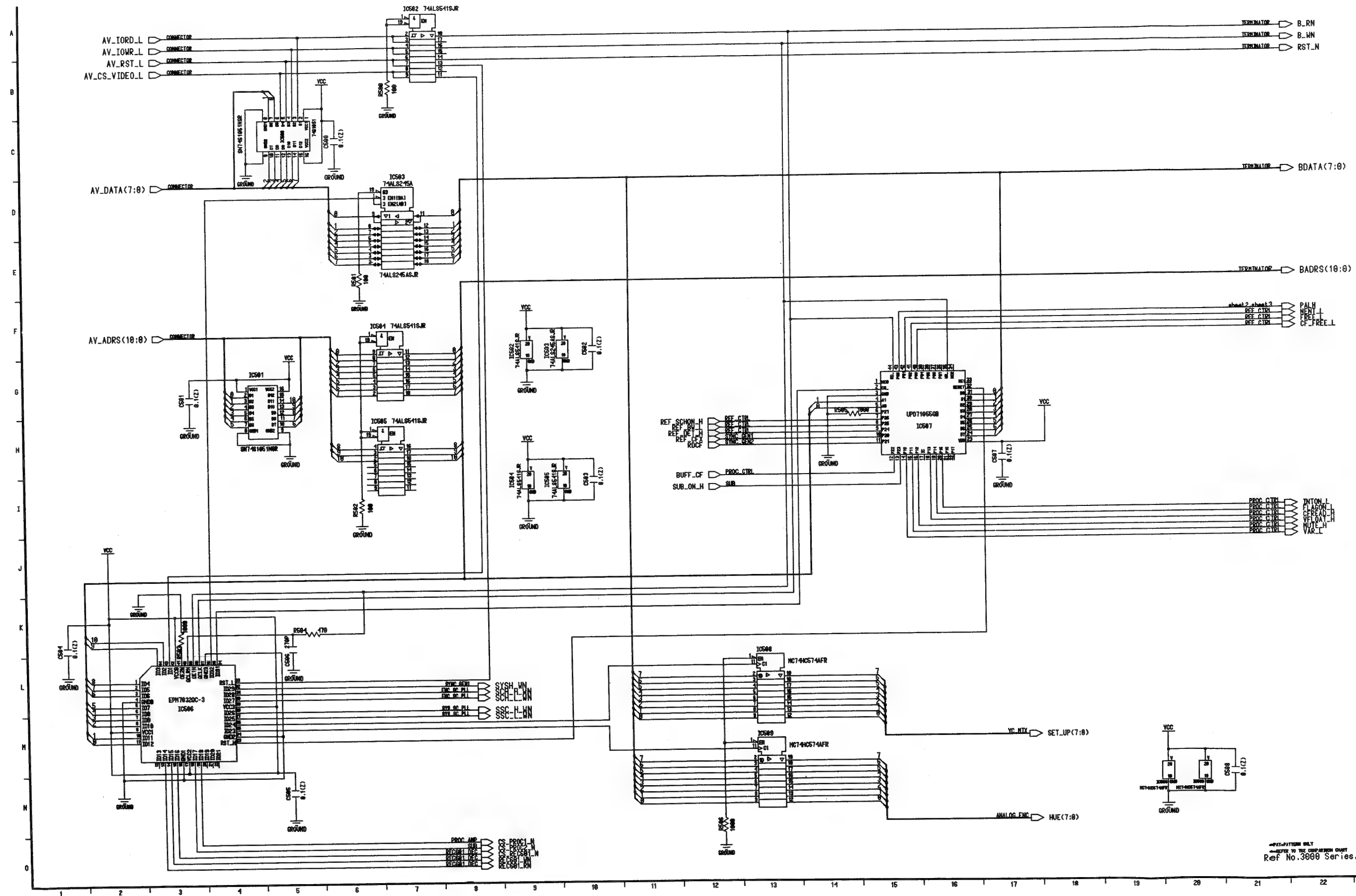


V OUT (F4 20/30) D OUT BUFF SCHEMATIC DIAGRAM

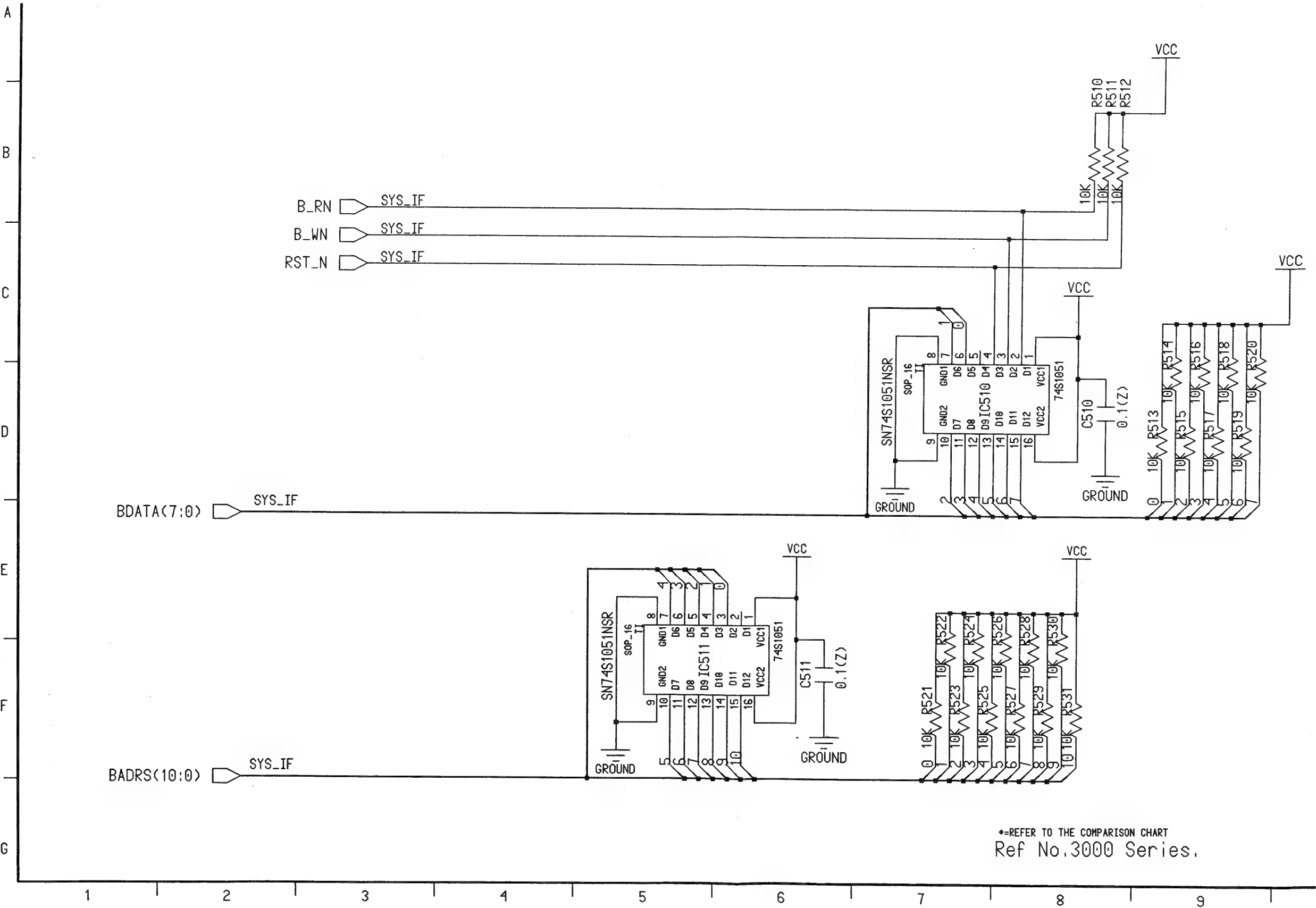


*PAT-PATTERN ONLY
*REFER TO THE COMPARISON CHART
Ref No.3000 Series.

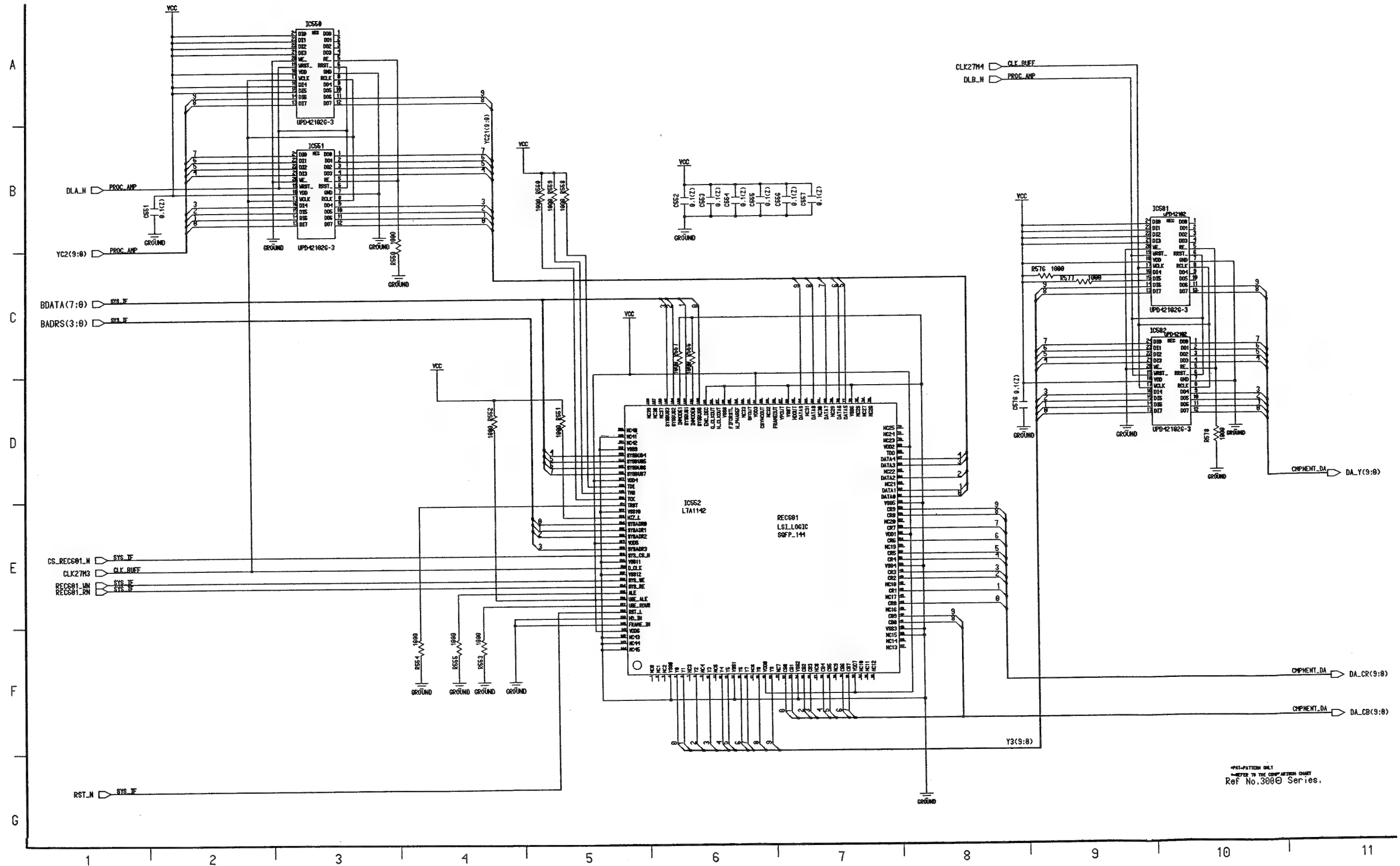
V OUT (F4 21/30) SYS IF SCHEMATIC DIAGRAM



V OUT (F4 22/30) TERMINATOR SCHEMATIC DIAGRAM

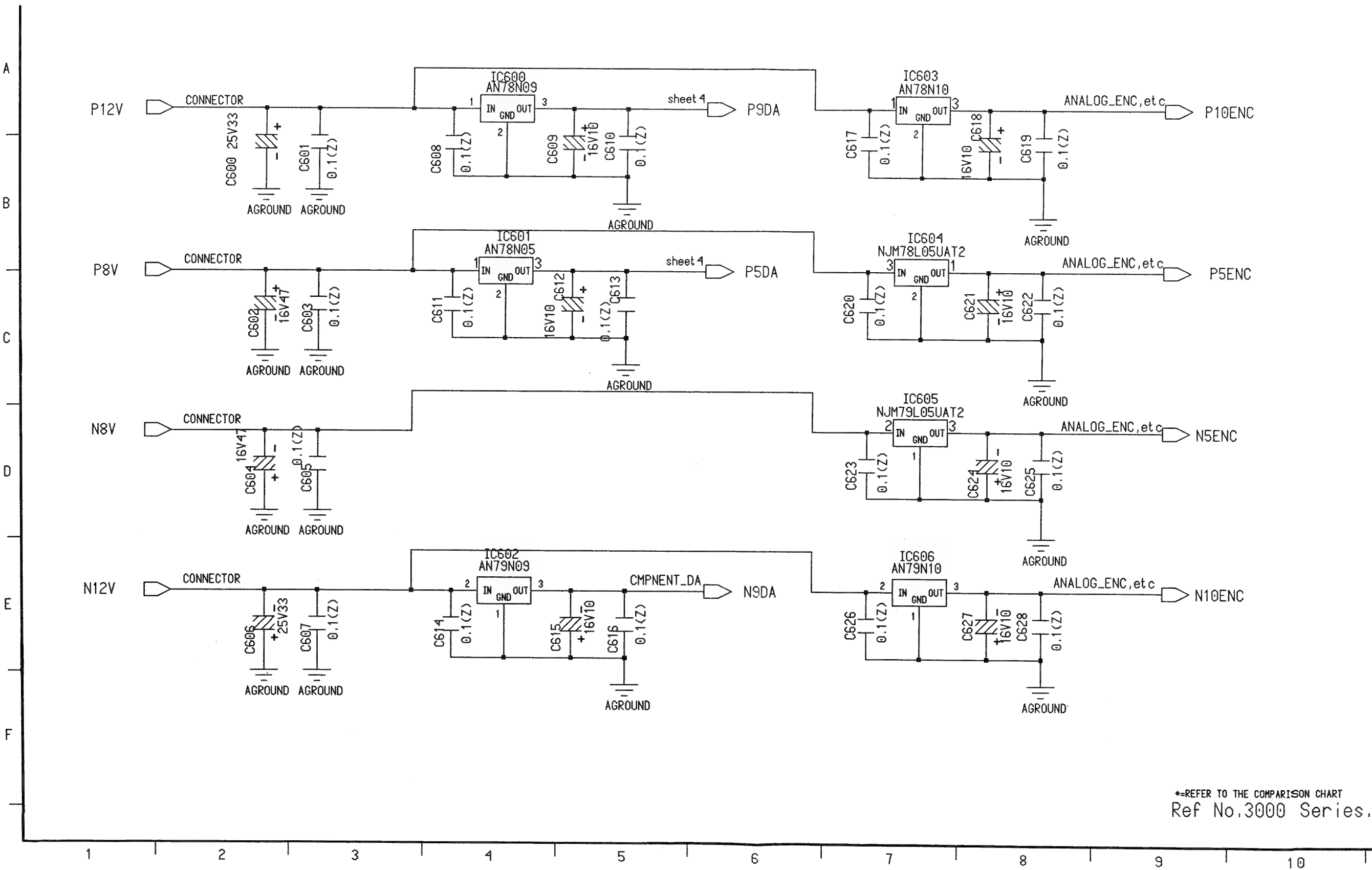


V OUT (F4 23/30) REC601 DEC SCHEMATIC DIAGRAM

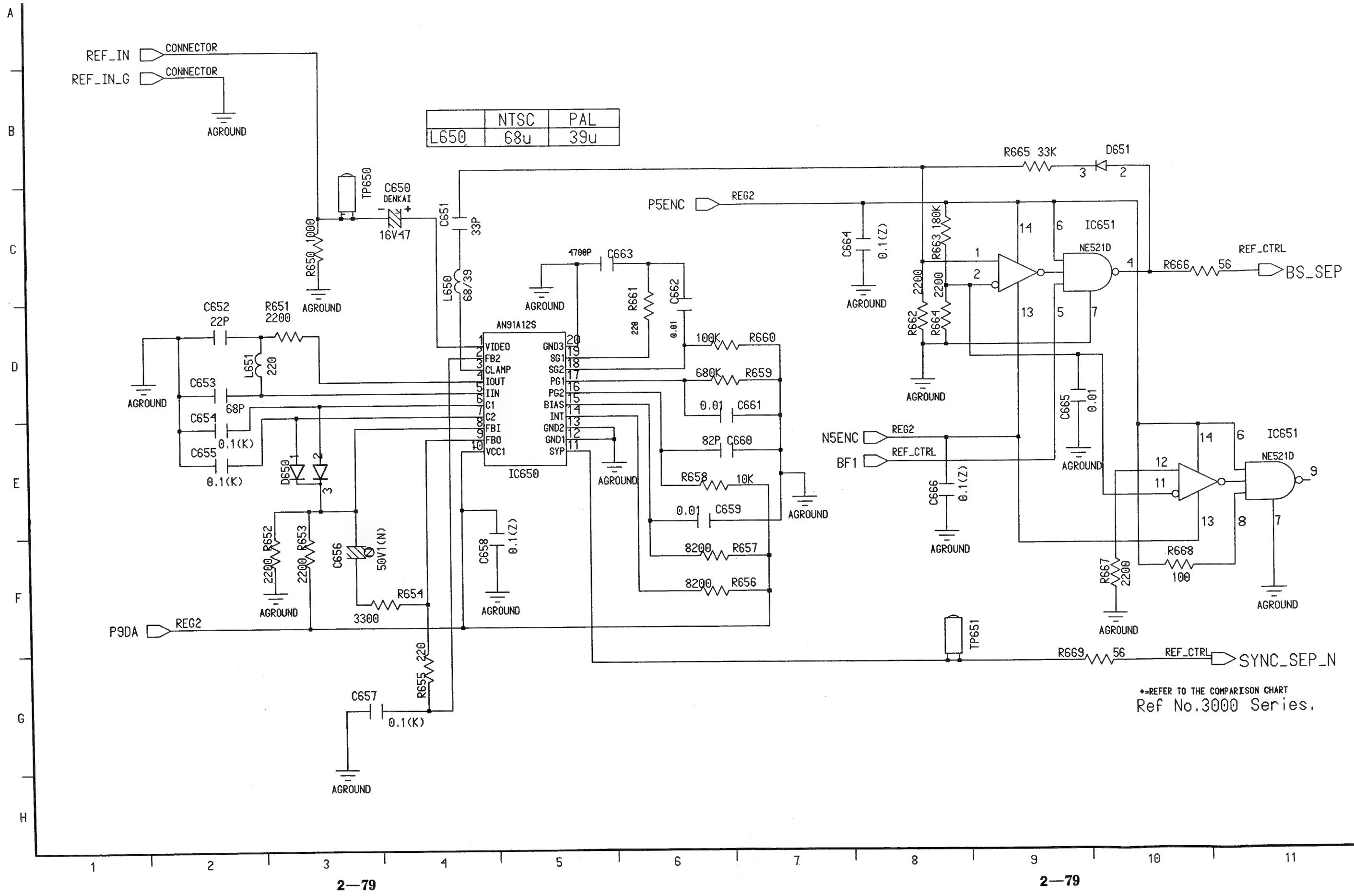


NOT-PATTERN ONLY
 REFER TO THE COMPARTMENT CHART
 Ref No.3000 Series.

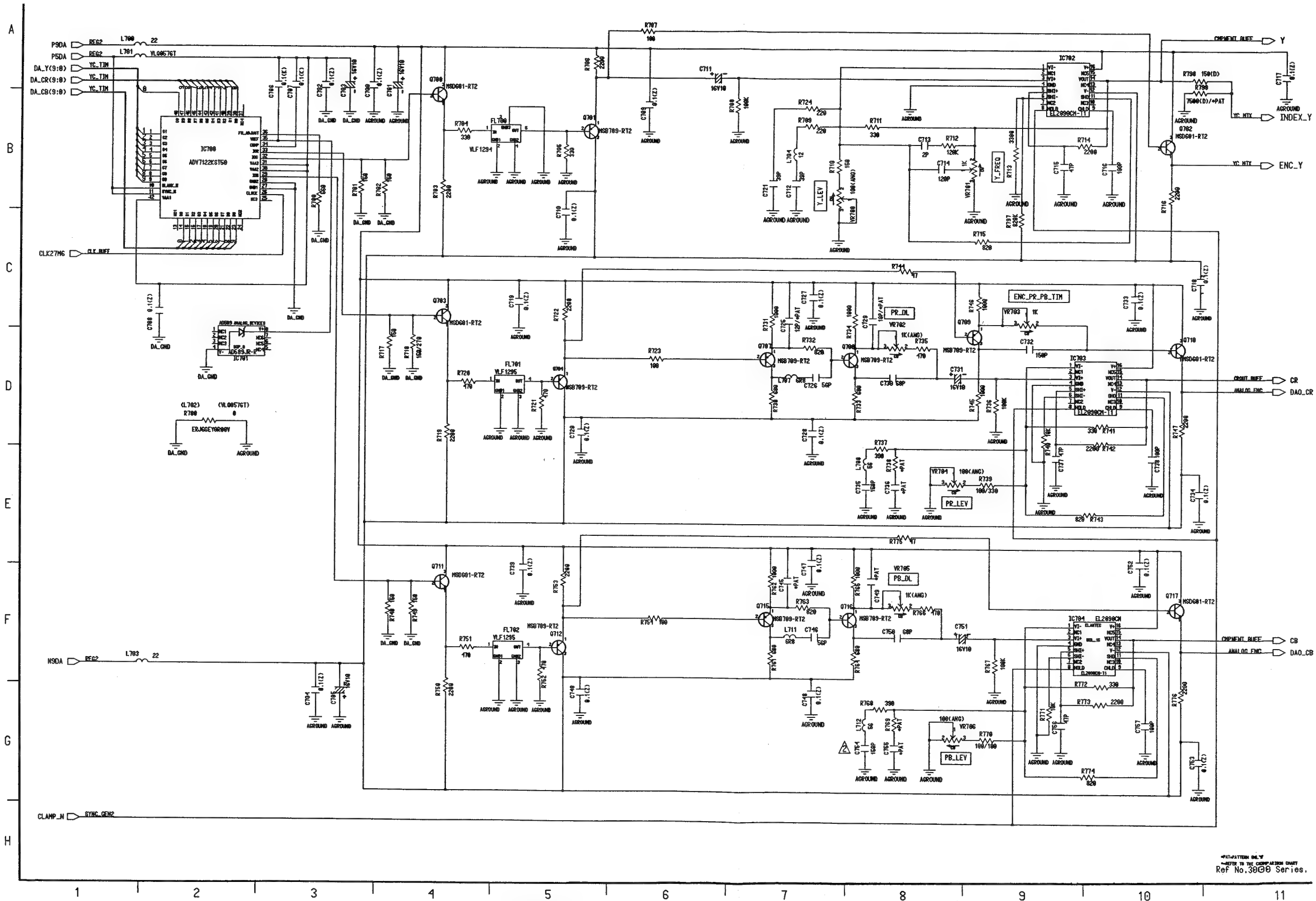
V OUT (F4 24/30) REG 2 SCHEMATIC DIAGRAM



V OUT (F4 25/30) SYNC BURST SEP SCHEMATIC DIAGRAM

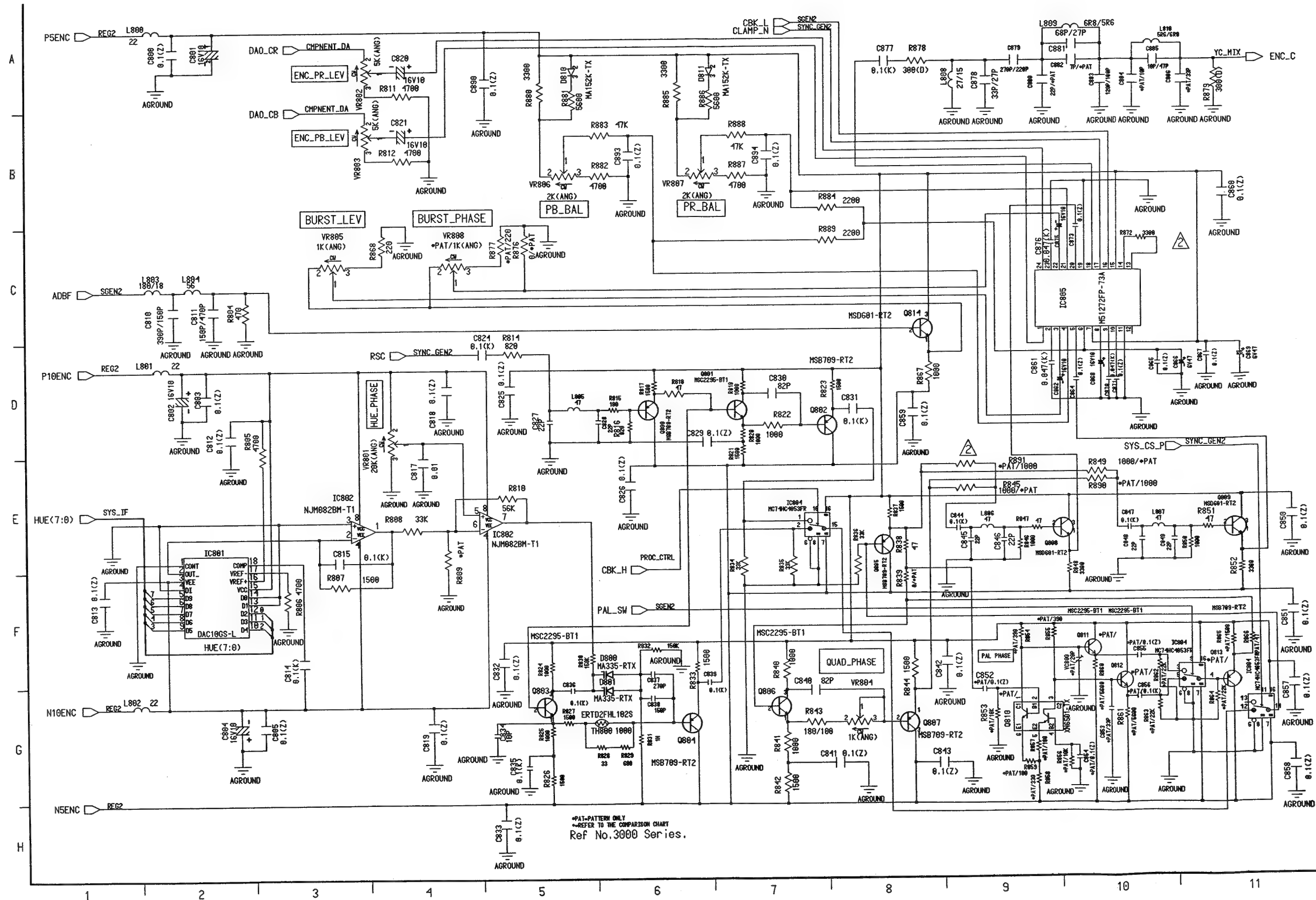


V OUT (F4 26/30) CMPNENT DA SCHEMATIC DIAGRAM

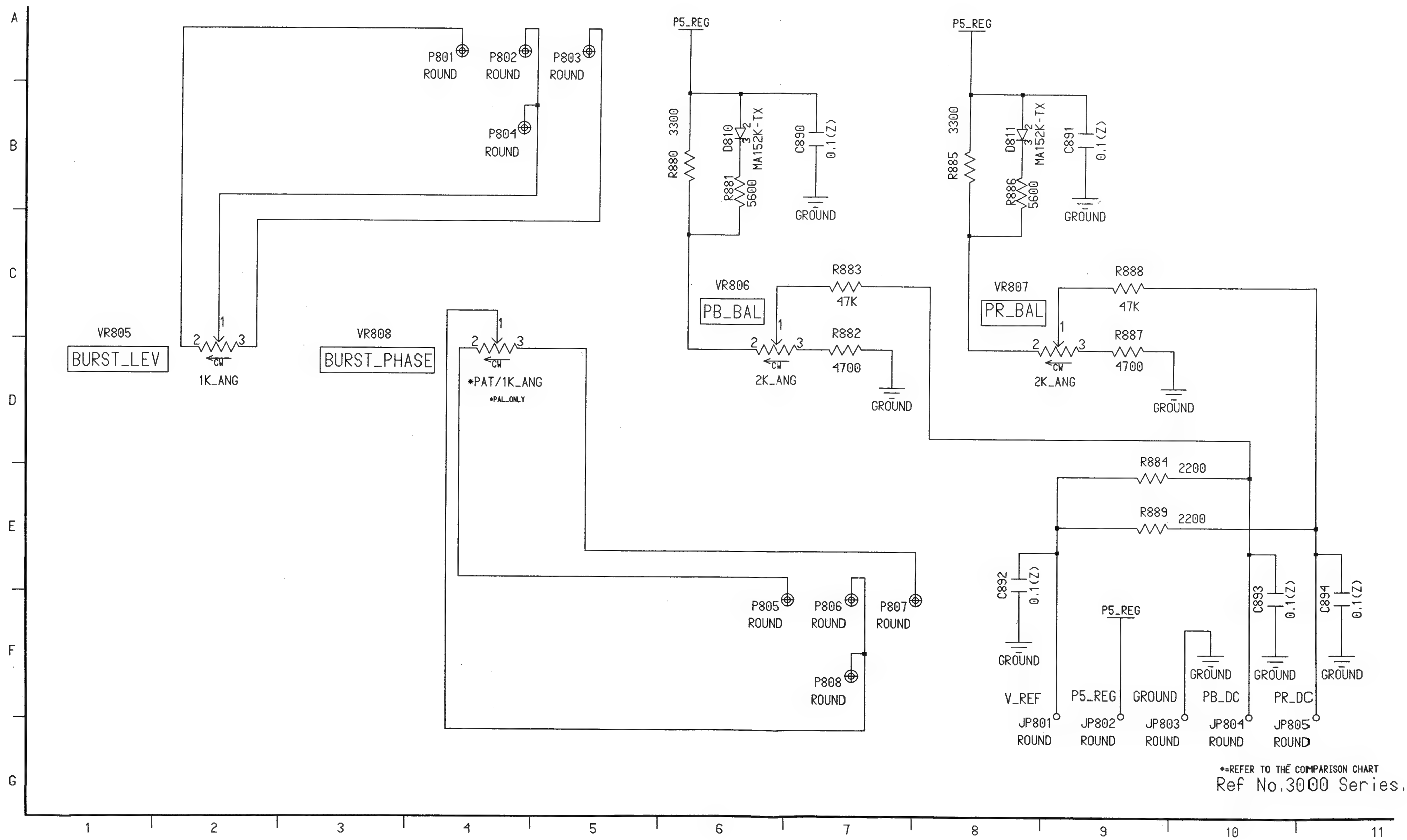


4-01-PATTERN 04.10
-REFER TO THE COMPARISON CHART
Ref No.3000 Series.

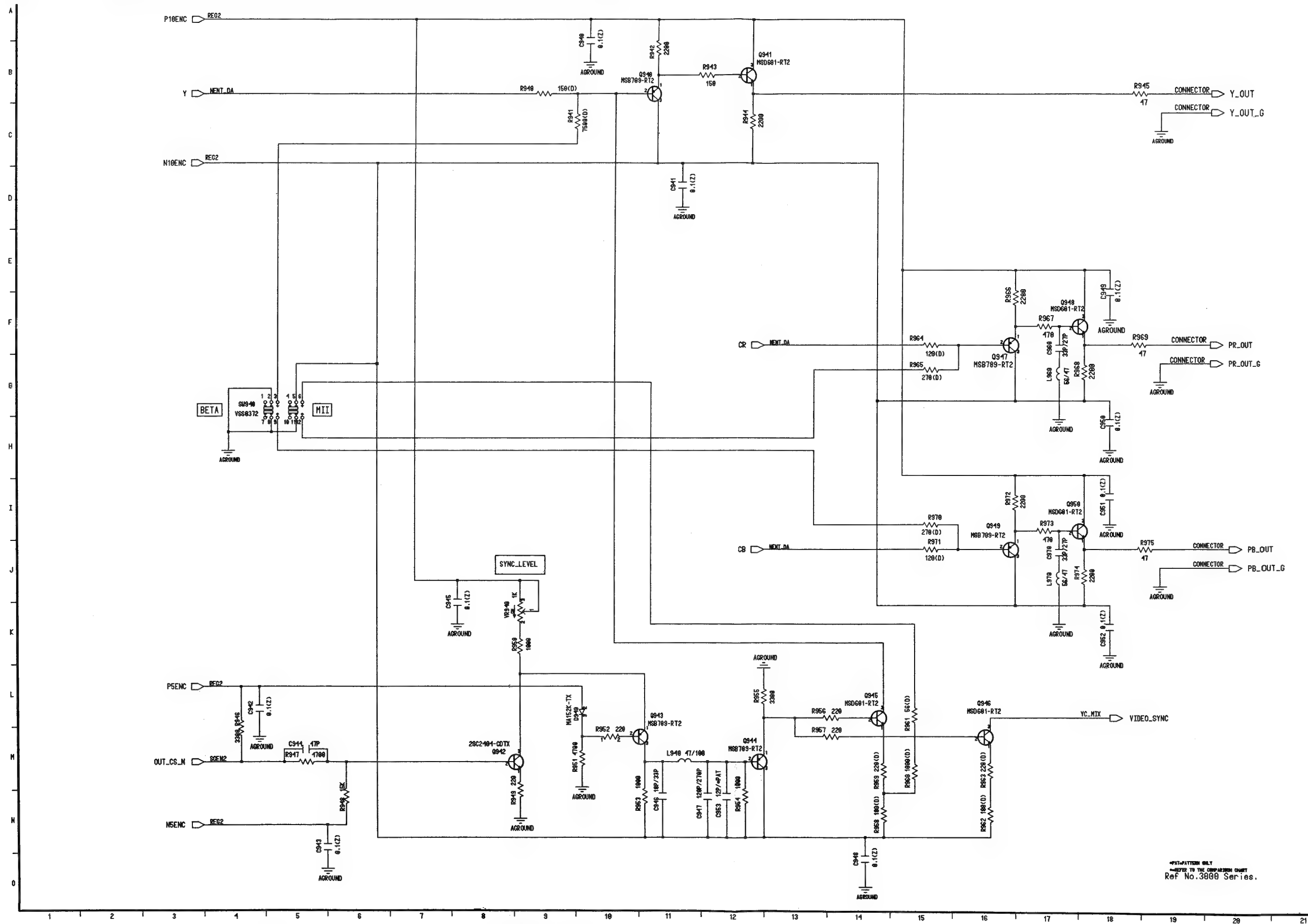
V OUT (F4 27/30) ANALOG ENC SCHEMATIC DIAGRAM



V OUT (F4 27B/30) VR SUB SCHEMATIC DIAGRAM

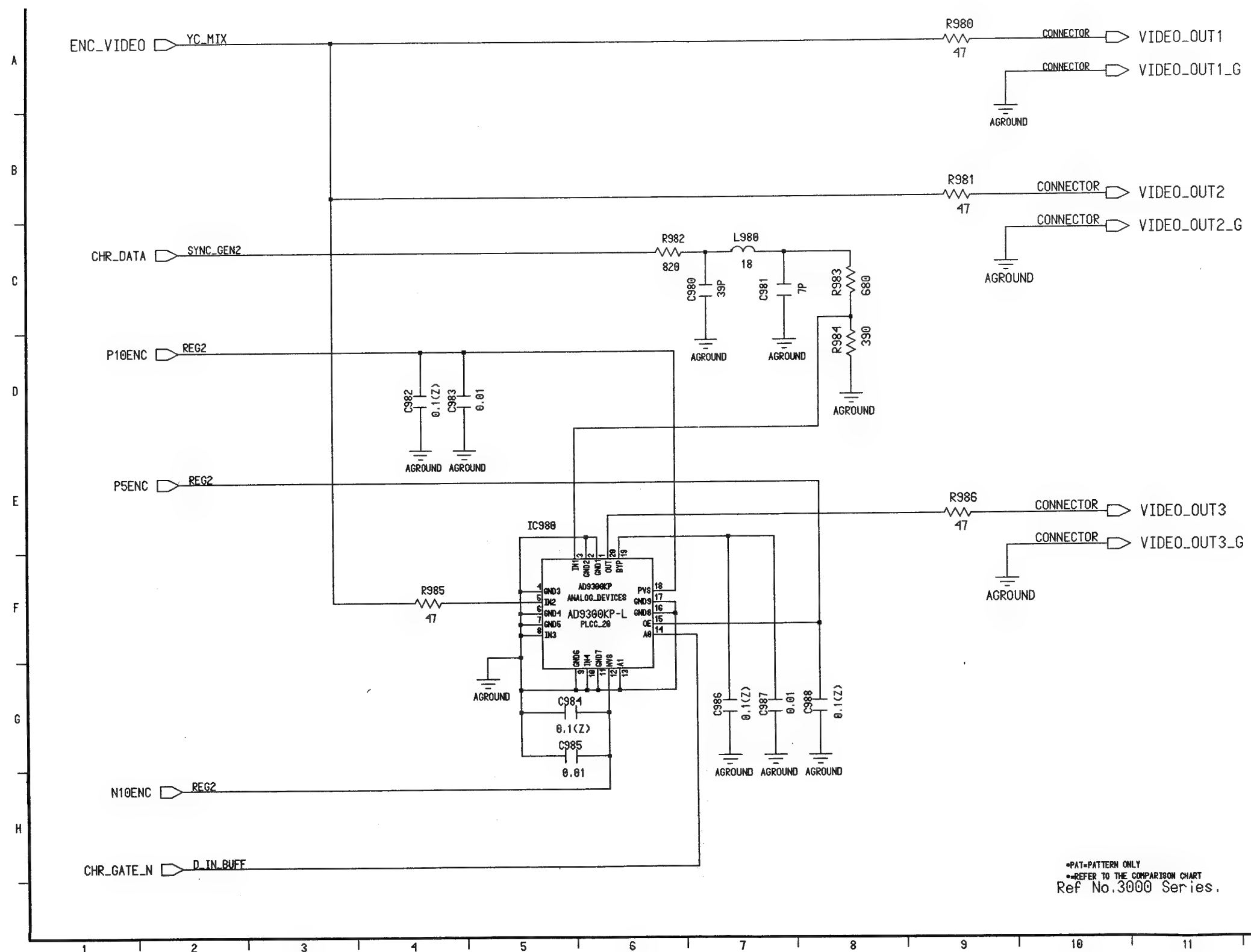


V OUT (F4 29/30) CMPNENT BUFF SCHEMATIC DIAGRAM

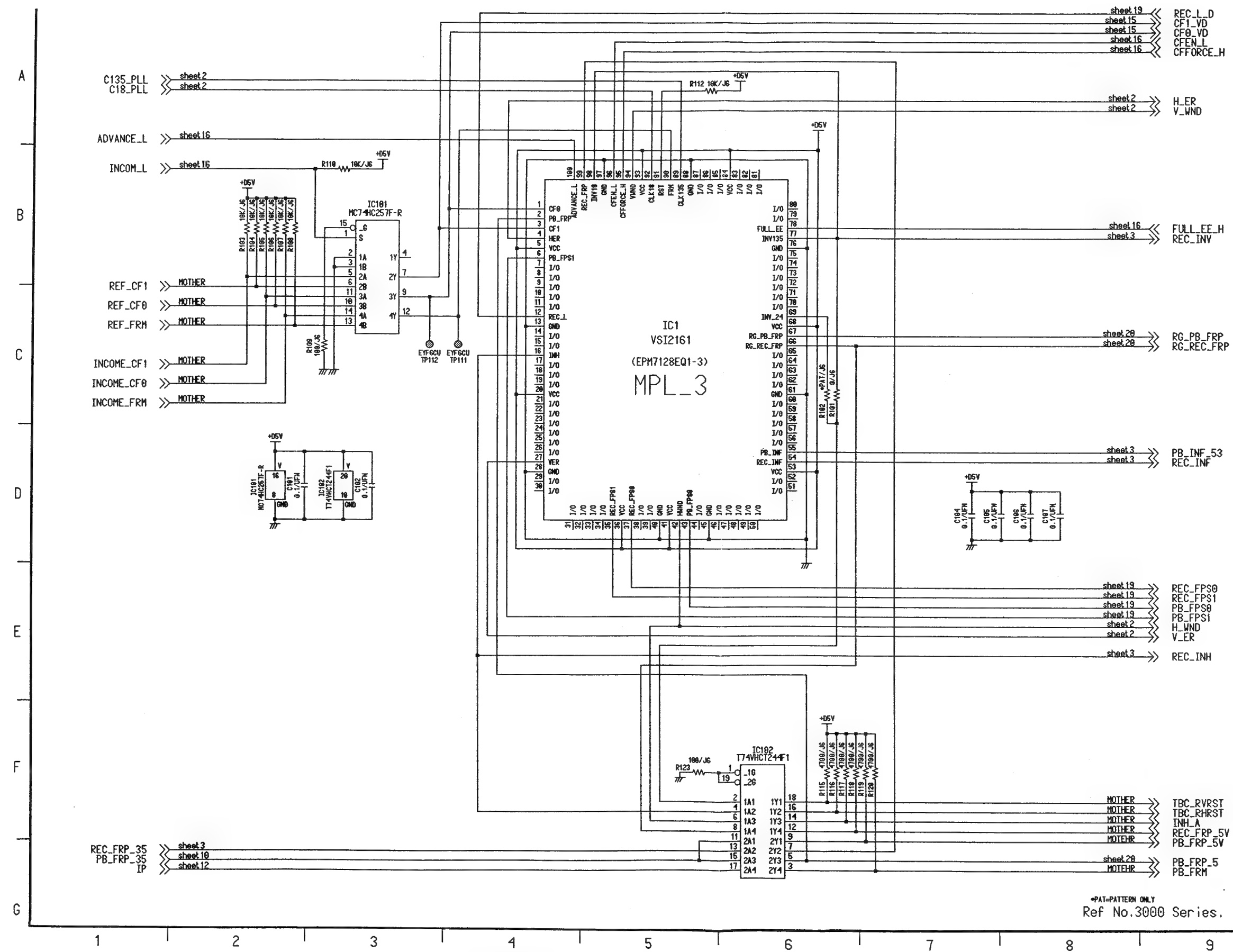


REF. NO. 3800 SERIES

V OUT (F4 30/30) CMPSITE BUFF SCHEMATIC DIAGRAM

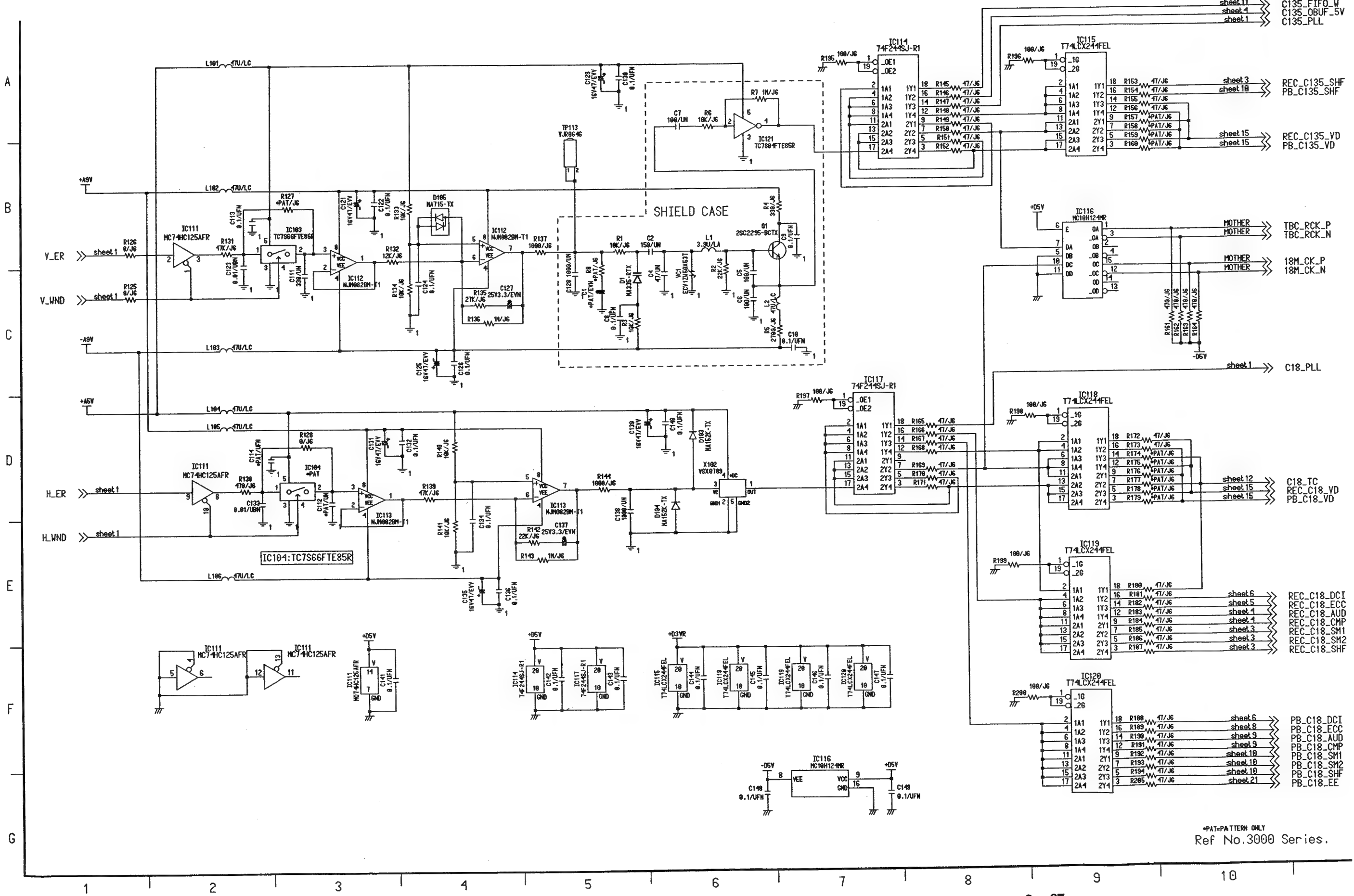


REC PB (F5 1/23) PLL 1 SCHEMATIC DIAGRAM

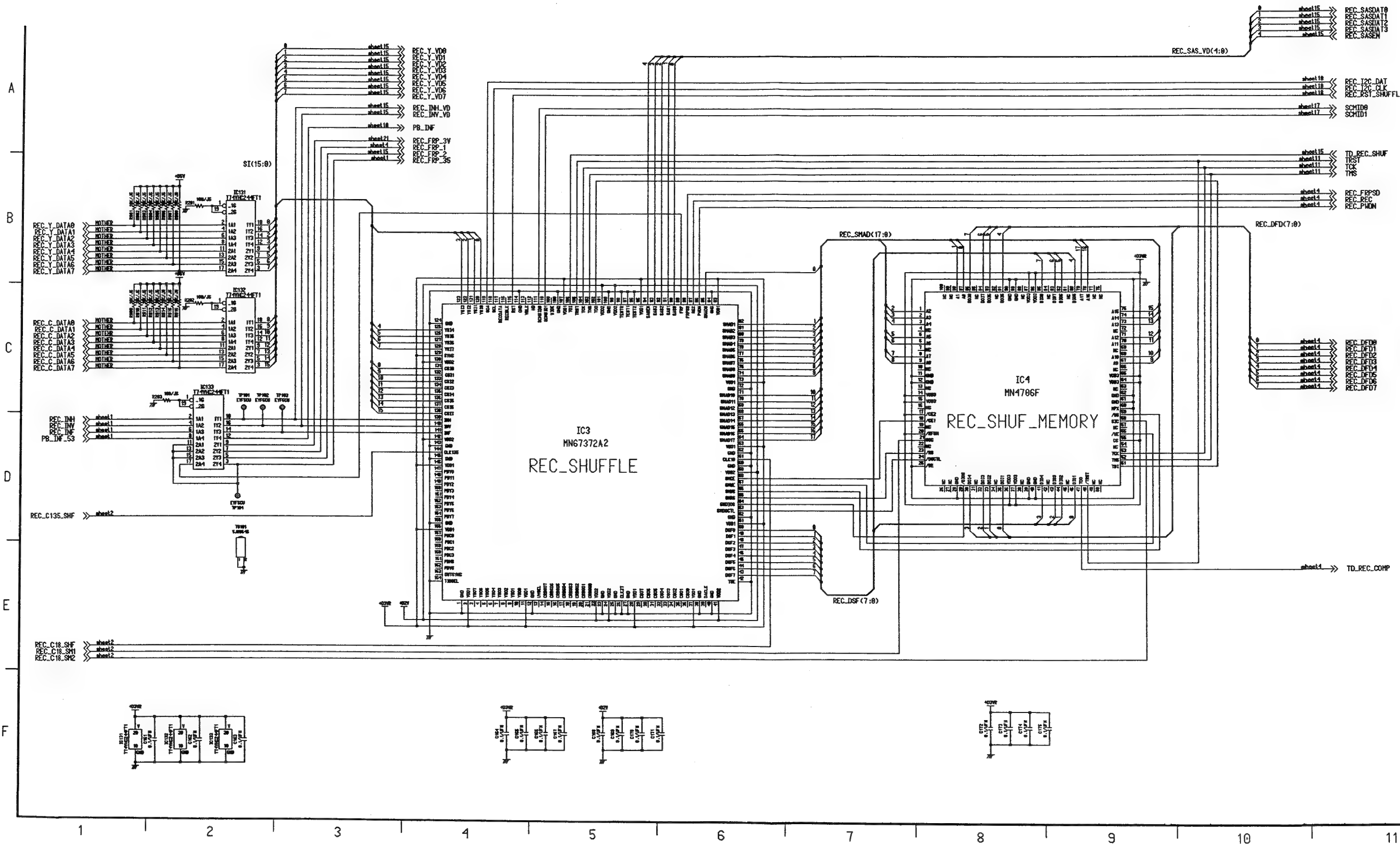


•PAT= PATTERN ONLY
Ref No.3000 Series.

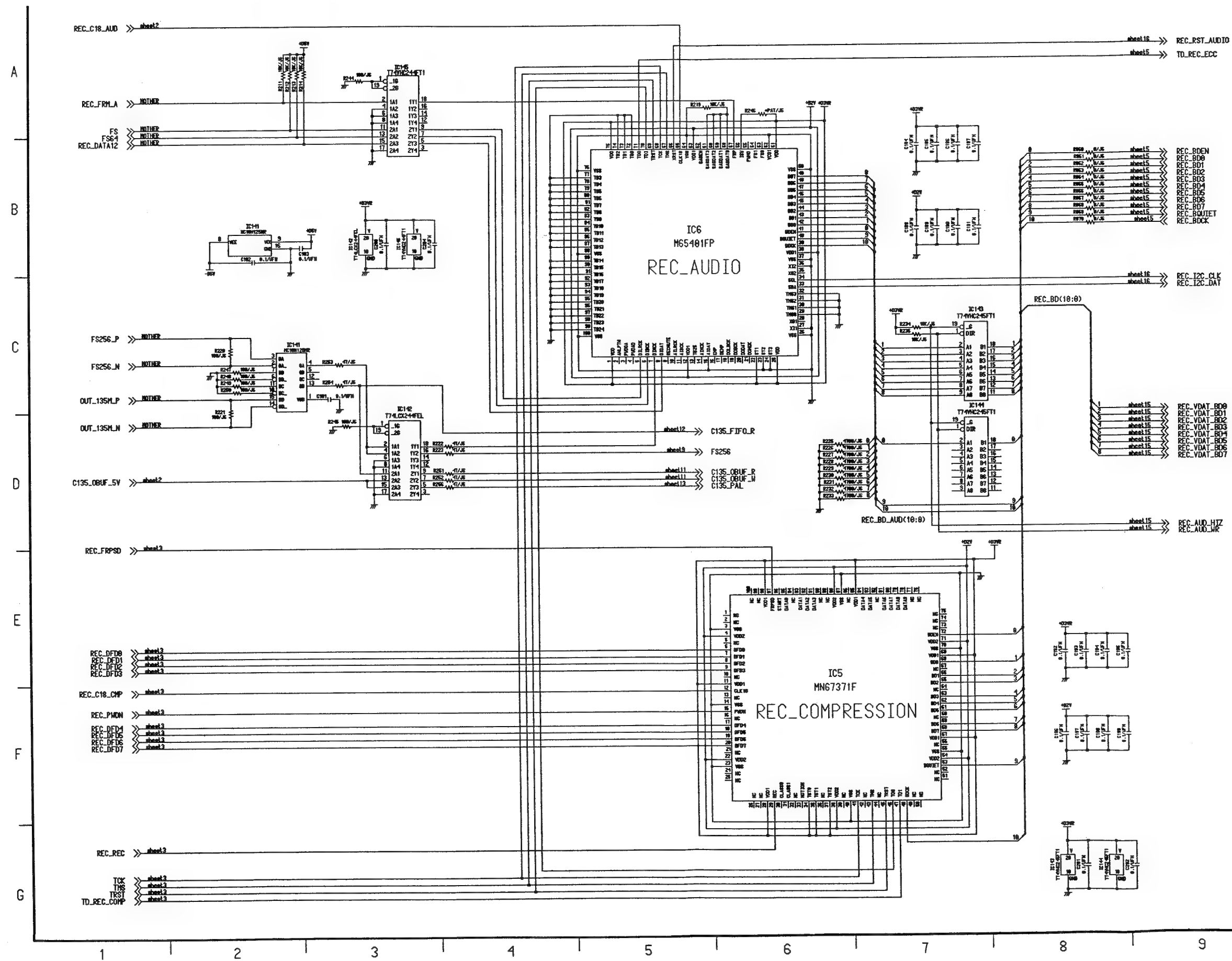
REC PB (F5 2/23) PLL 2 SCHEMATIC DIAGRAM



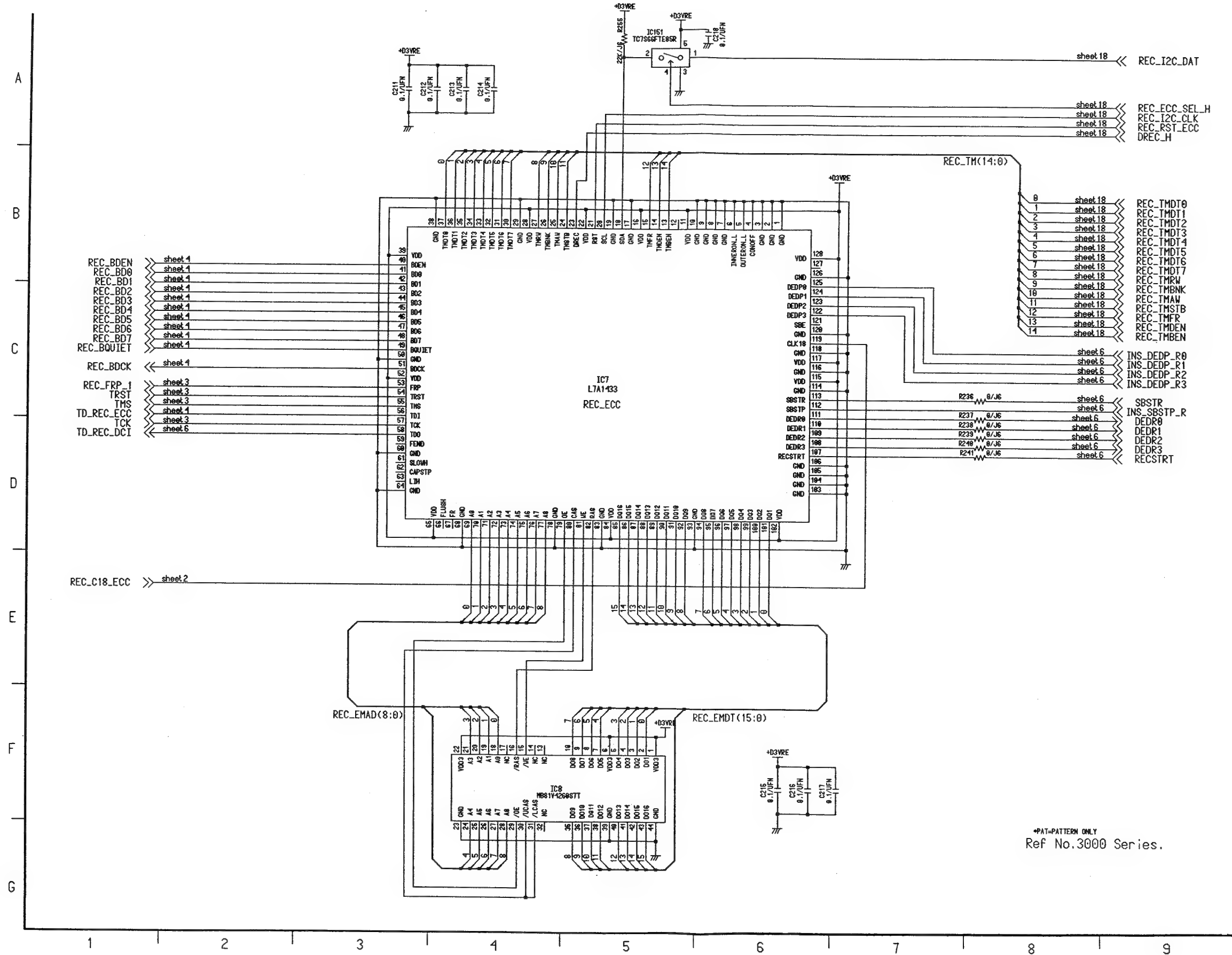
REC PB (F5 3/23) REC SHUF SCHEMATIC DIAGRAM



REC PB (F5 4/23) REC COMP AUD SCHEMATIC DIAGRAM

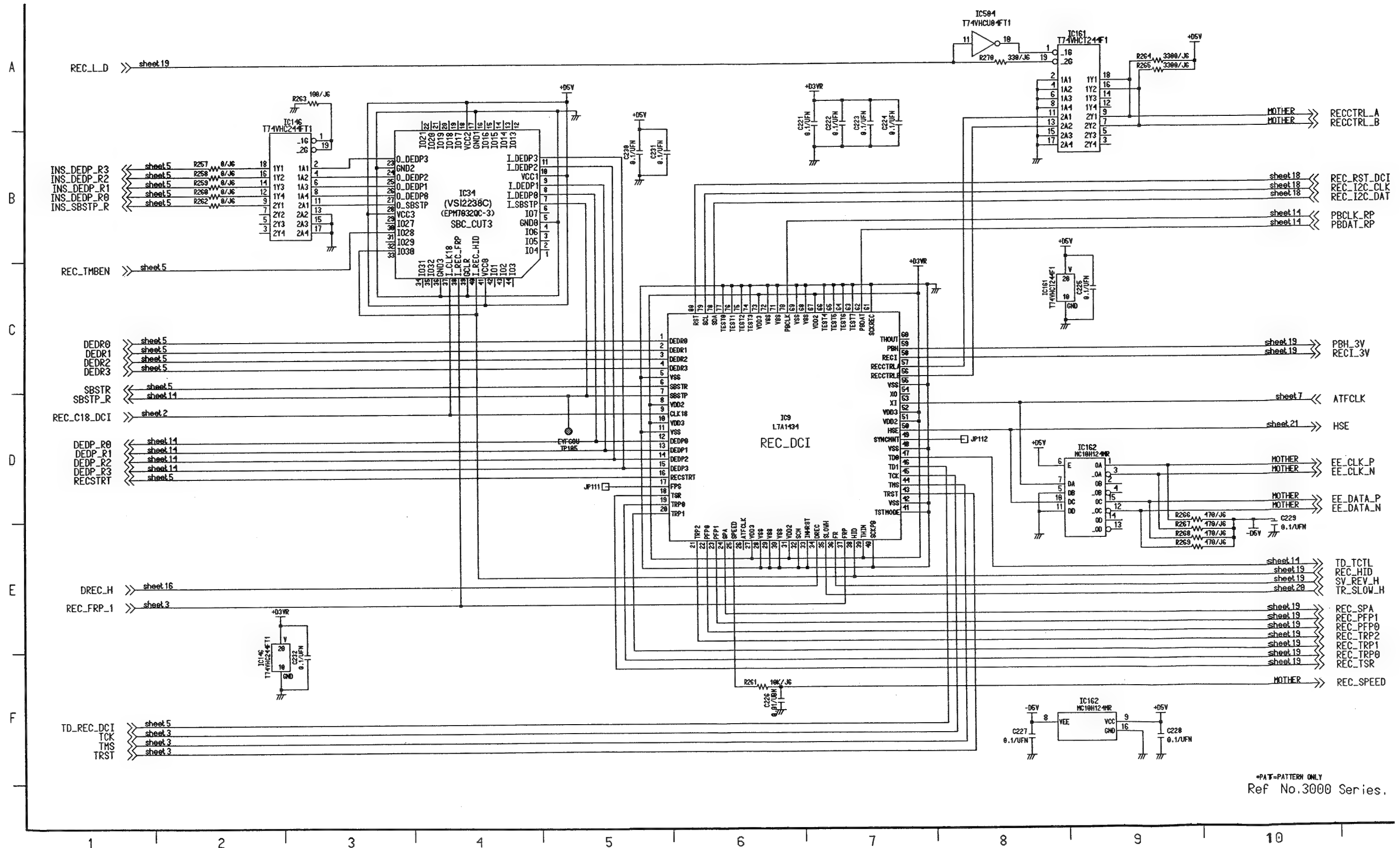


REC PB (F5 5/23) REC ECC SCHEMATIC DIAGRAM



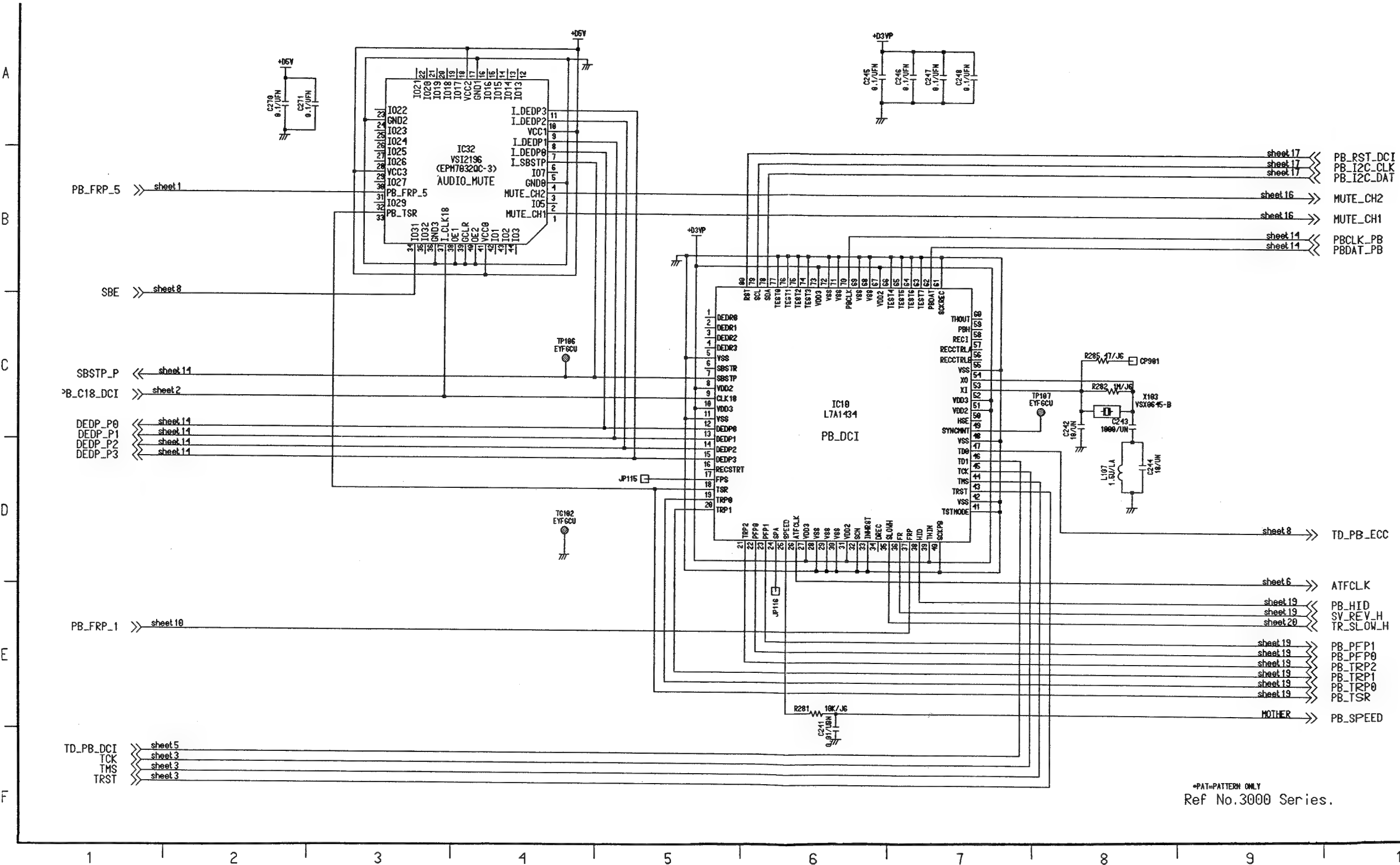
*PAT-PATTERN ONLY
Ref No.3000 Series.

REC PB (F5 6/23) REC DCI SCHEMATIC DIAGRAM



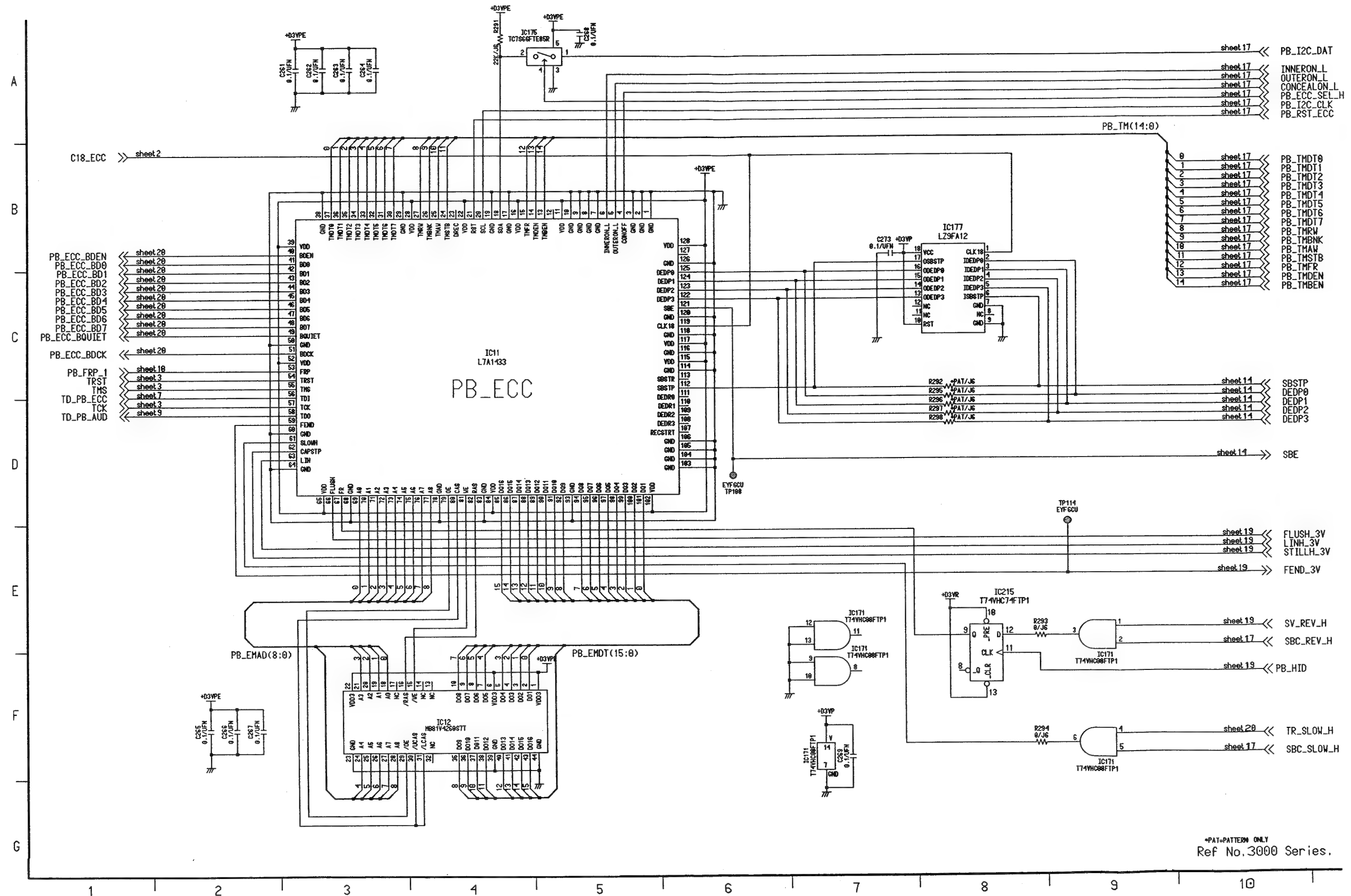
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Ref No.3000 Series.

REC PB (F5 7/23) PB DCI SCHEMATIC DIAGRAM



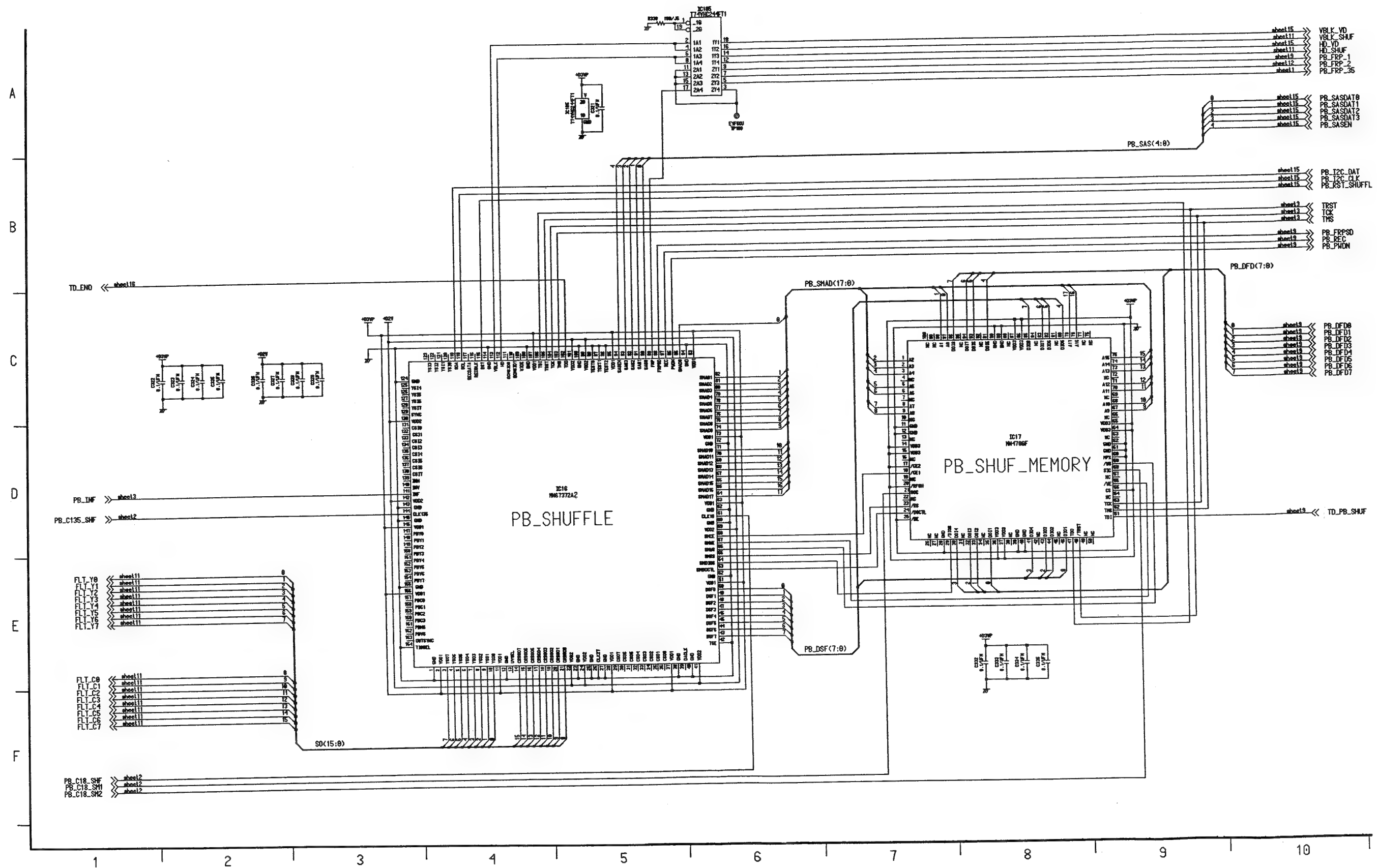
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Ref No.3000 Series.

REC PB (F5 8/23) PB ECC SCHEMATIC DIAGRAM

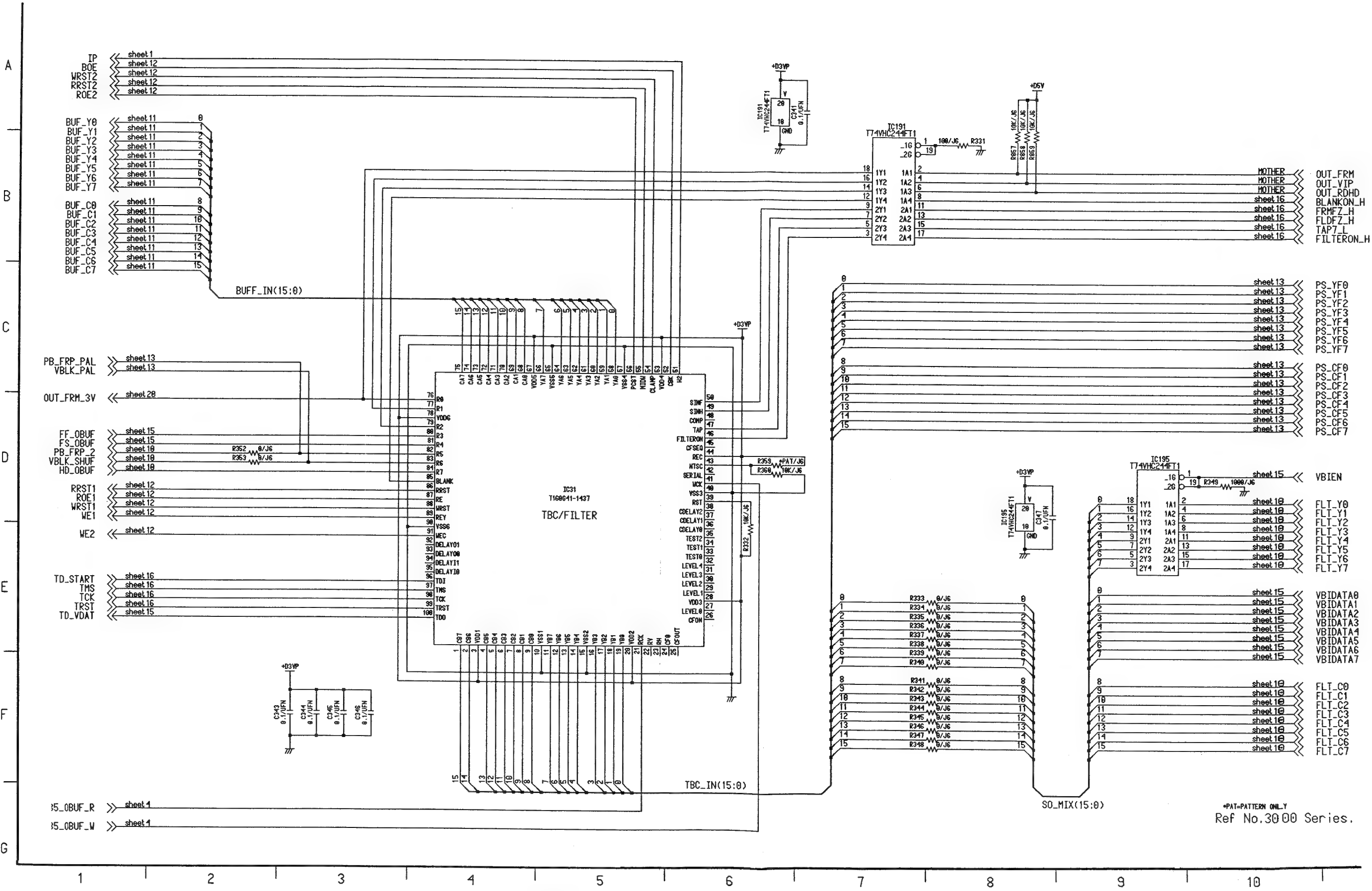


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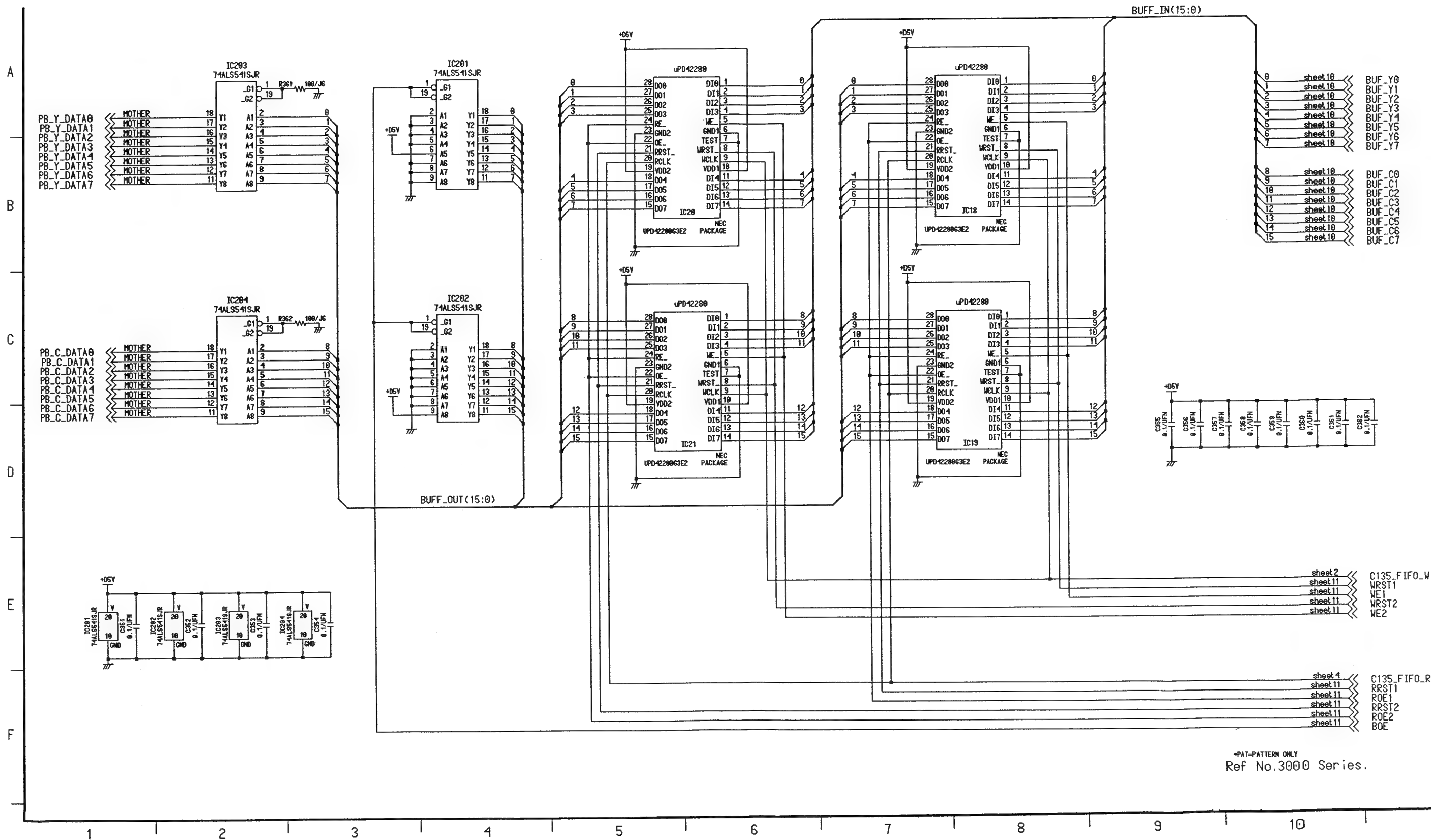
REC PB (F5 10/23) PB SHUF SCHEMATIC DIAGRAM



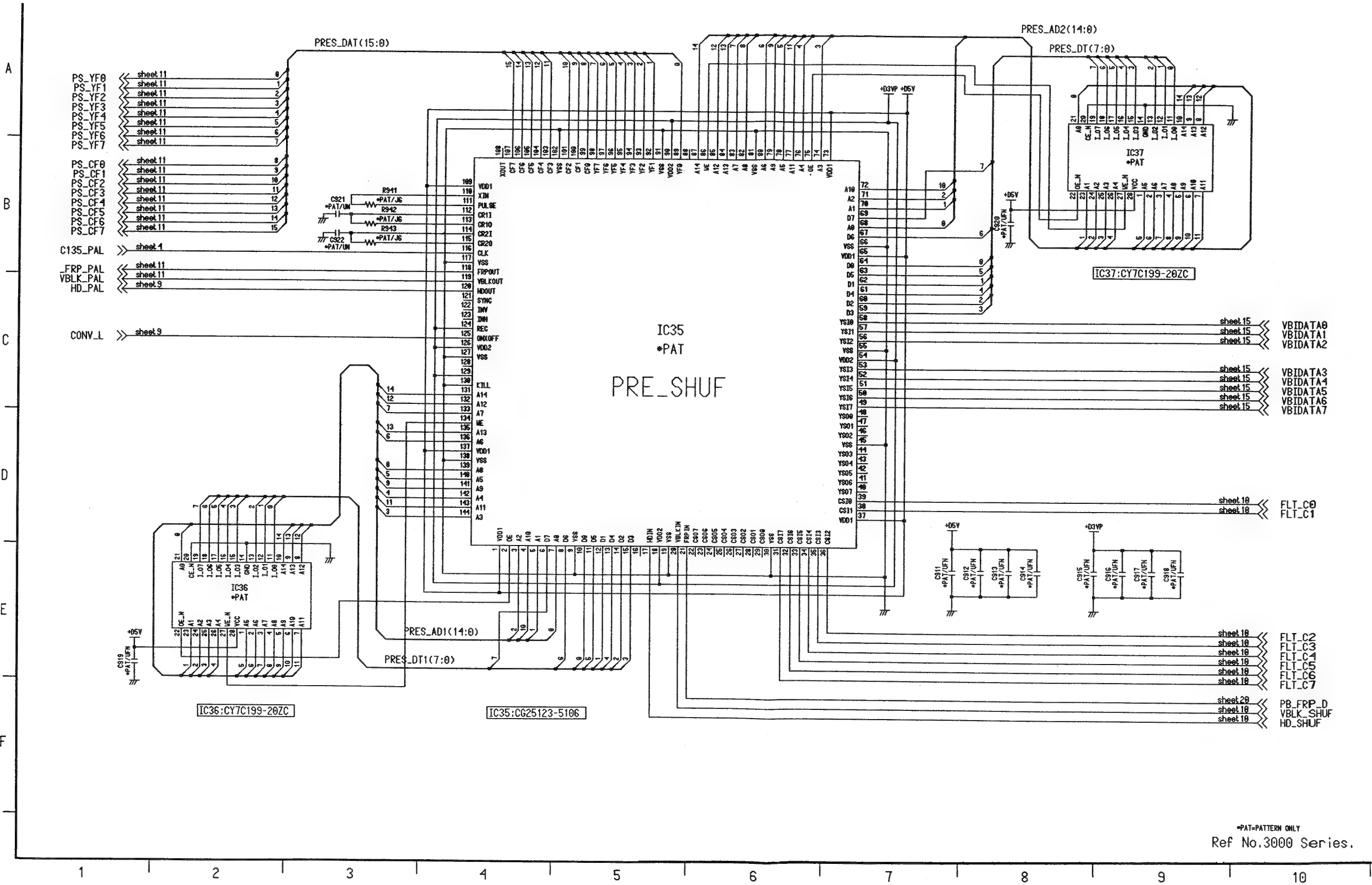
REC PB (F5 11/23) OUT BUFF 1 SCHEMATIC DIAGRAM



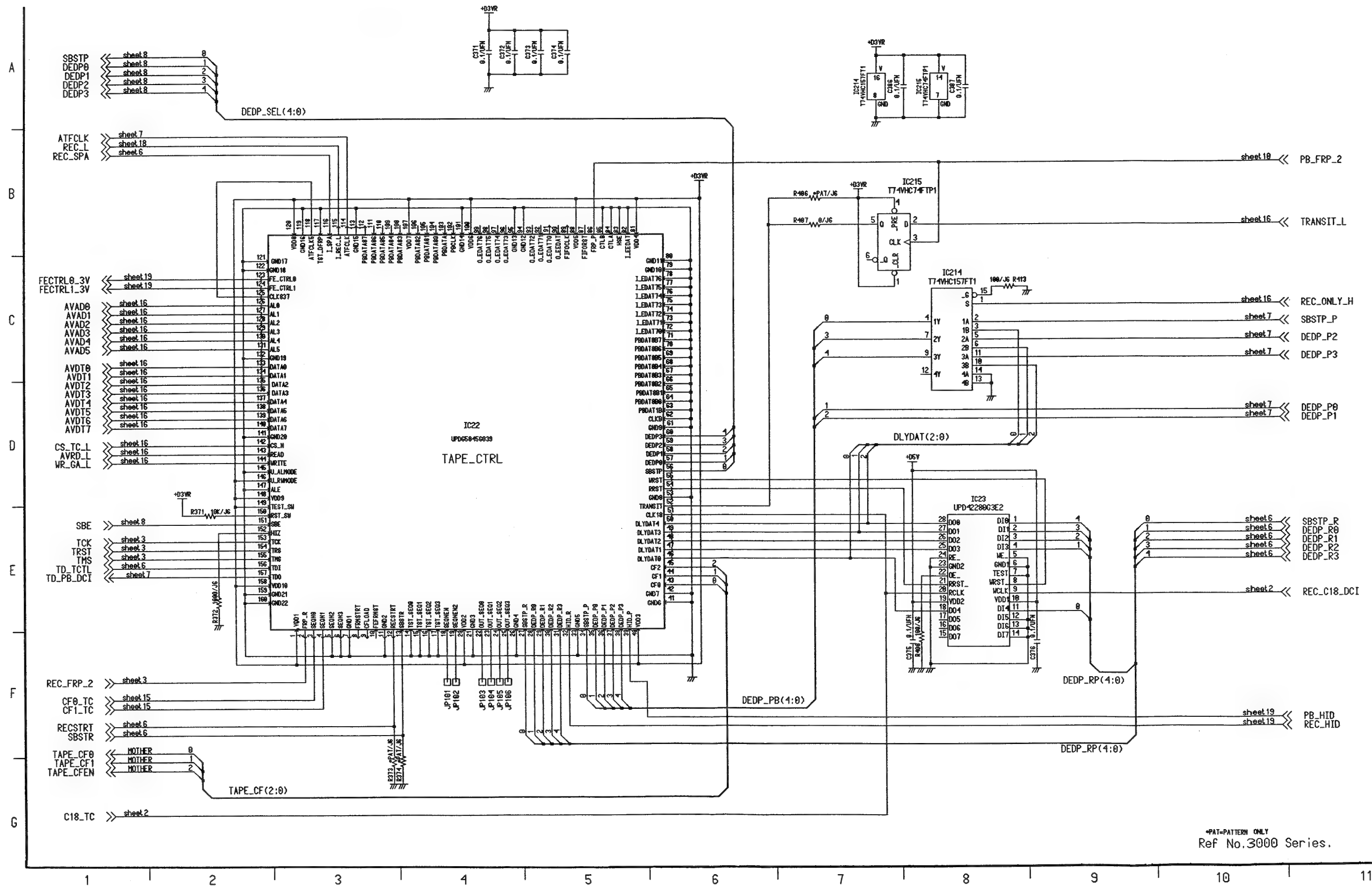
REC PB (F5 12/23) OUT BUFF 2 SCHEMATIC DIAGRAM



REC PB (F5 13/23) CONNECTOR SCHEMATIC DIAGRAM

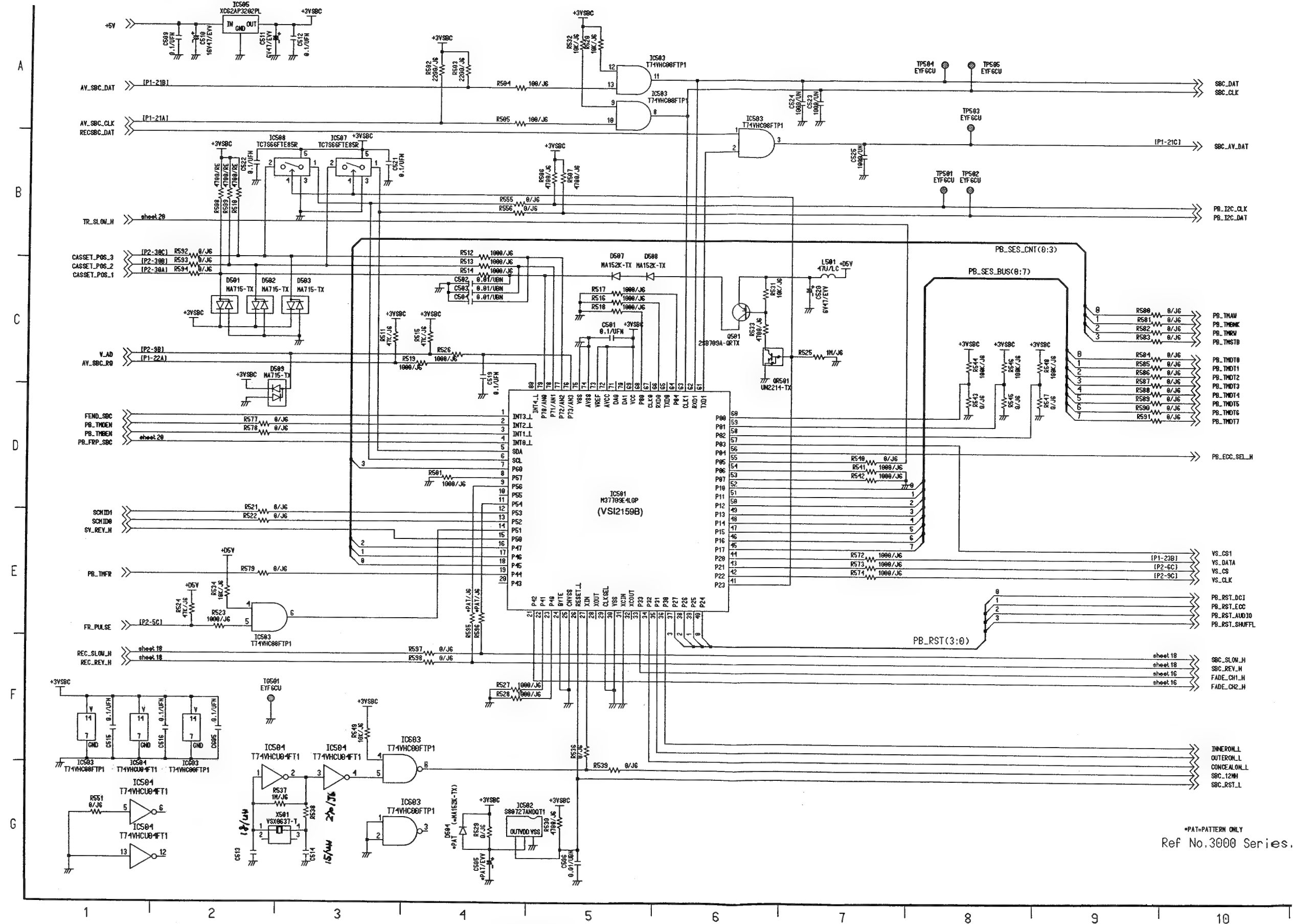


REC PB (F5 14/23) TAPE CTRL SCHEMATIC DIAGRAM



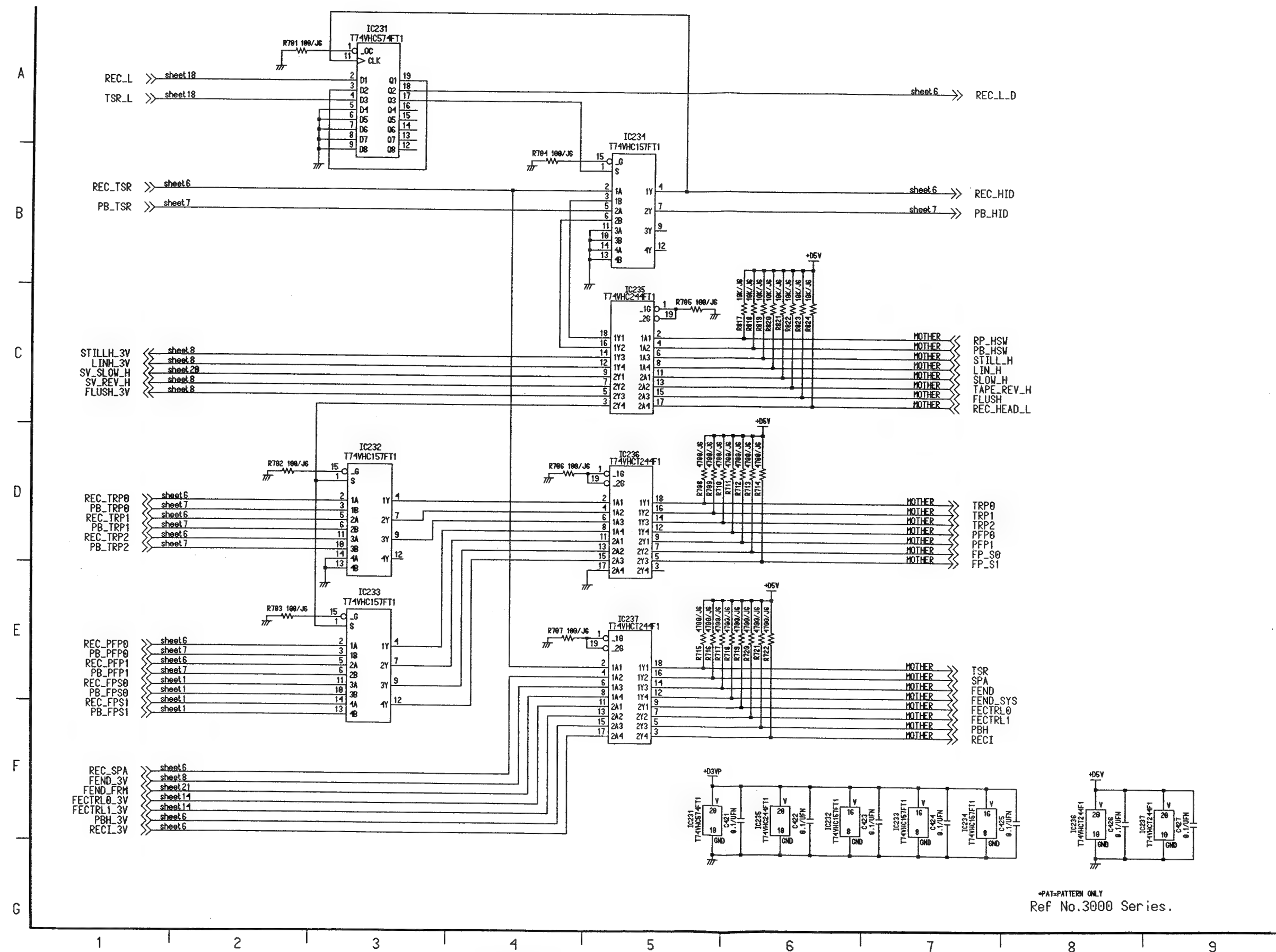
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Ref No.3000 Series.

REC PB (F5 17/23) SBC PB SCHEMATIC DIAGRAM

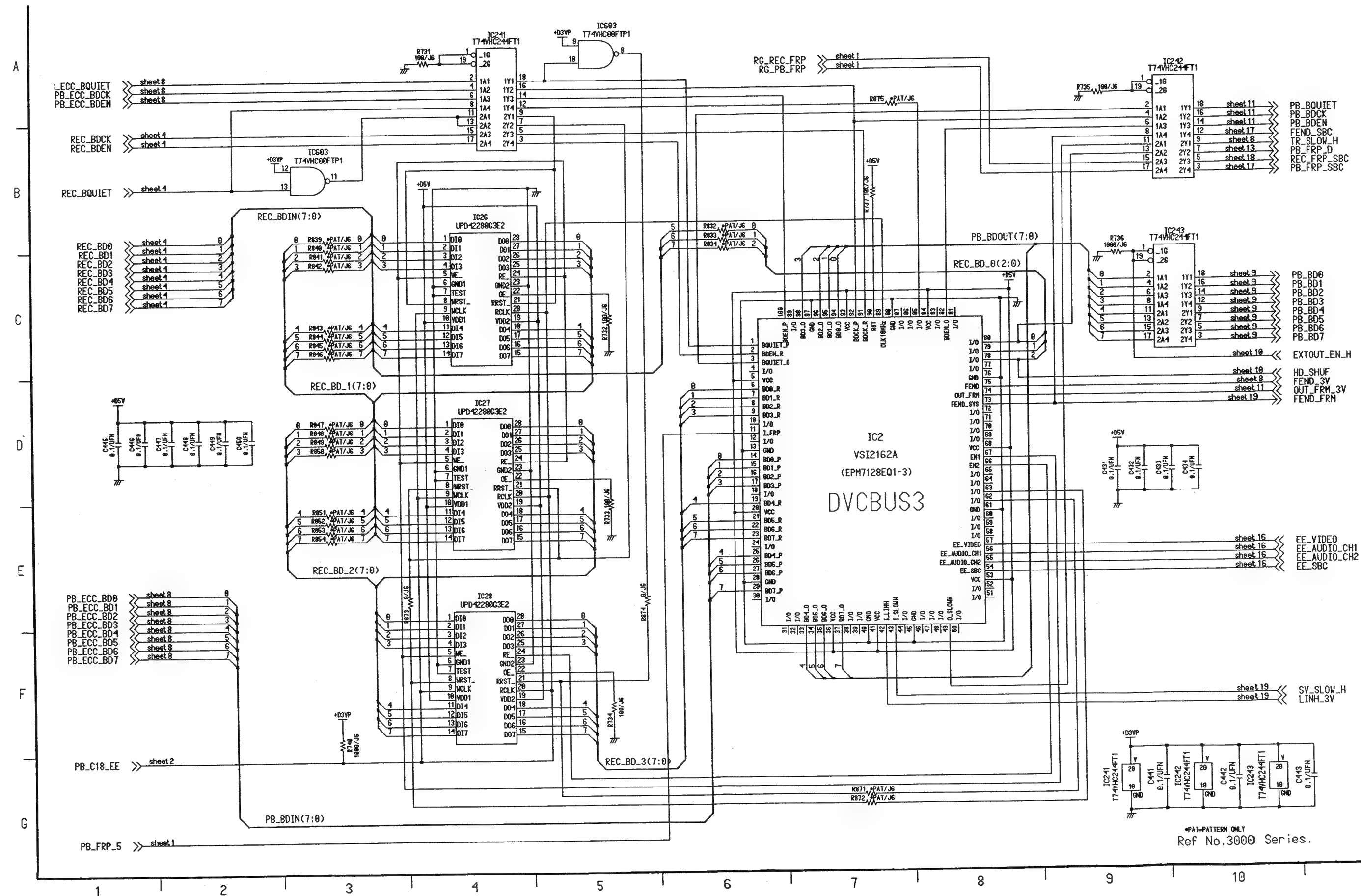


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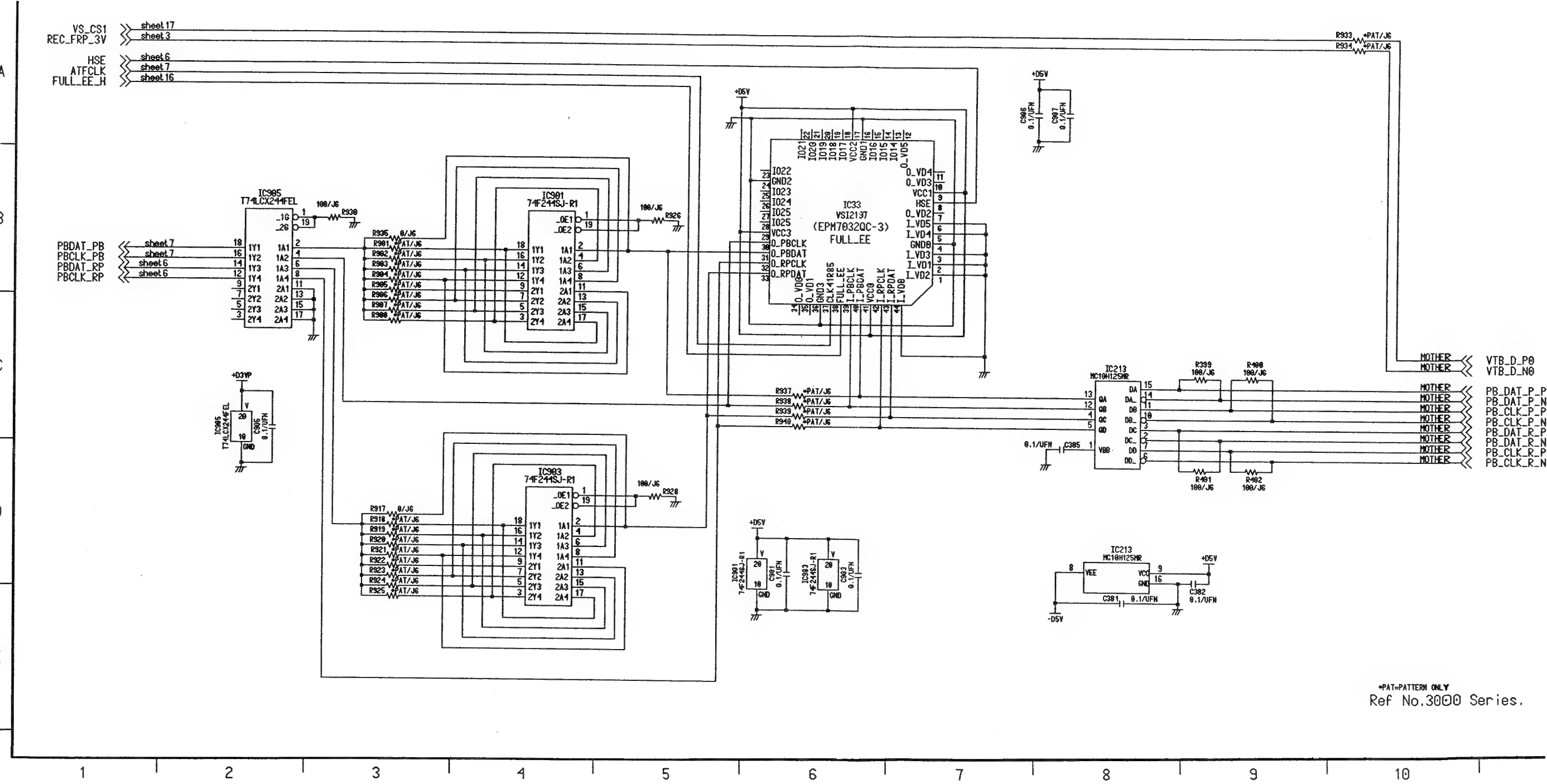
REC PB (F5 19/23) SERVO SEPA SCHEMATIC DIAGRAM



REC PB (F5 20/23) DVC RETERN SCHEMATIC DIAGRAM

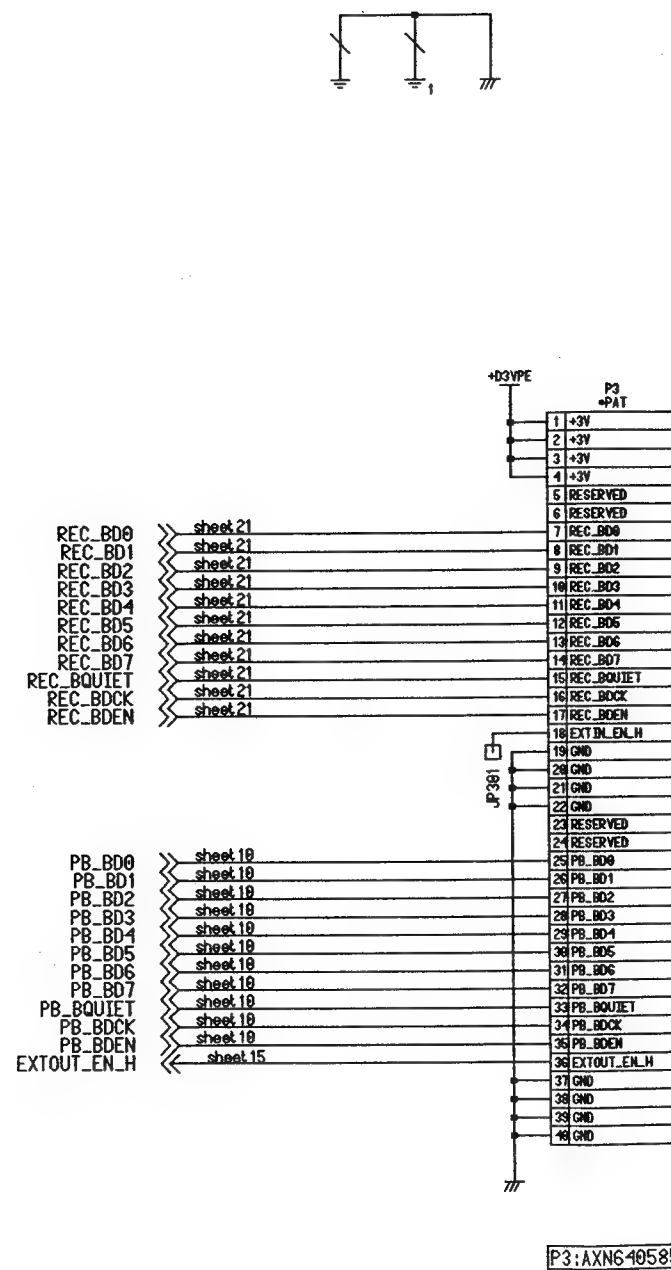
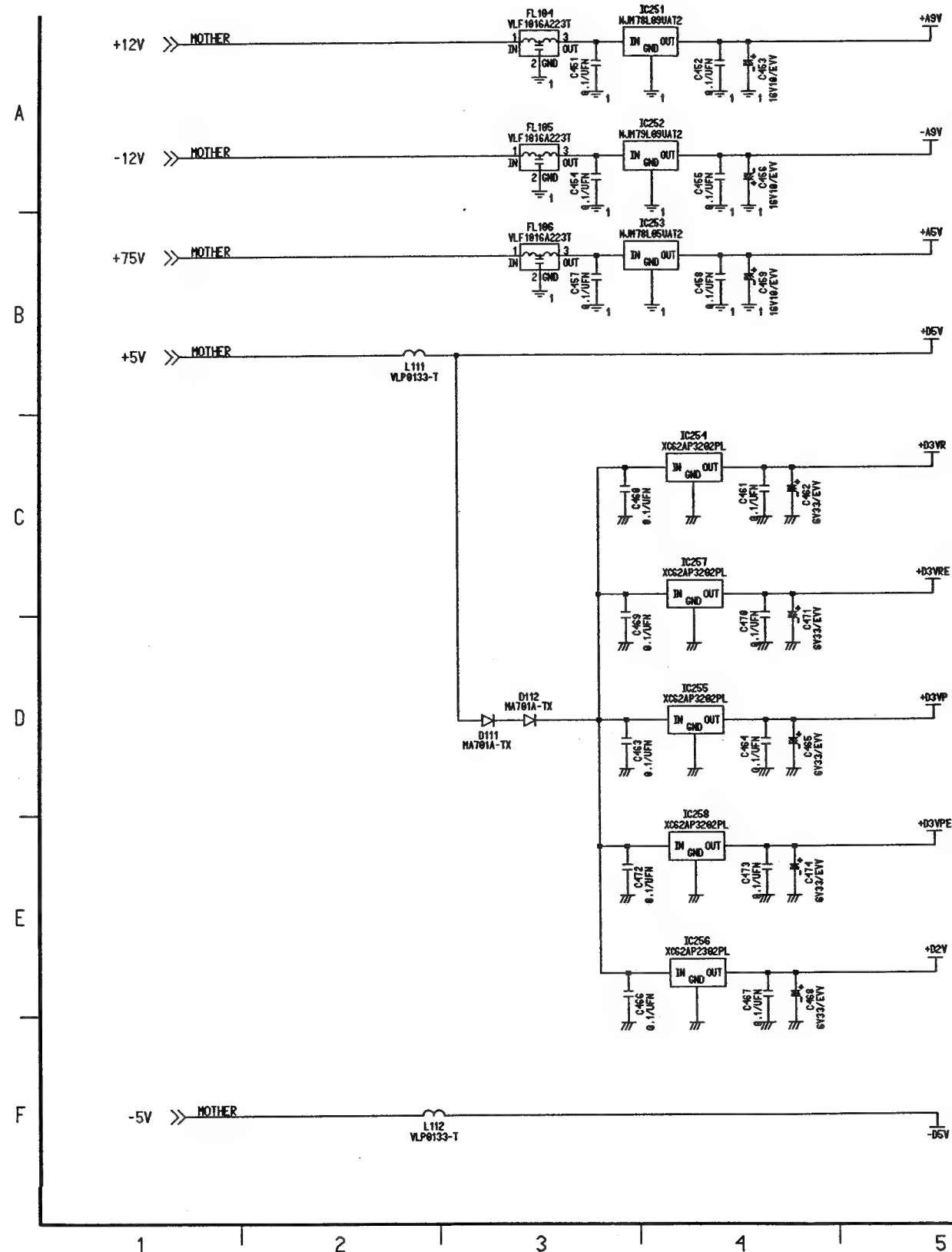


REC PB (F5 21/23) RF DATA SCHEMATIC DIAGRAM



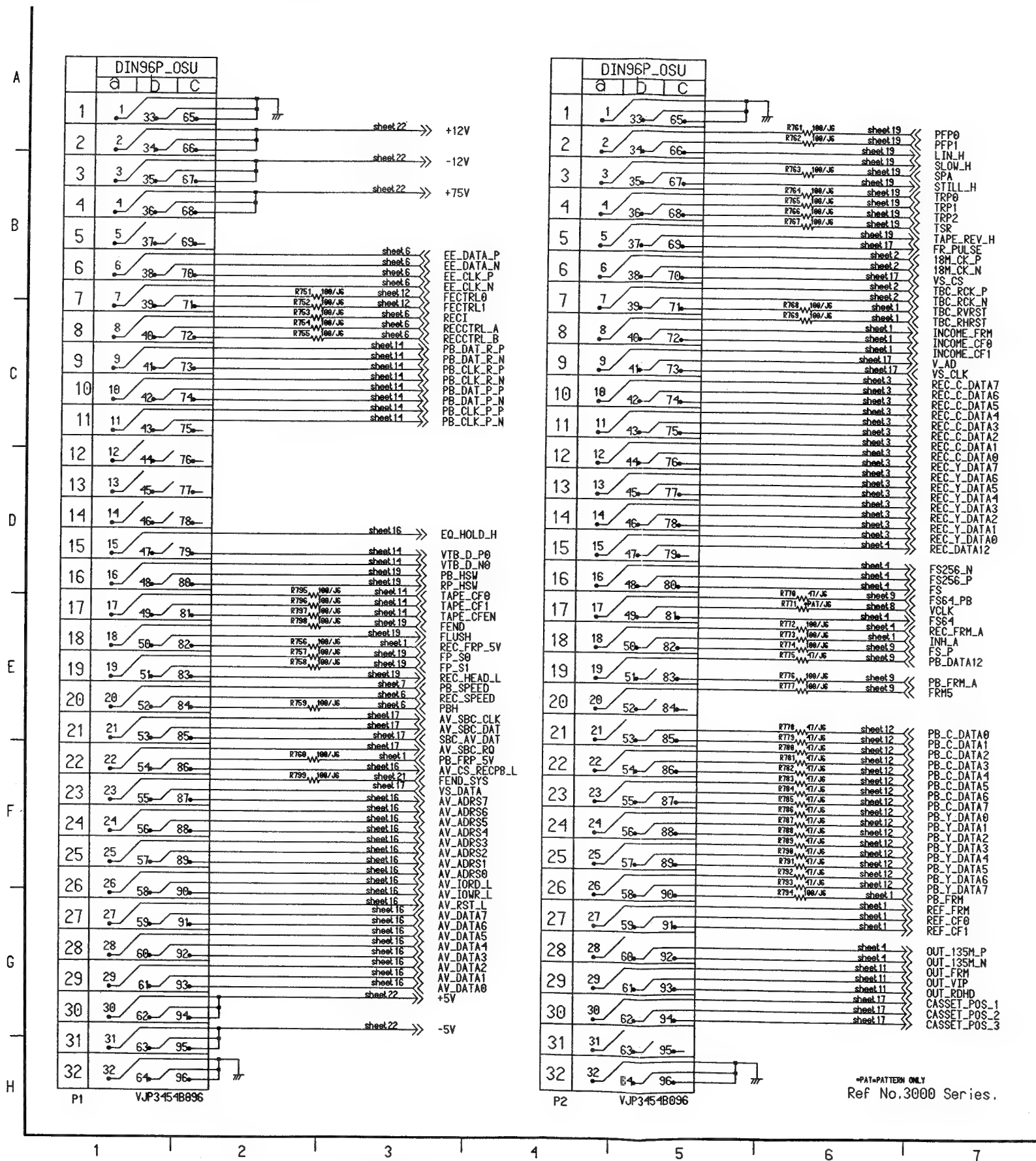
*PAT=PATTERN ONLY
Ref No.3000 Series.

REC PB (F5 22/23) POWER SCHEMATIC DIAGRAM



•PAT=PATTERN ONLY
Ref No.3000 Series.

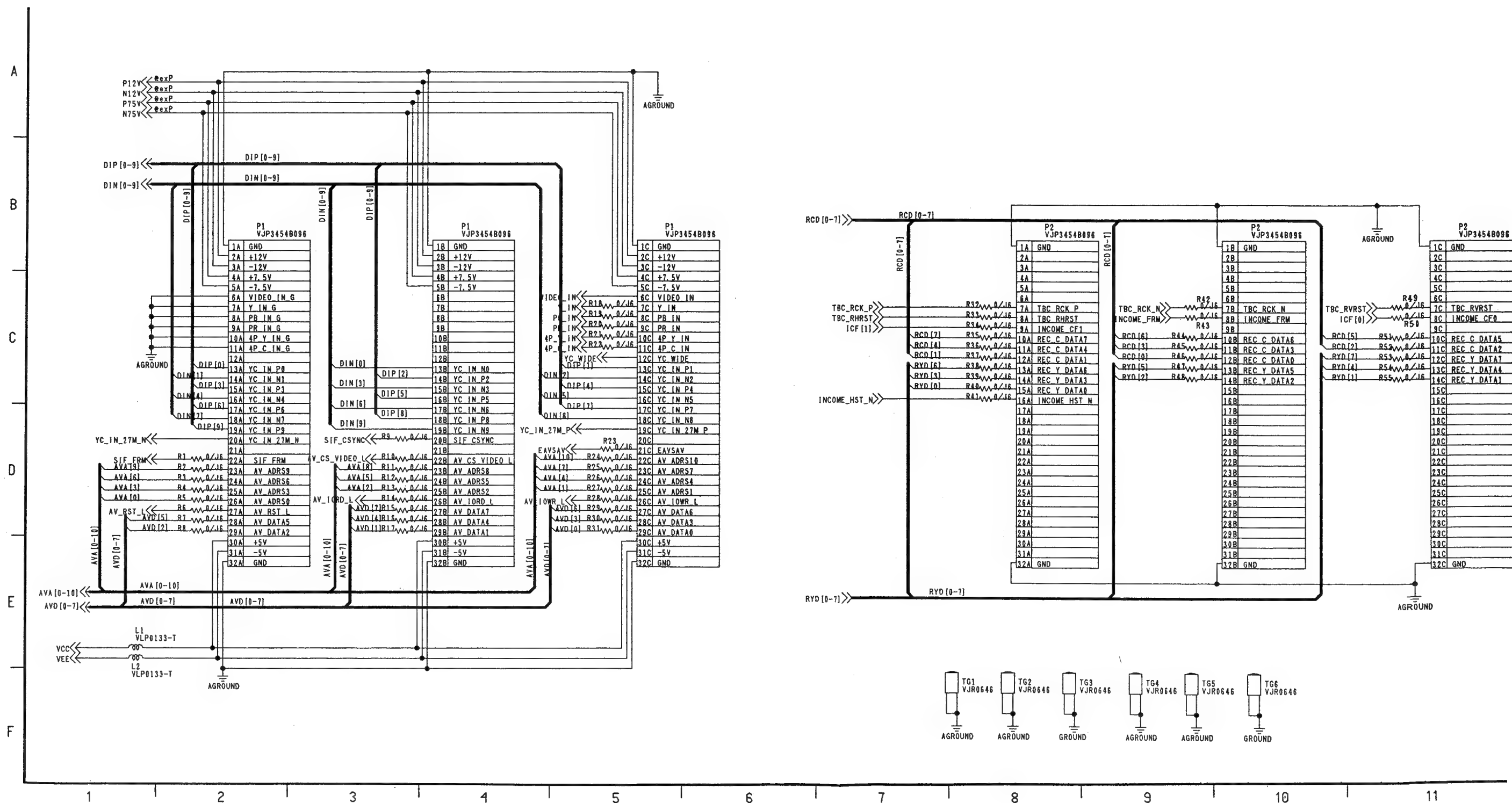
REC PB (F5 23/23) CONNECTOR SCHEMATIC DIAGRAM



REC PB (F5) COMPARISON CHART BETWEEN MODELS

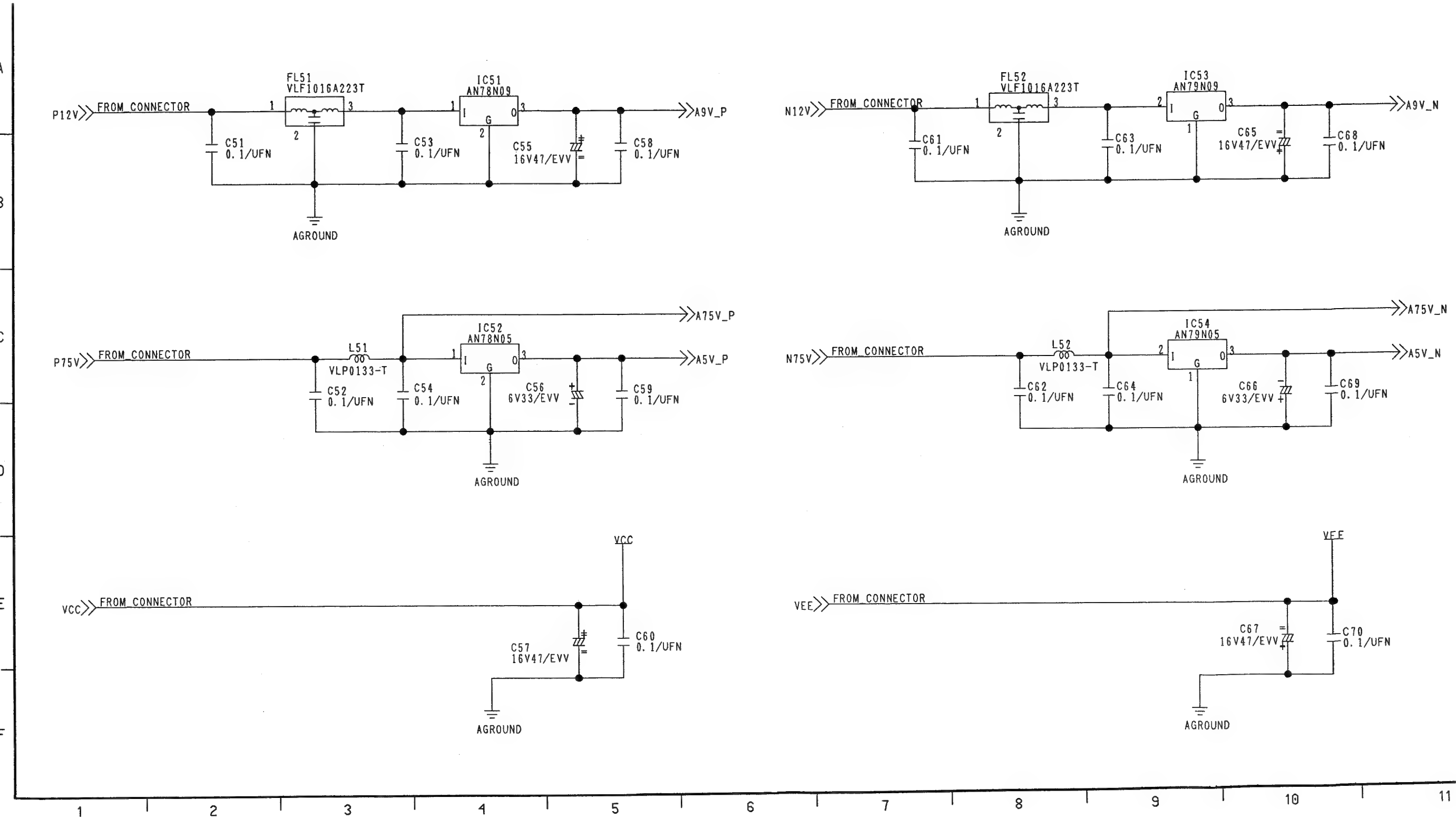
Ref. No.	NTSC	PAL
C911	PAT/UFN	ECUV1E104ZFN
C912	PAT/UFN	ECUV1E104ZFN
C913	PAT/UFN	ECUV1E104ZFN
C914	PAT/UFN	ECUV1E104ZFN
C915	PAT/UFN	ECUV1E104ZFN
C916	PAT/UFN	ECUV1E104ZFN
C917	PAT/UFN	ECUV1E104ZFN
C918	PAT/UFN	ECUV1E104ZFN
C919	PAT/UFN	ECUV1E104ZFN
C920	PAT/UFN	ECUV1E104ZFN
C921	PAT/UN	ECUV1H330JCN
C922	PAT/UN	ECUV1H150JCN
IC1	VS12161	VS12268
IC17	MN4706F	MN4707F
IC2	VS12162A	VS12269
IC32	VS12196	VS12270
IC34	VS12238B	VS12271A
IC35	PAT	CG25123-5106
IC36	PAT	CY7C199-20ZC
IC37	PAT	CY7C199-20ZC
IC4	MN4706F	MN4707F
IC501	VS12159B	VS12282
IC601	VS12159B	VS12282
R101	ERJ6GEY0R00V	PAT/J6
R102	PAT/J6	ERJ6GEY0R00V
R309	ERJ6GEY0R00V	PAT/J6
R333	ERJ6GEY0R00V	PAT/J6
R334	ERJ6GEY0R00V	PAT/J6
R335	ERJ6GEY0R00V	PAT/J6
R336	ERJ6GEY0R00V	PAT/J6
R337	ERJ6GEY0R00V	PAT/J6
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R347	ERJ6GEY0R00V	PAT/J6
R348	ERJ6GEY0R00V	PAT/J6
R352	ERJ6GEY0R00V	PAT/J6
R353	ERJ6GEY0R00V	PAT/J6
R359	PAT/J6	ERJ6GEYJ103V
R360	ERJ6GEYJ103V	PAT/J6
R543	ERJ6GEY0R00V	PAT/J6
R626	ERJ6GEY0R00V	PAT/J6
R875	PAT/J6	ERJ6GEY0R00V
R941	PAT/J6	ERJ6GEY0R00V
R942	PAT/J6	ERJ6GEYJ271V
R943	PAT/J6	ERJ6GEYJ101V

V IN (F6 1/18) CONNECTOR SCHEMATIC DIAGRAM

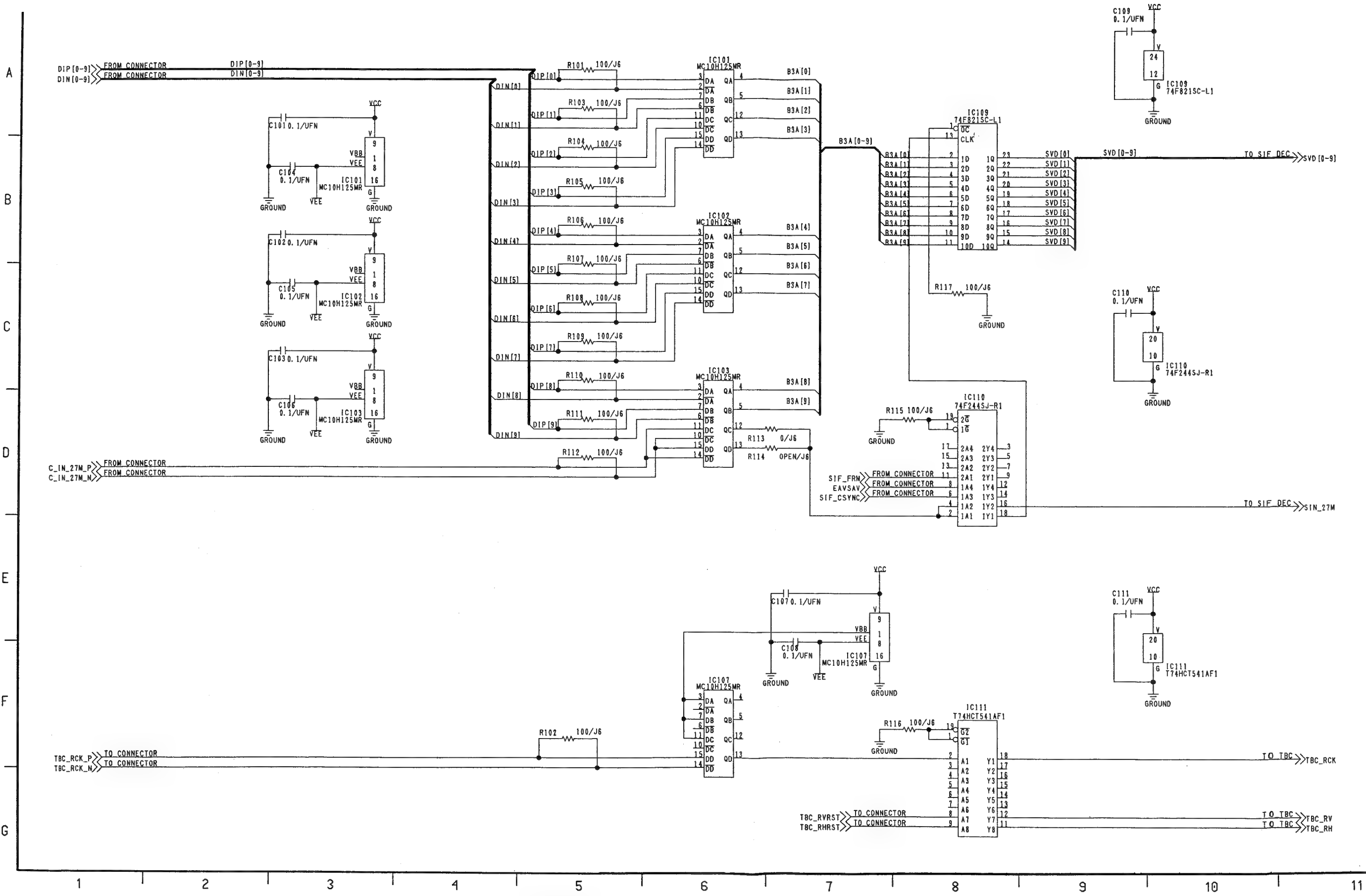


REVERSE SIDE
F5 CHART

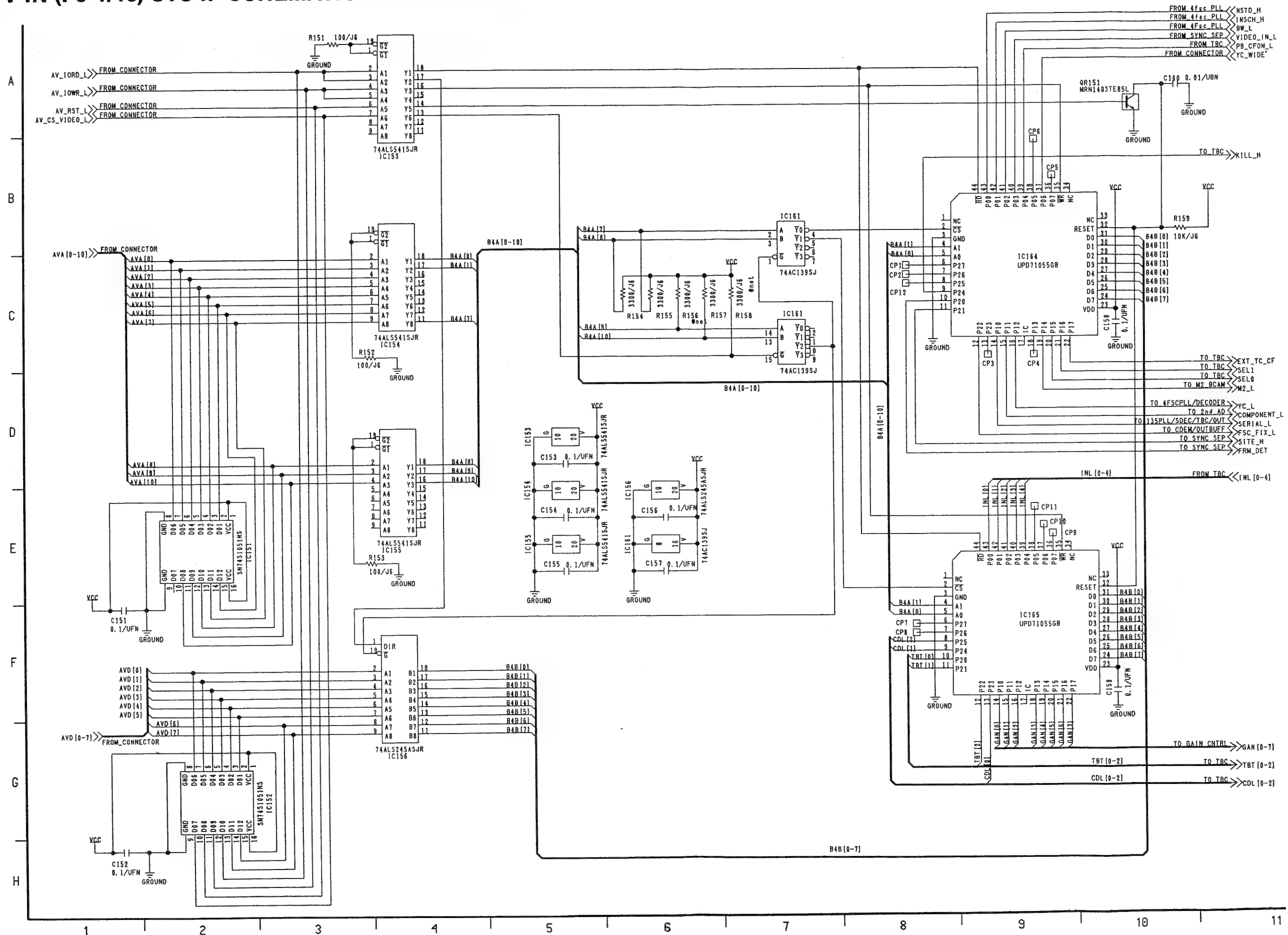
V IN (F6 2/18) POWER SCHEMATIC DIAGRAM



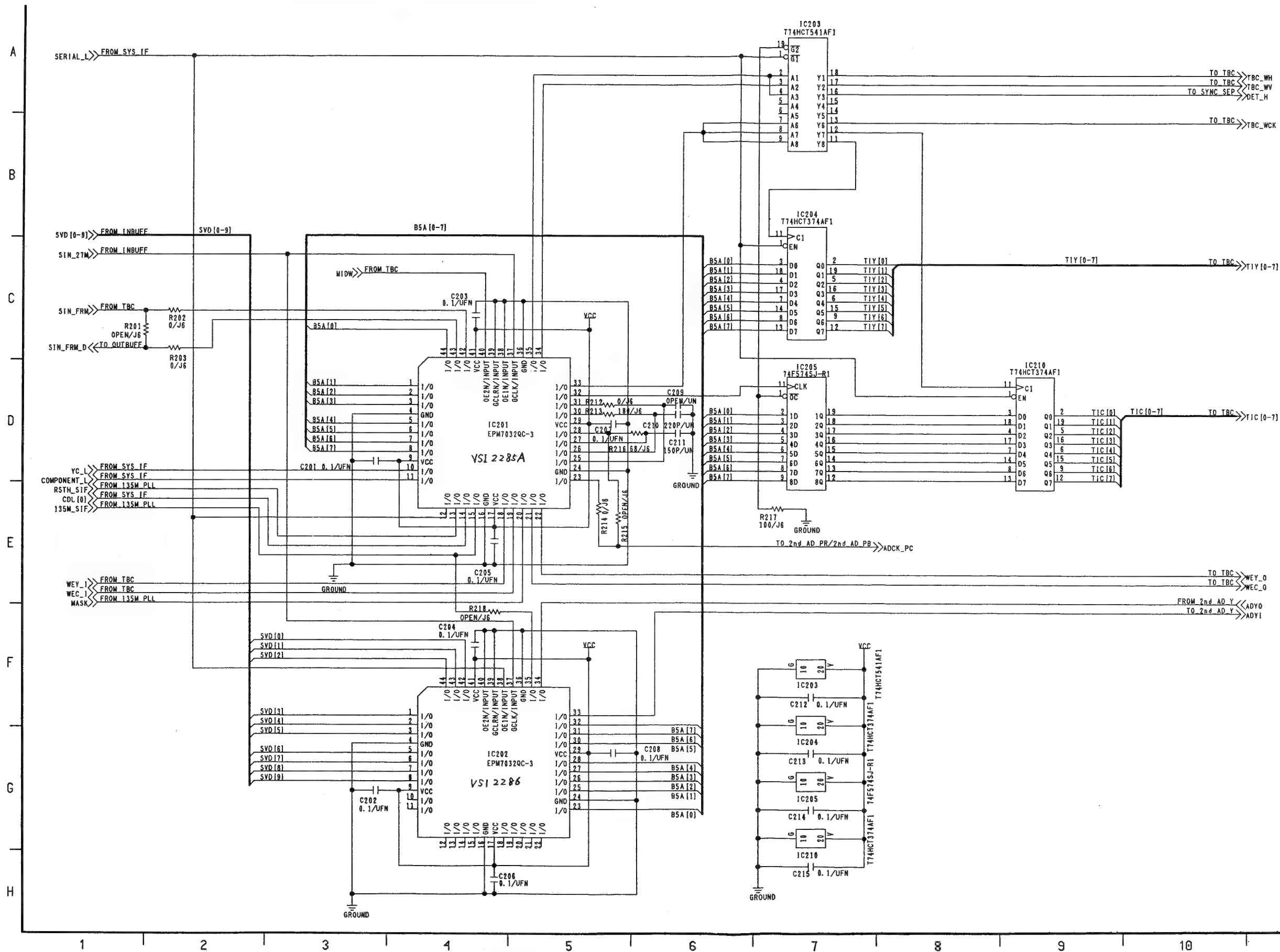
V IN (F6 3/18) IN BUFF SCHEMATIC DIAGRAM



V IN (F6 4/18) SYS IF SCHEMATIC DIAGRAM

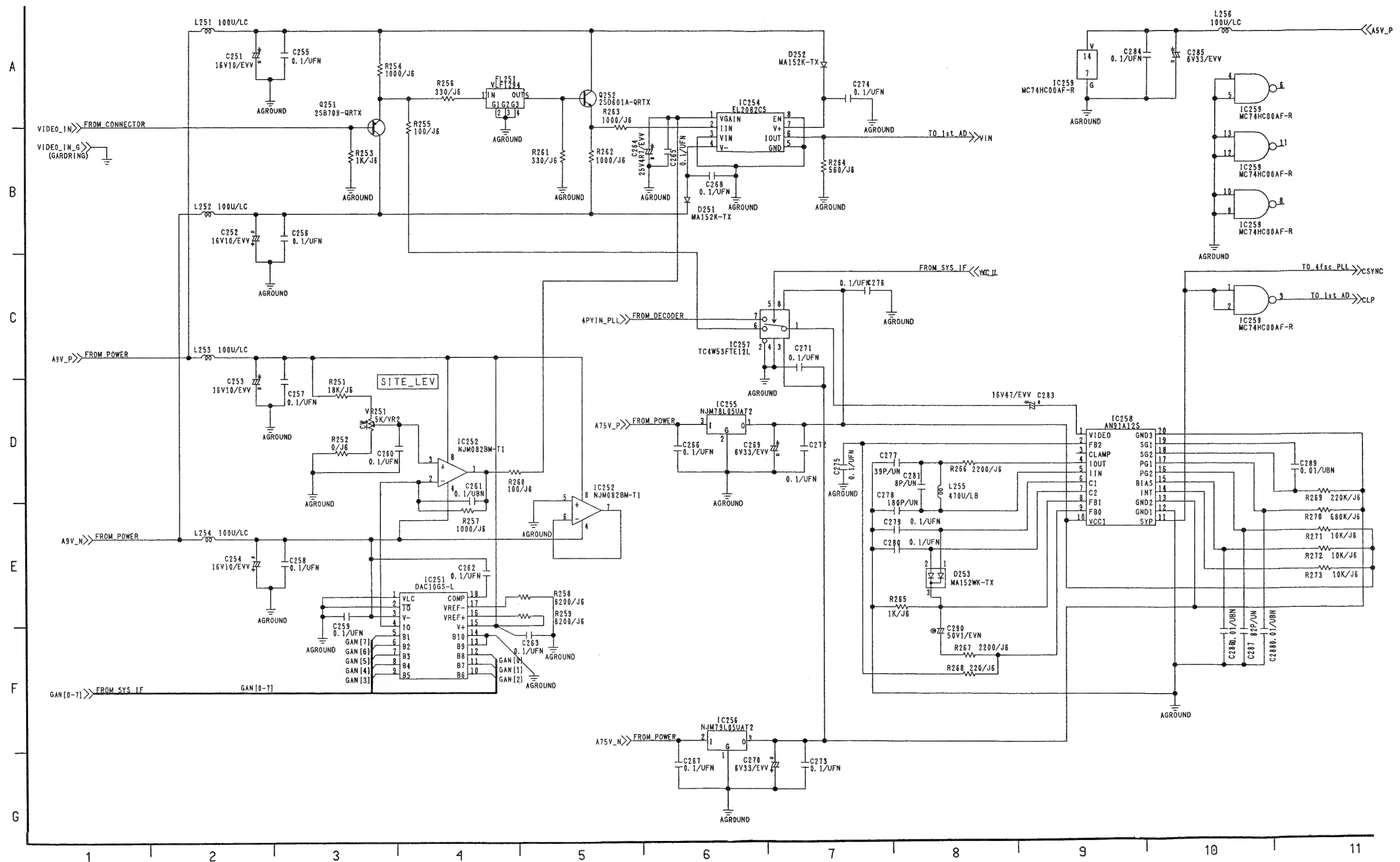


V IN (F6 5/18) SIF DEC SCHEMATIC DIAGRAM

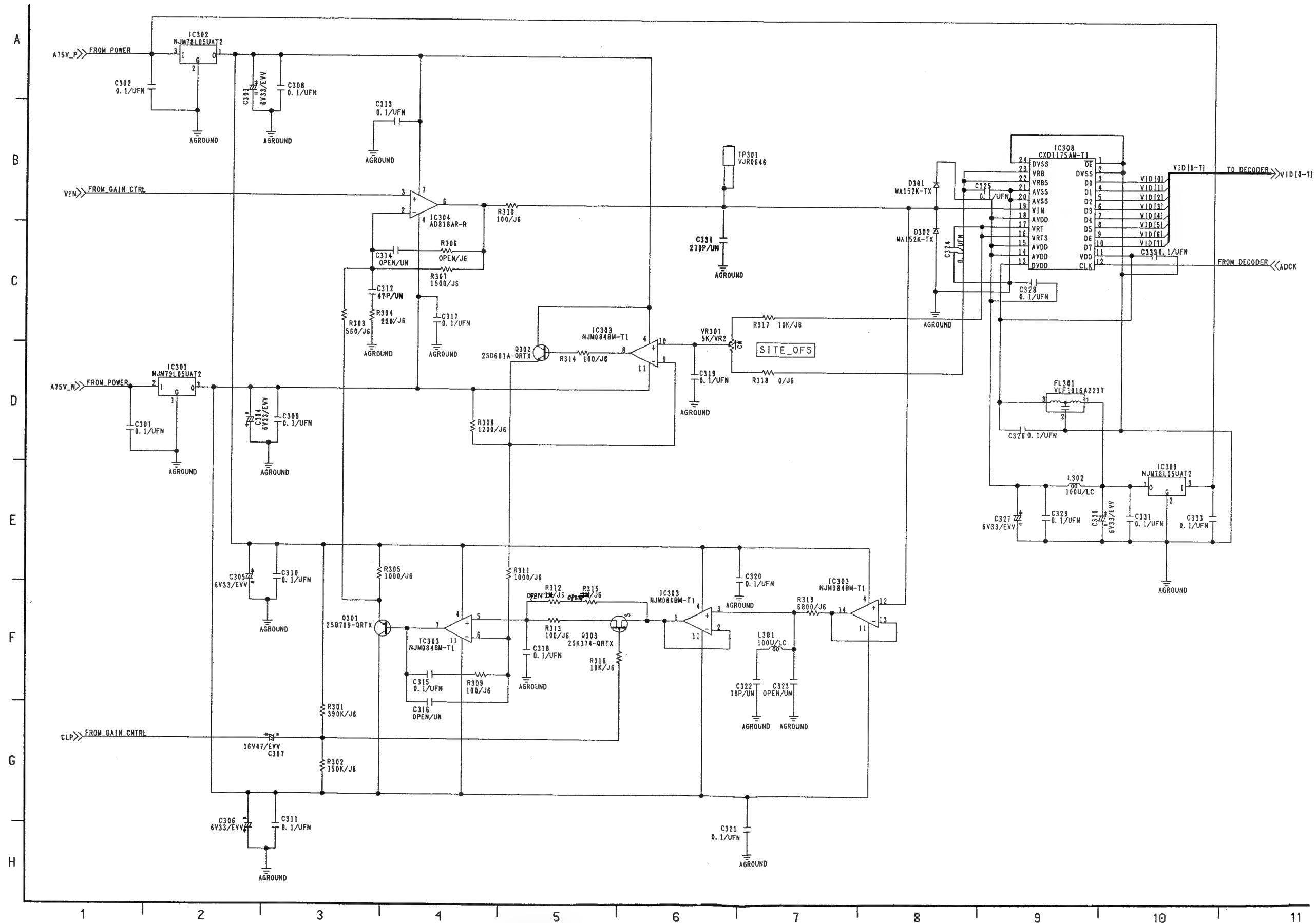


REVERSE SIDE
F6 V IN 4/18

V IN (F6 6/18) GAIN CTRL SCHEMATIC DIAGRAM



V IN (F6 7/18) 1st AD SCHEMATIC DIAGRAM

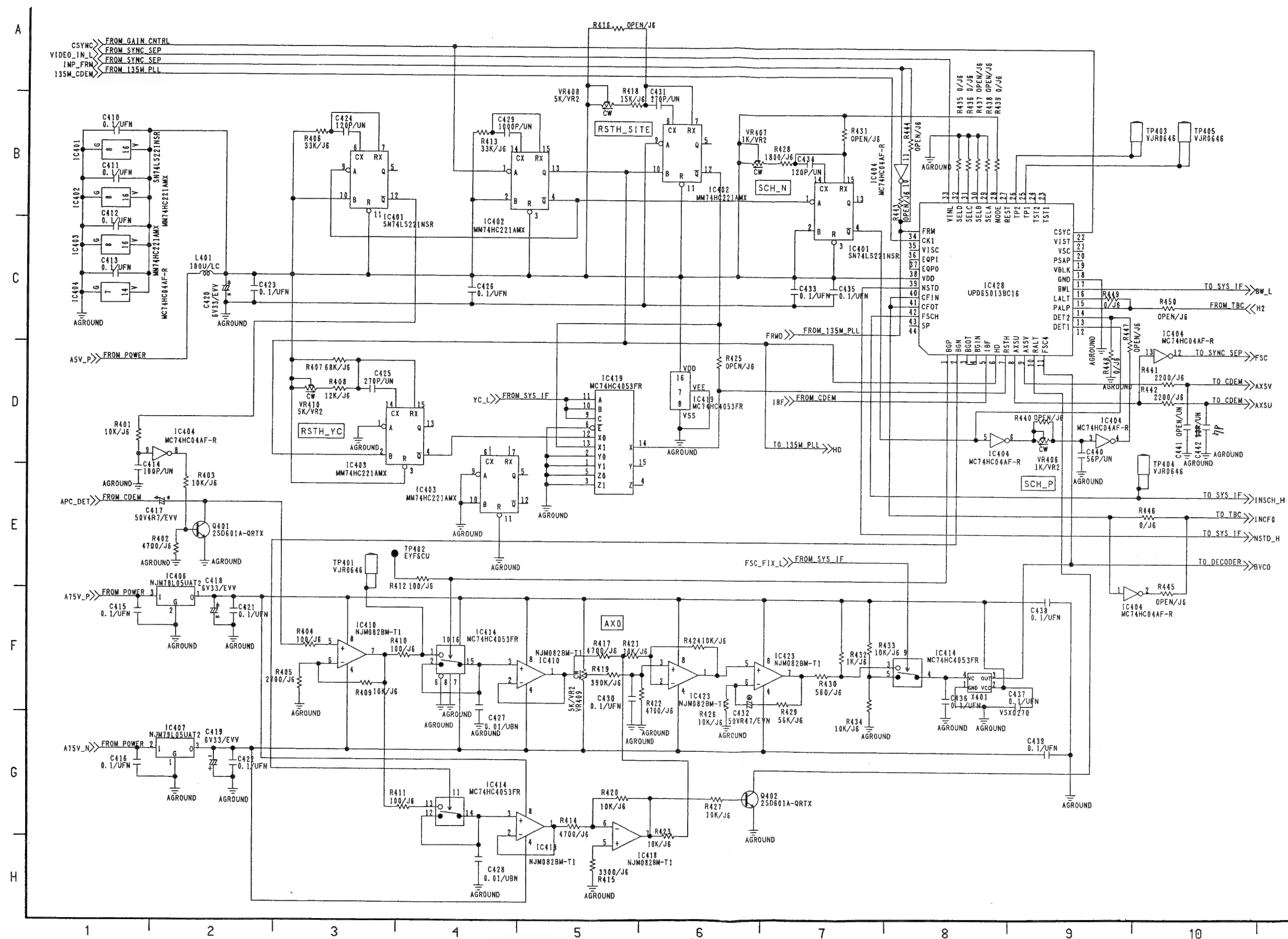


REVERSE SIDE

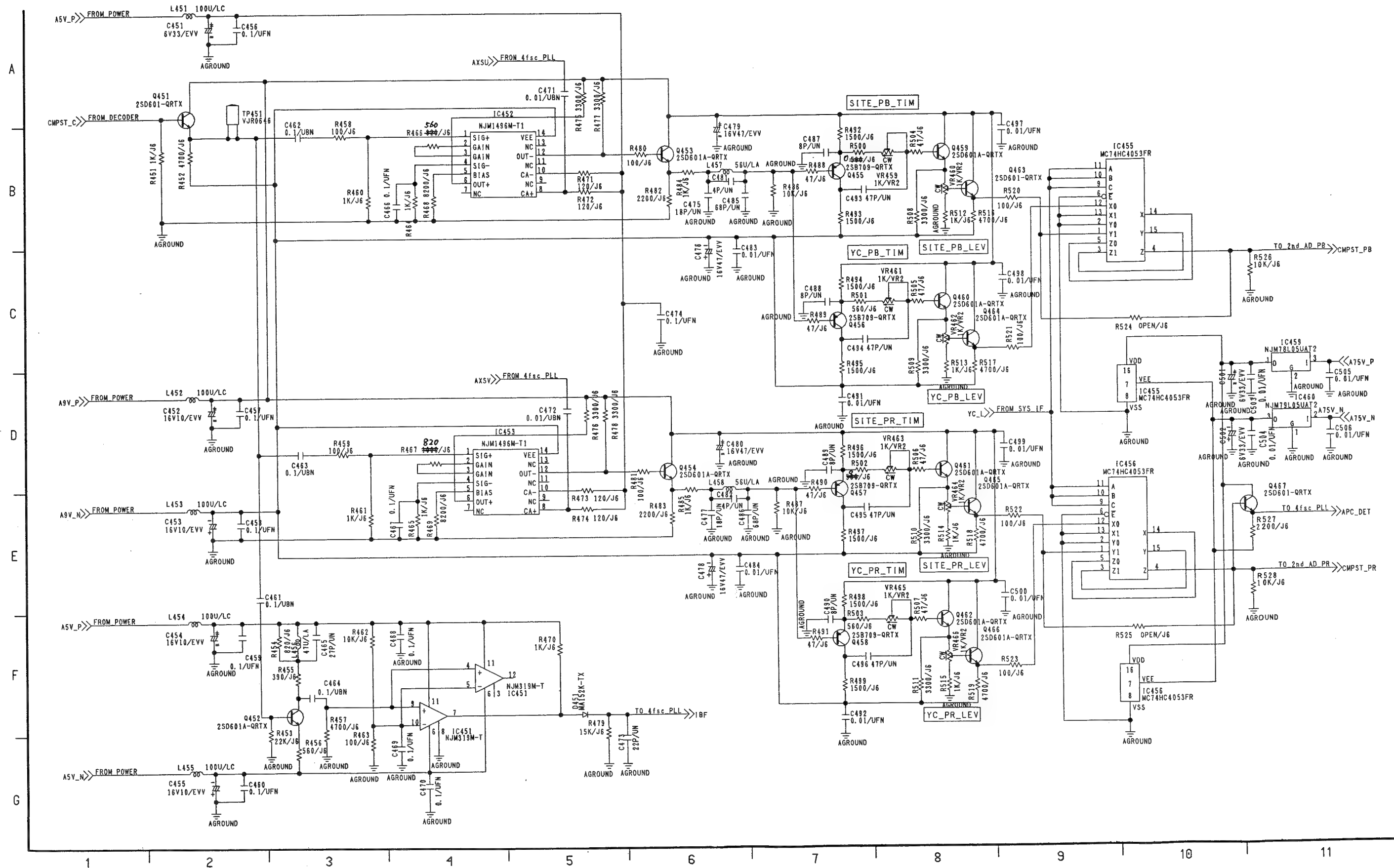
F6 V IN 6/18



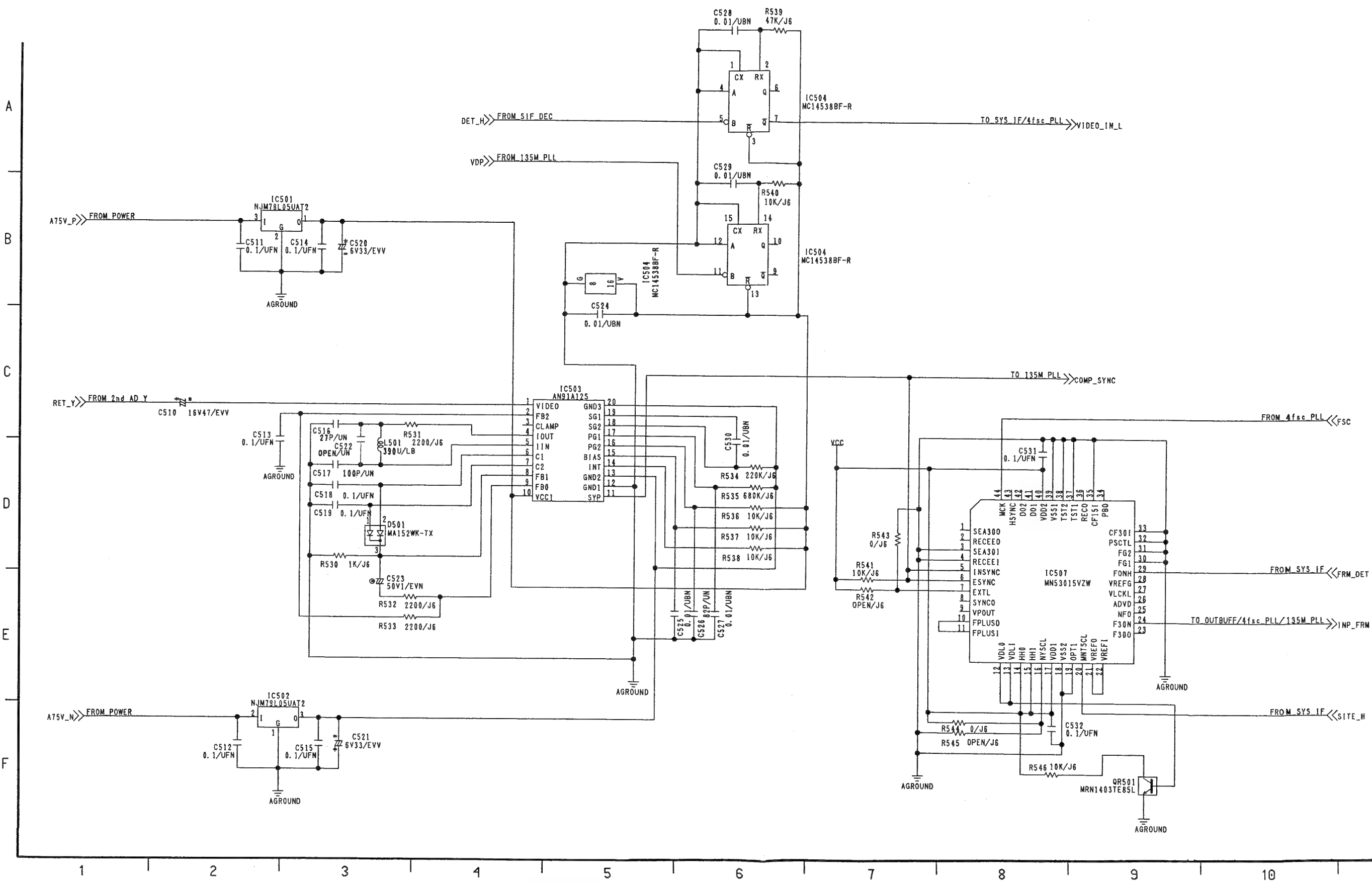
V IN (F6 9/18) 4 fsc PLL SCHEMATIC DIAGRAM



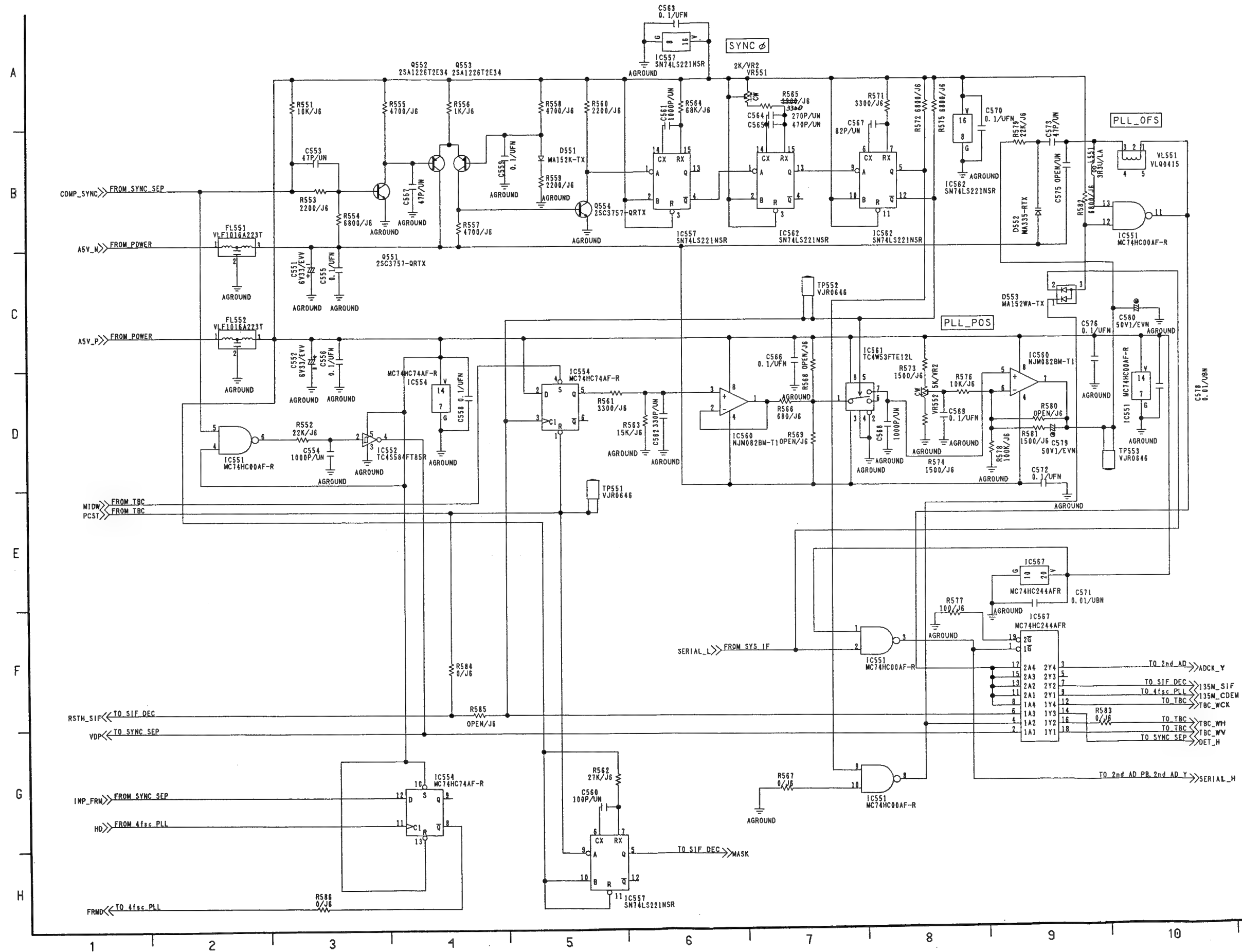
V IN (F6 10/18) C DEM SCHEMATIC DIAGRAM



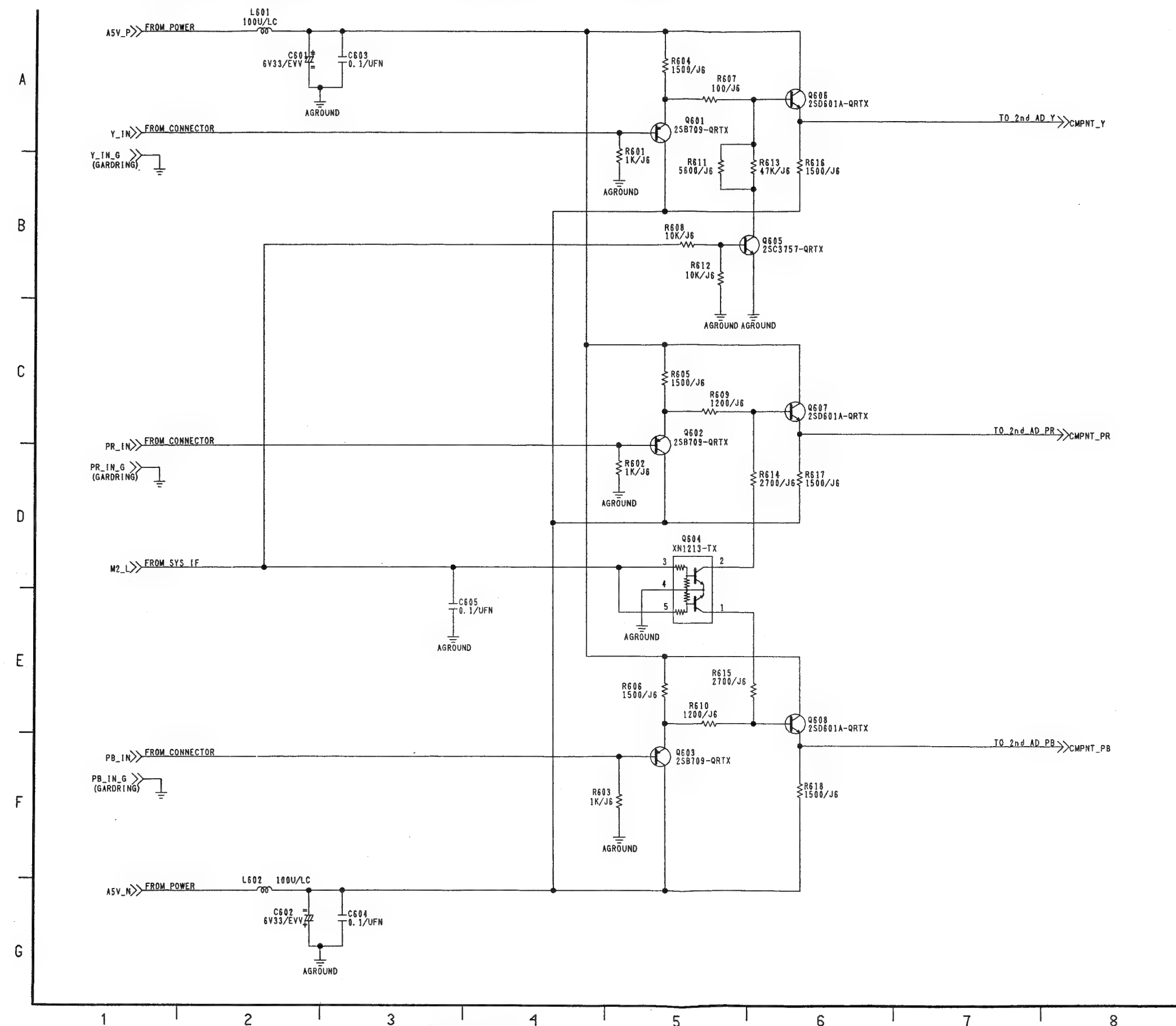
V IN (F6 11/18) SYNC SEP SCHEMATIC DIAGRAM



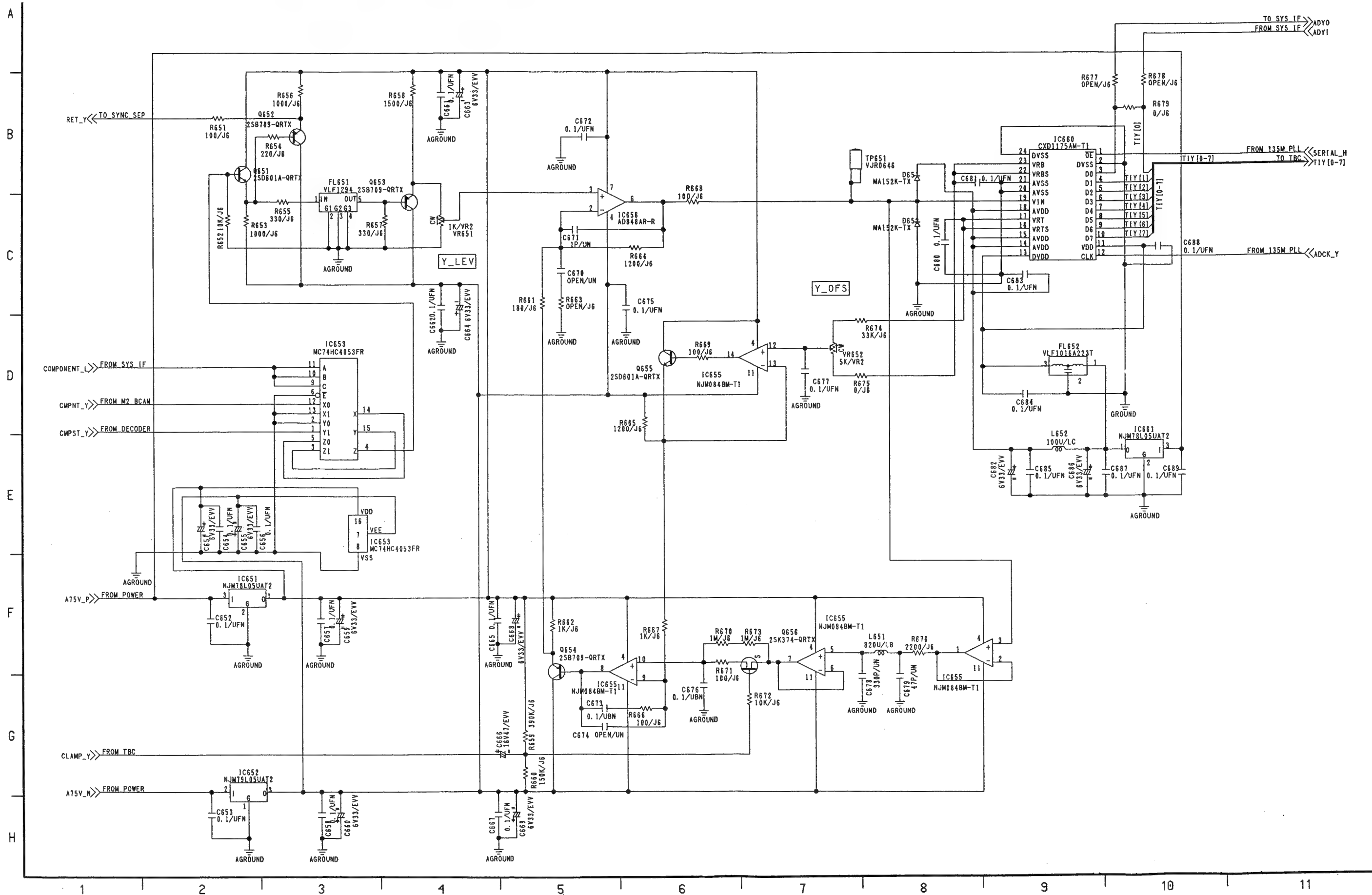
V IN (F6 12/18) 135M PLL SCHEMATIC DIAGRAM



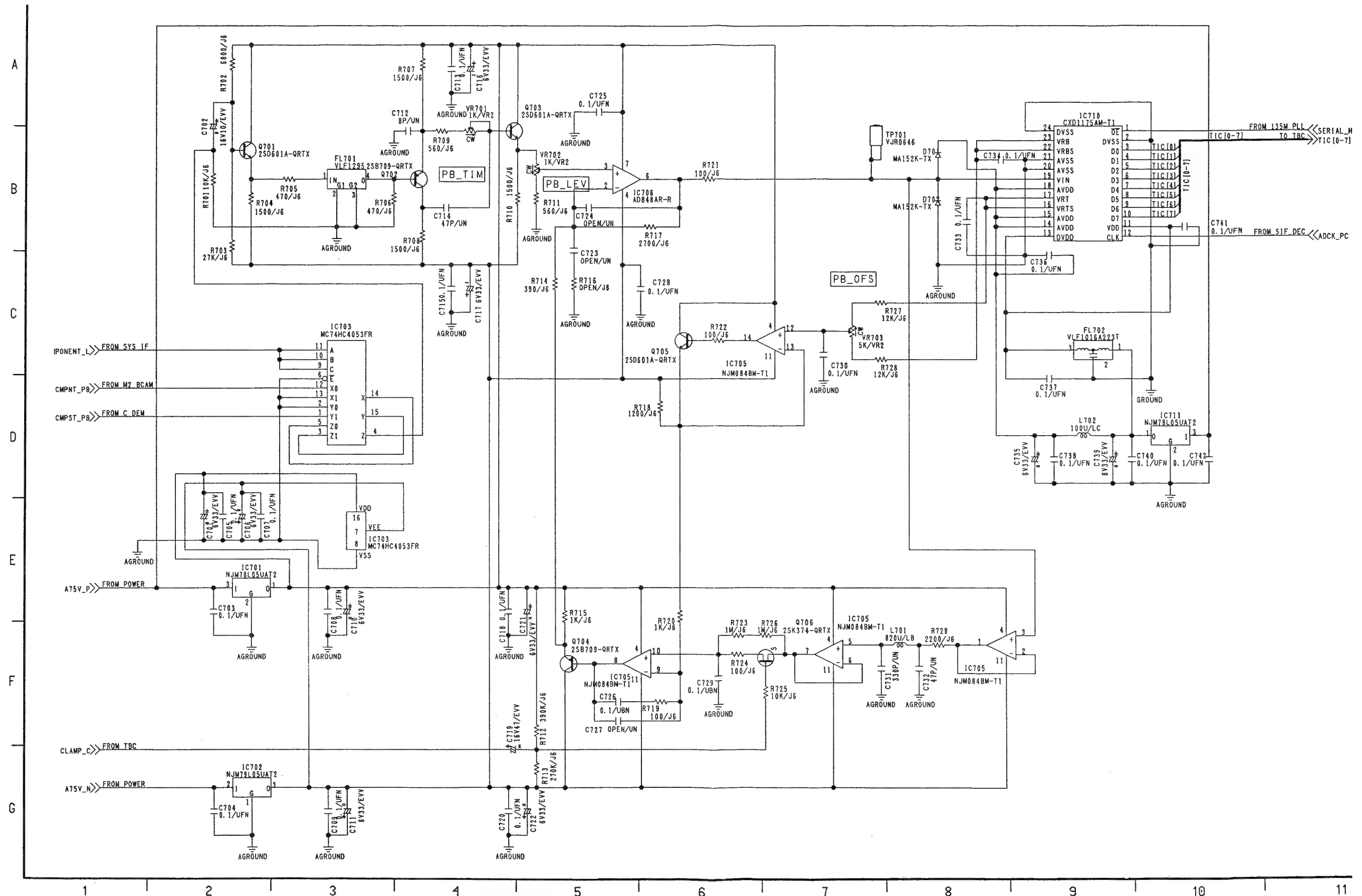
V IN (F6 13/18) M2 BCAM SELECT SCHEMATIC DIAGRAM



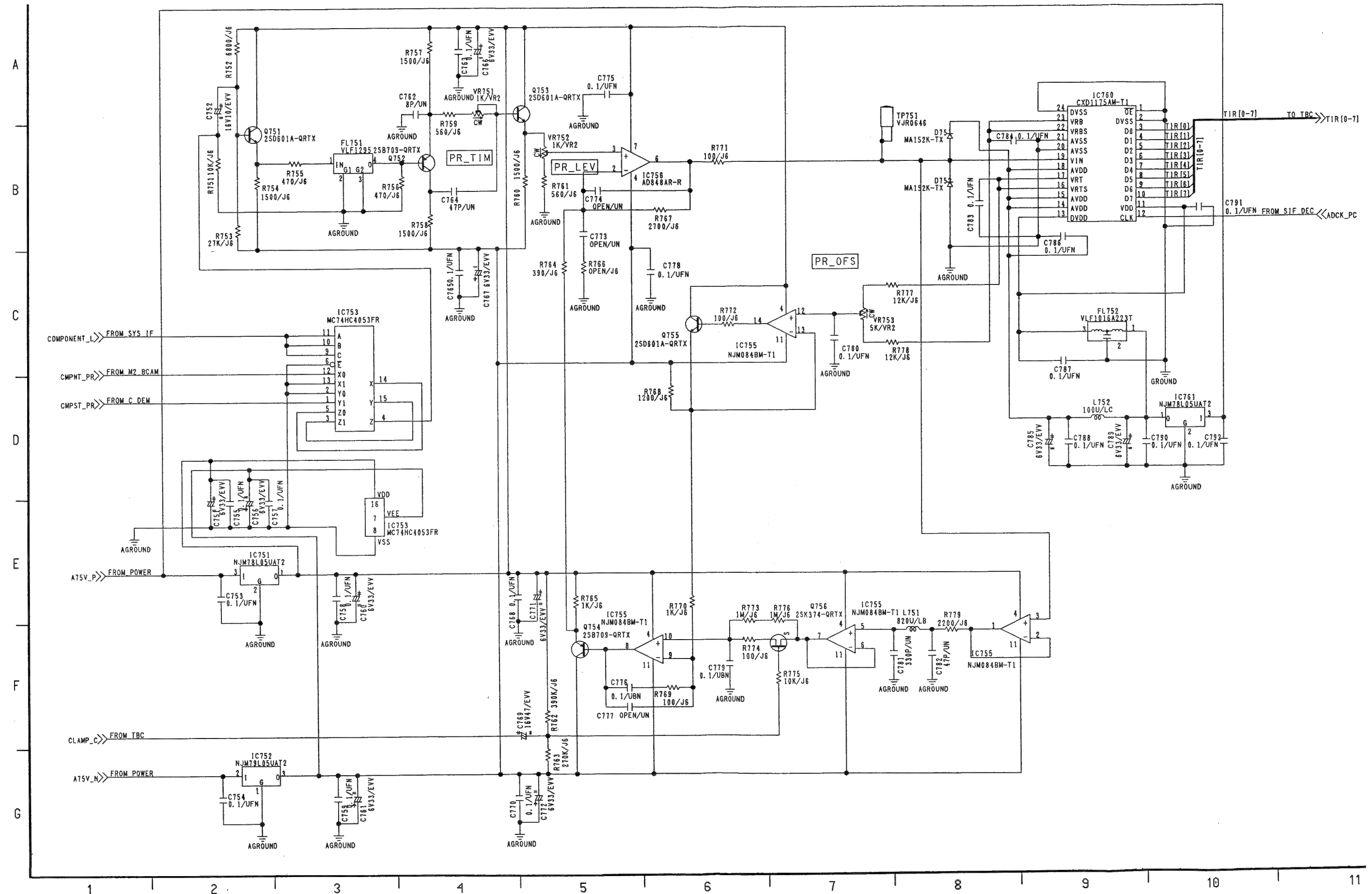
V IN (F6 14/18) 2nd AD Y SCHEMATIC DIAGRAM



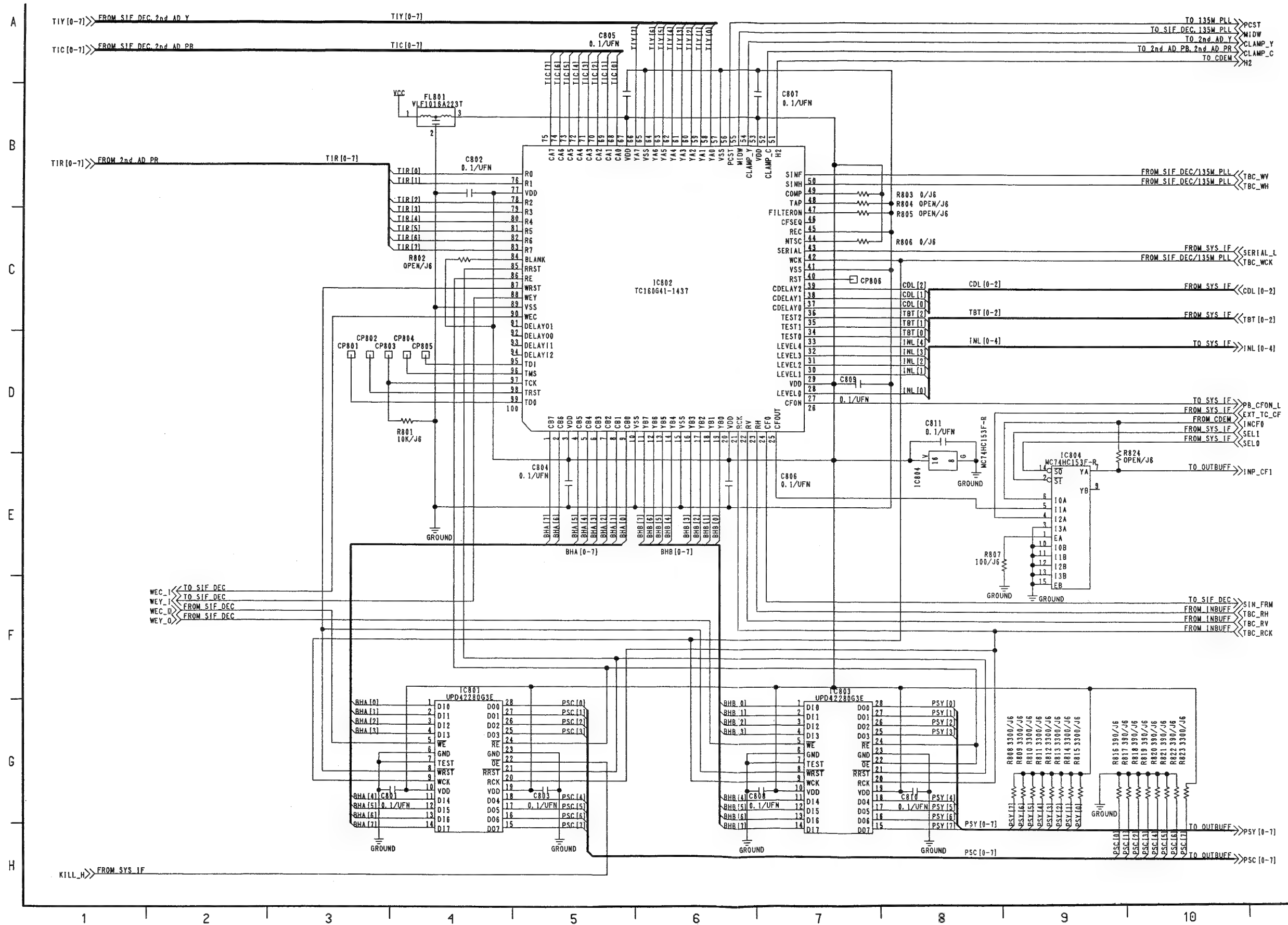
V IN (F6 15/18) 2nd AD PB SCHEMATIC DIAGRAM



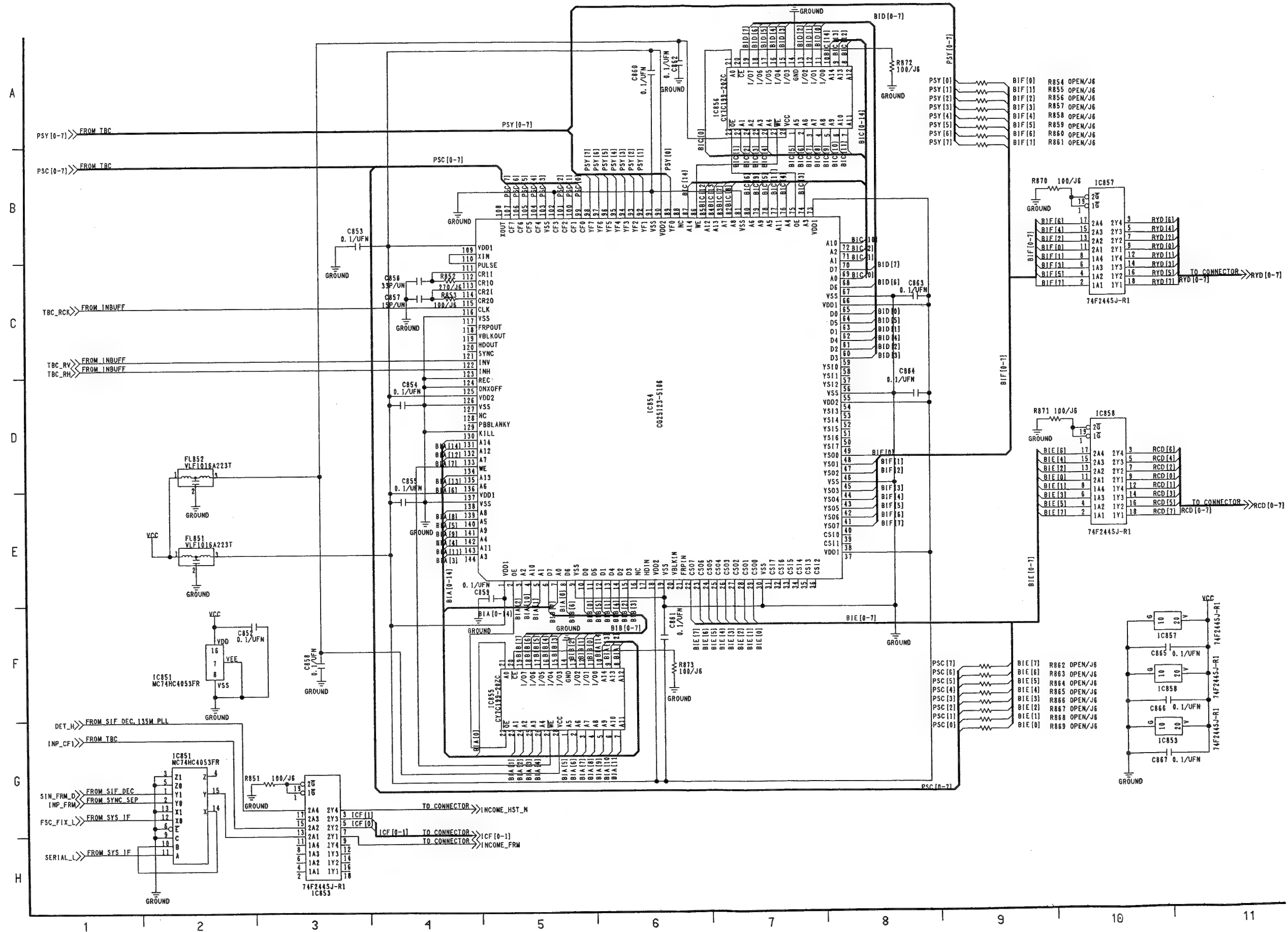
V IN (F6 16/18) 2nd AD PR SCHEMATIC DIAGRAM



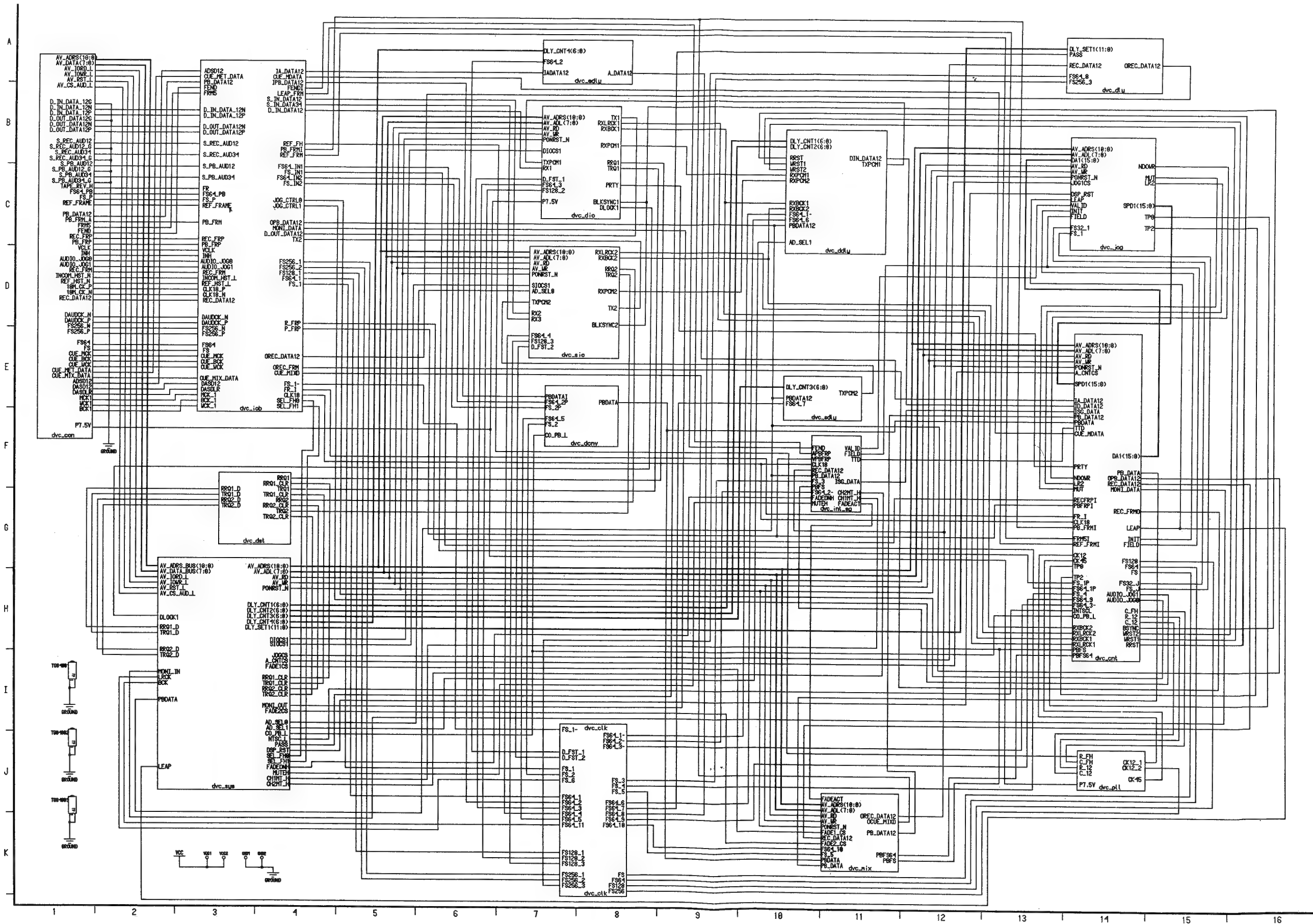
V IN (F6 17/18) TBC SCHEMATIC DIAGRAM



V IN (F6 18/18) OUT BUFF SCHEMATIC DIAGRAM



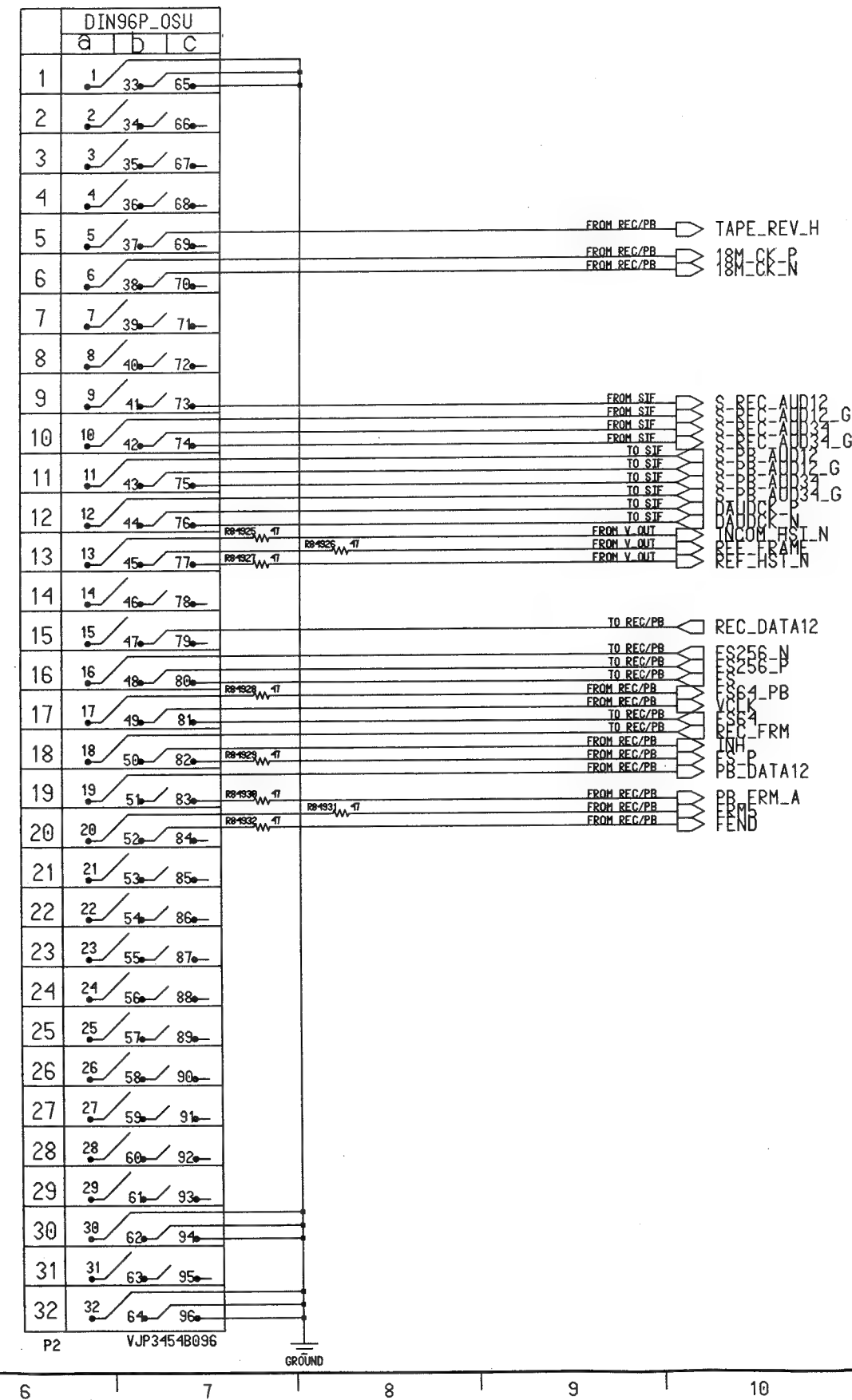
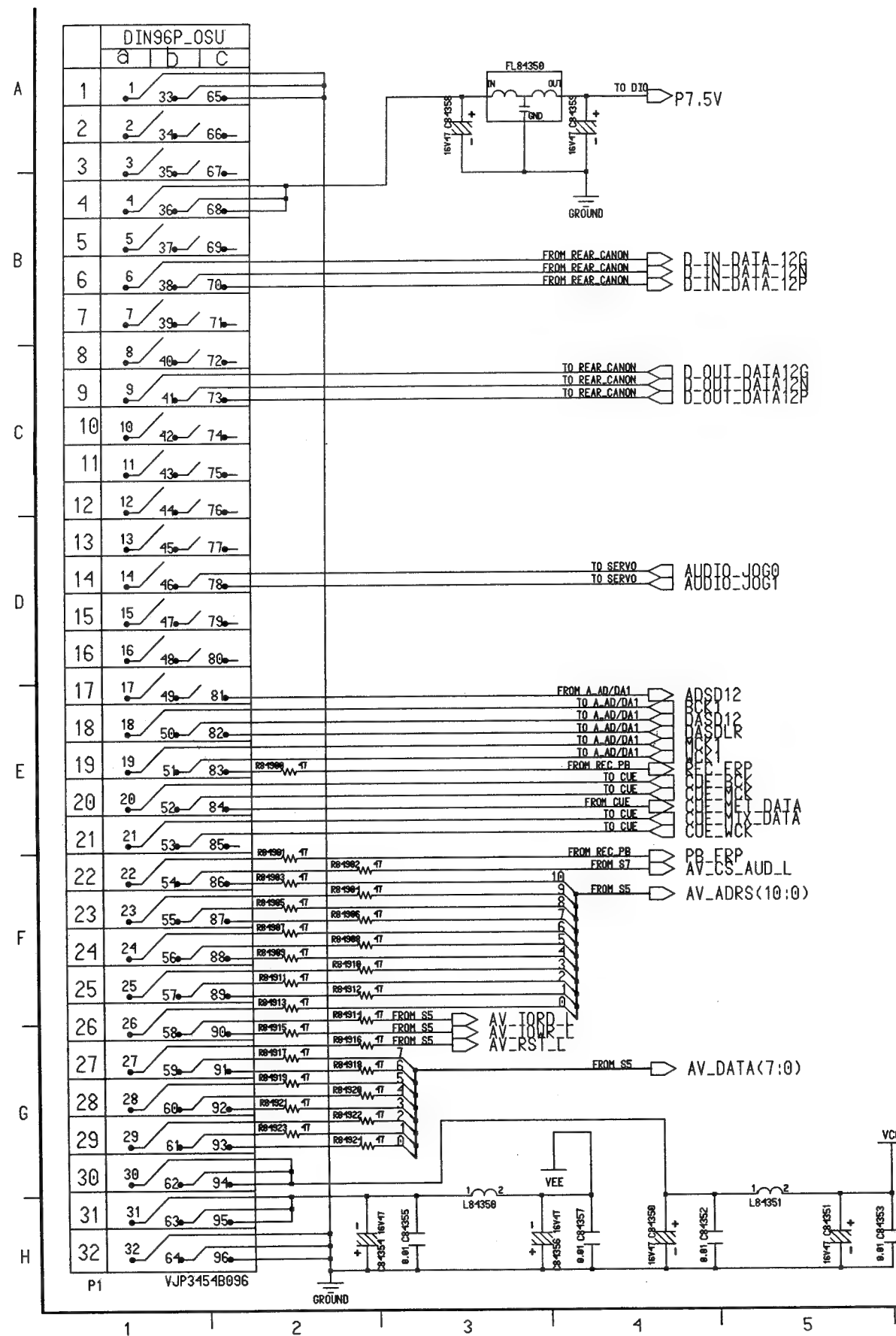
A PROC (F7 1/19) OVERALL SCHEMATIC DIAGRAM



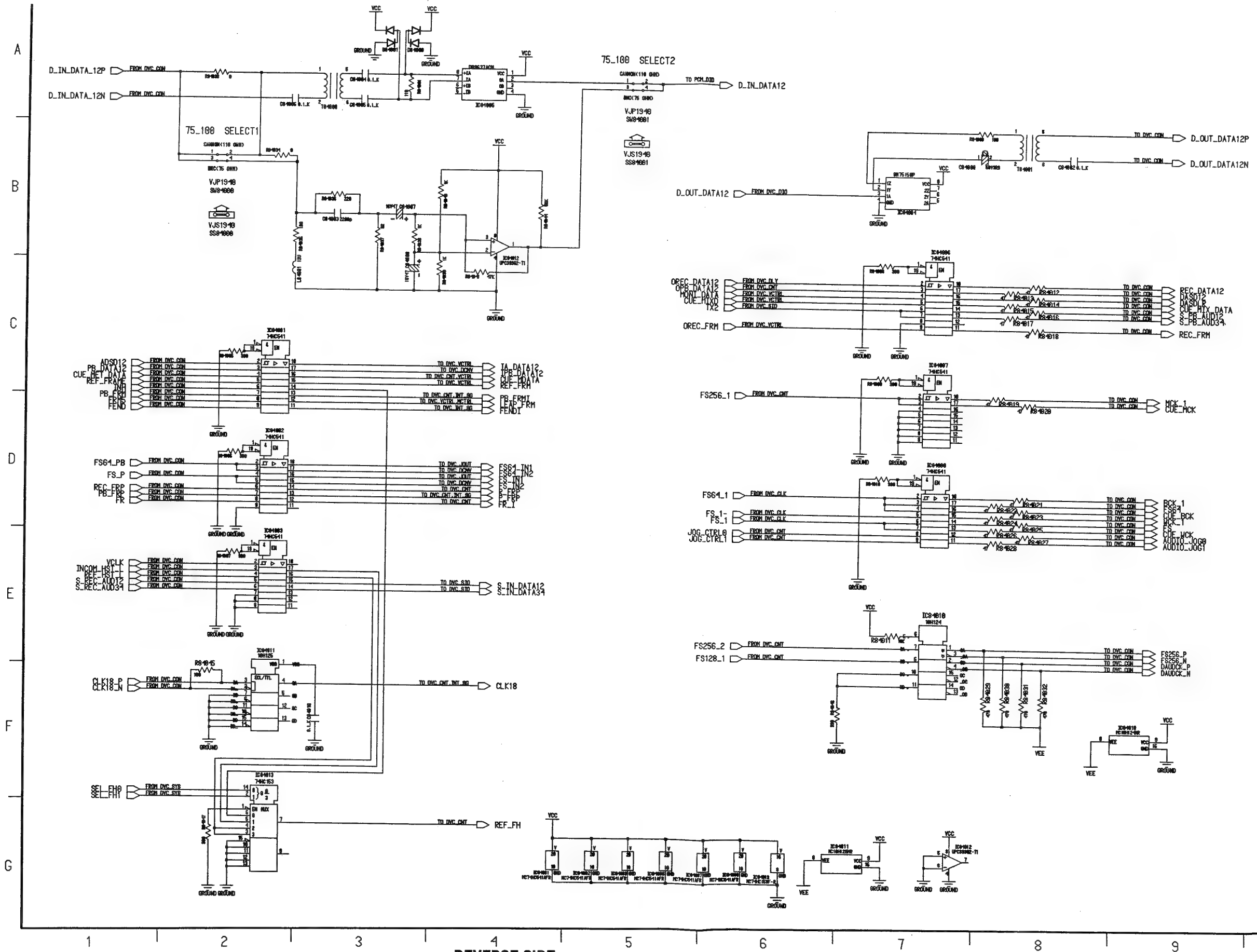
REVERSE SIDE

F6 V IN 18/18

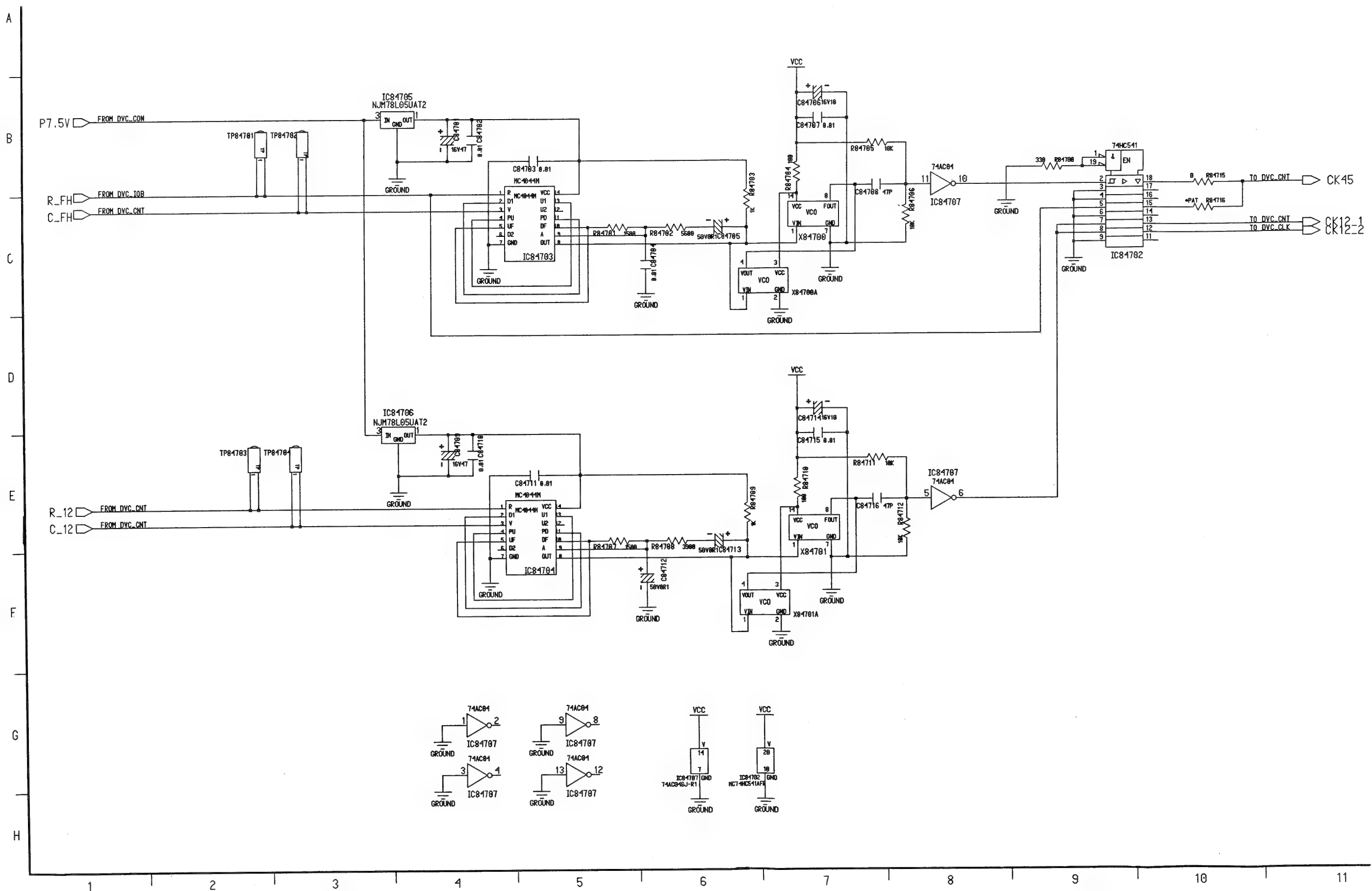
A PROC (F7 2/19) CONNECTOR SCHEMATIC DIAGRAM



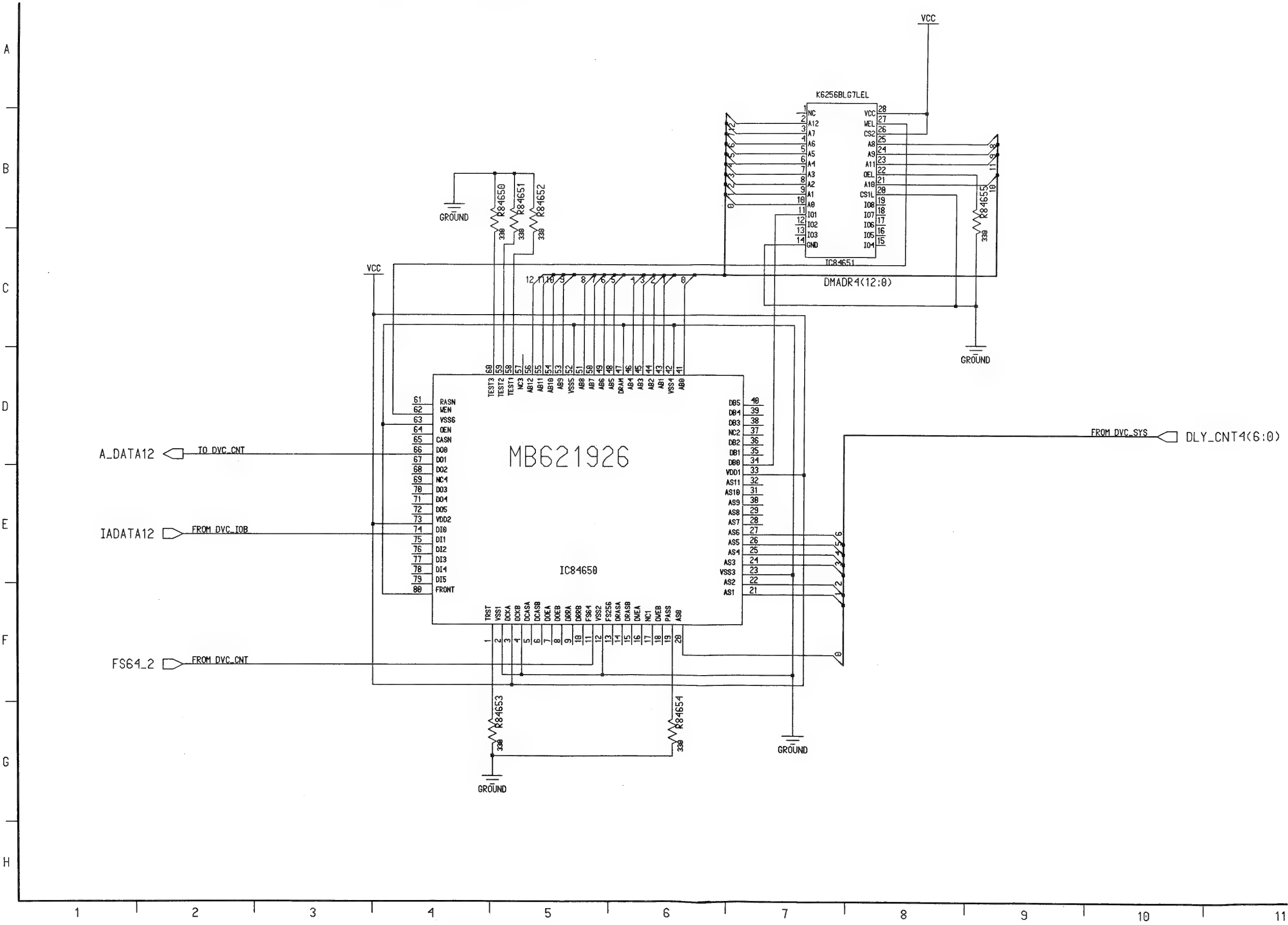
A PROC (F7 3/19) DVC IOB SCHEMATIC DIAGRAM



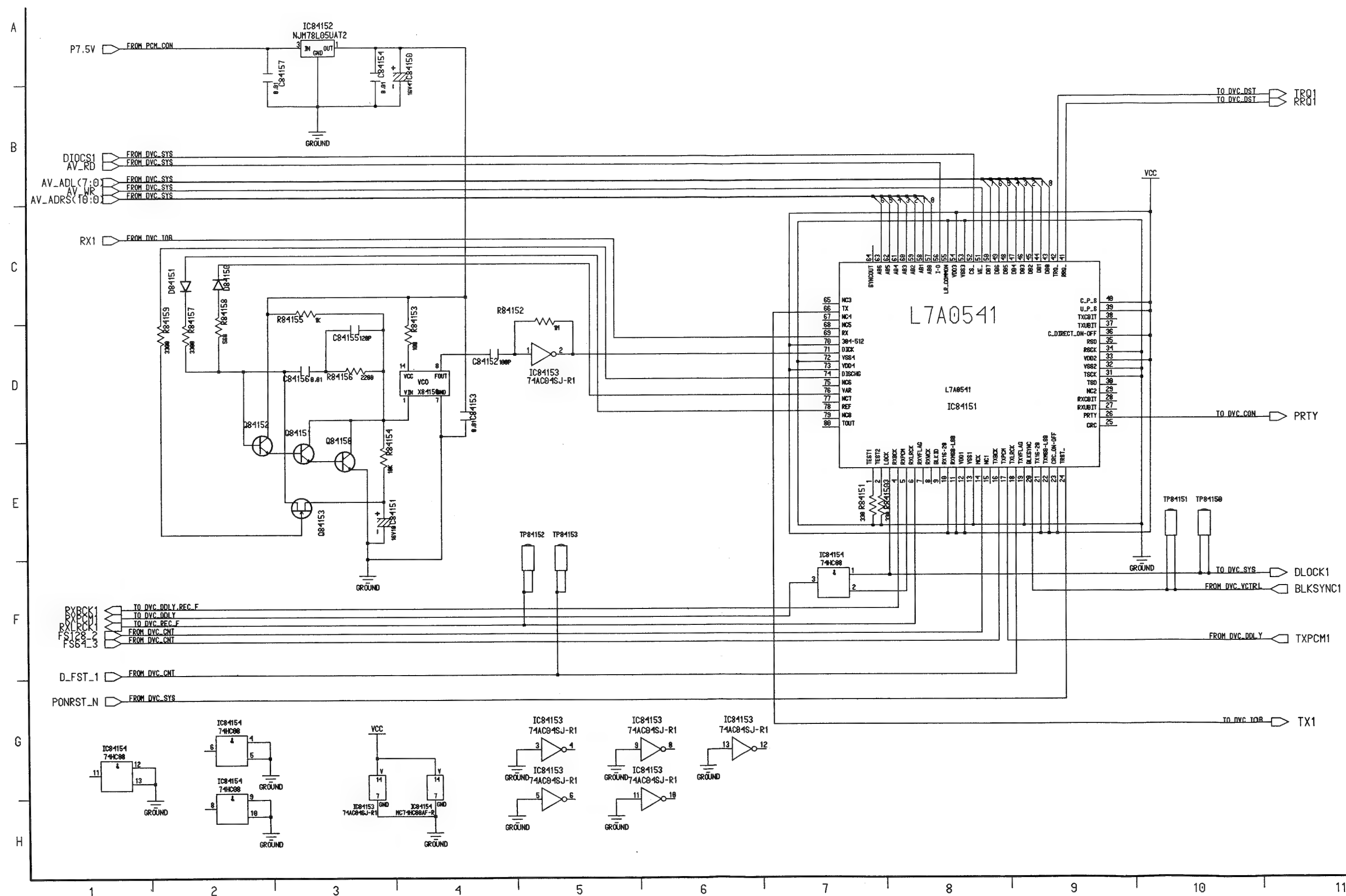
A PROC (F7 4/19) DVC PLL SCHEMATIC DIAGRAM



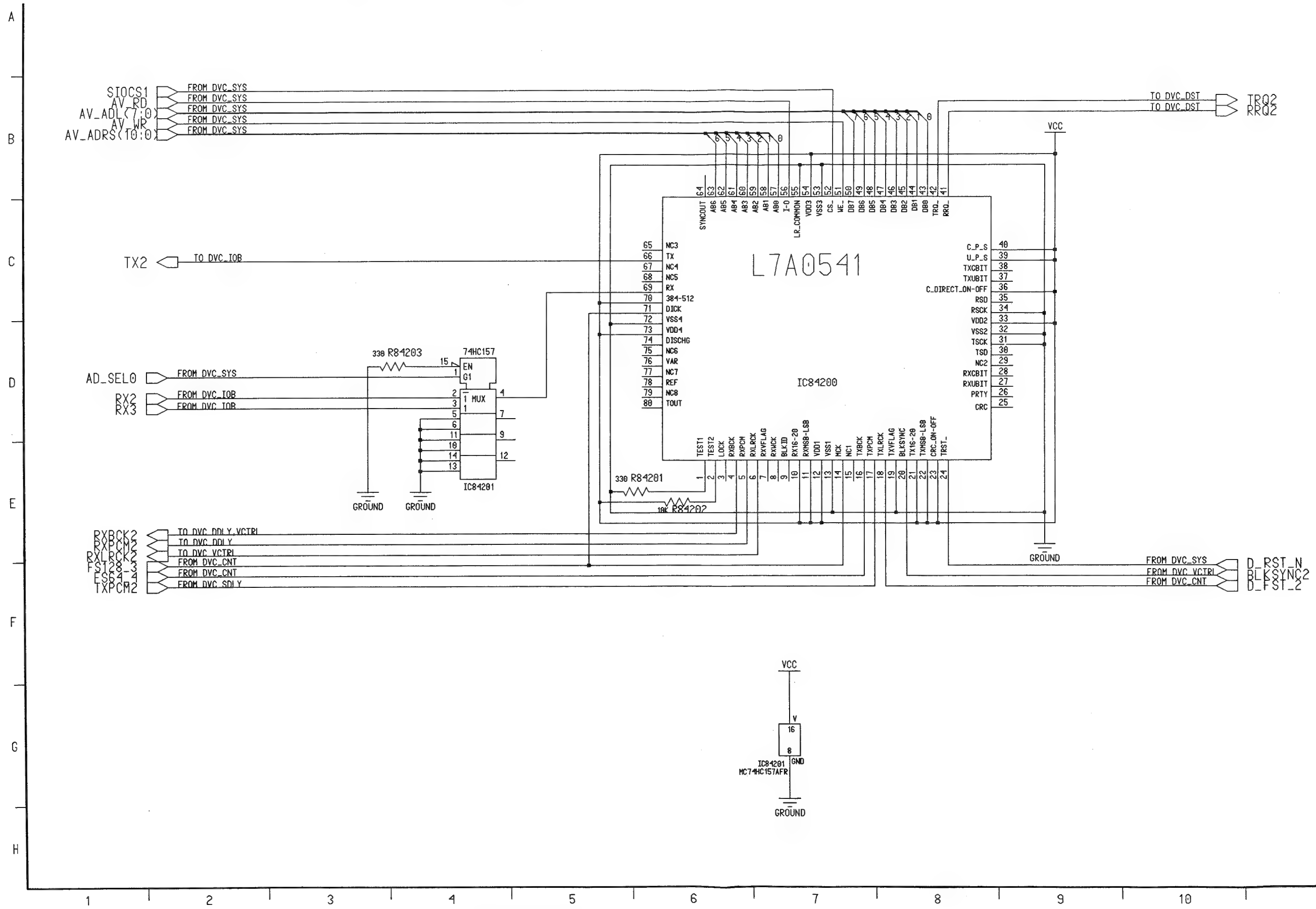
A PROC (F7 5/19) DVC ADLY SCHEMATIC DIAGRAM



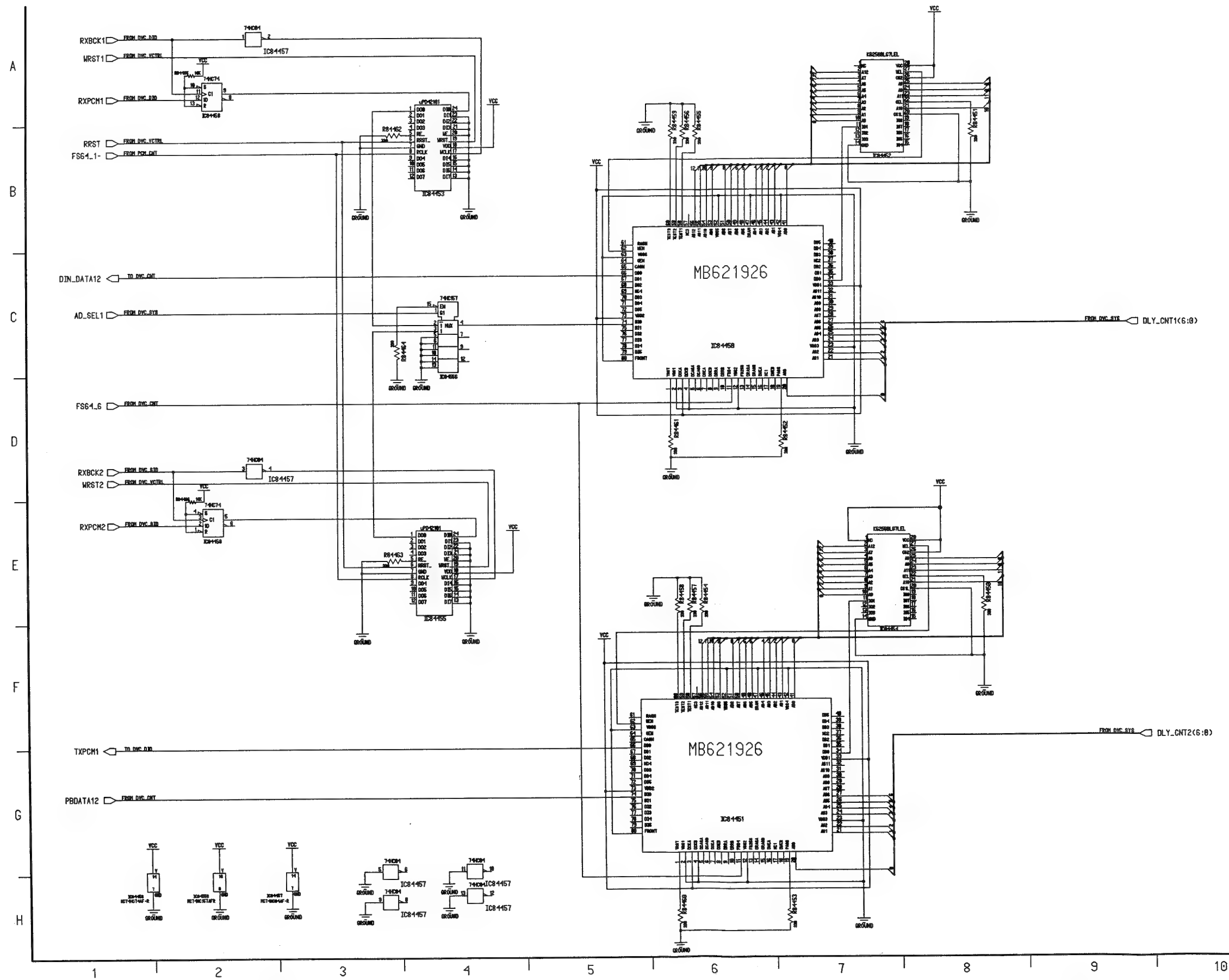
A PROC (F7 6/19) DVC DIO SCHEMATIC DIAGRAM



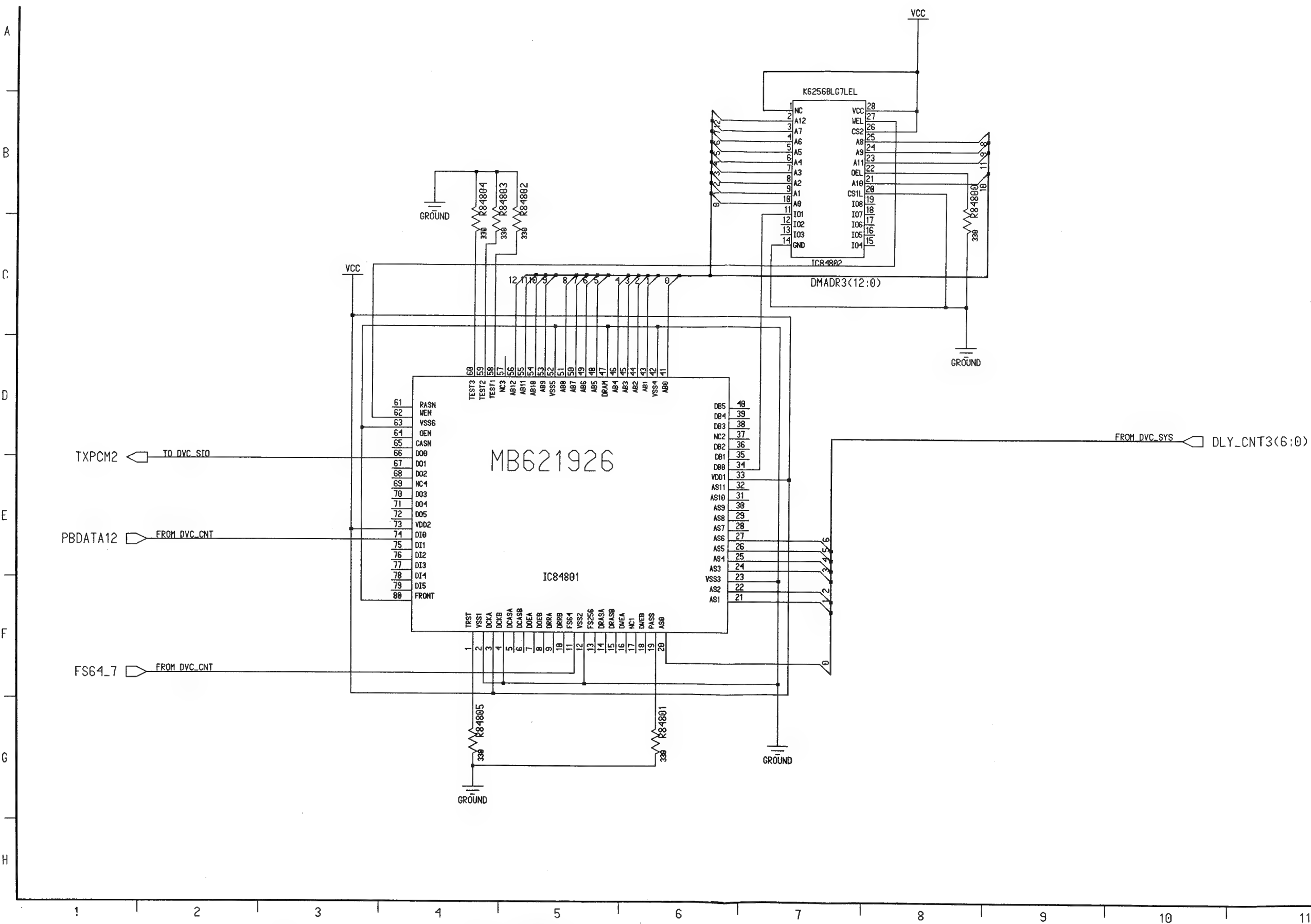
A PROC (F7 7/19) DVC SIO SCHEMATIC DIAGRAM



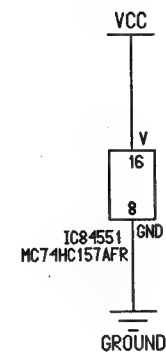
A PROC (F7 8/19) DVC DDLY SCHEMATIC DIAGRAM



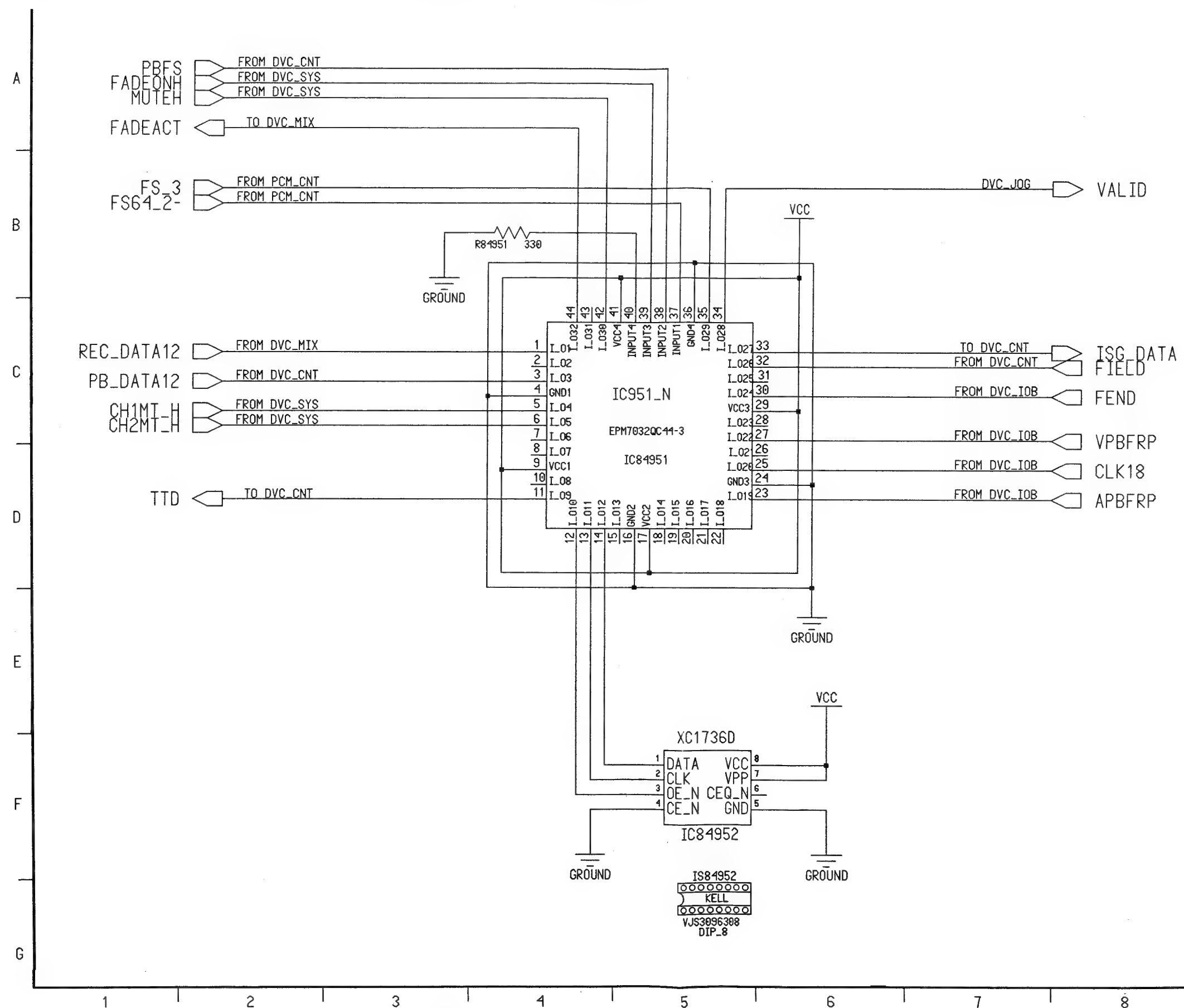
A PROC (F7 9/19) DVC SDLY SCHEMATIC DIAGRAM



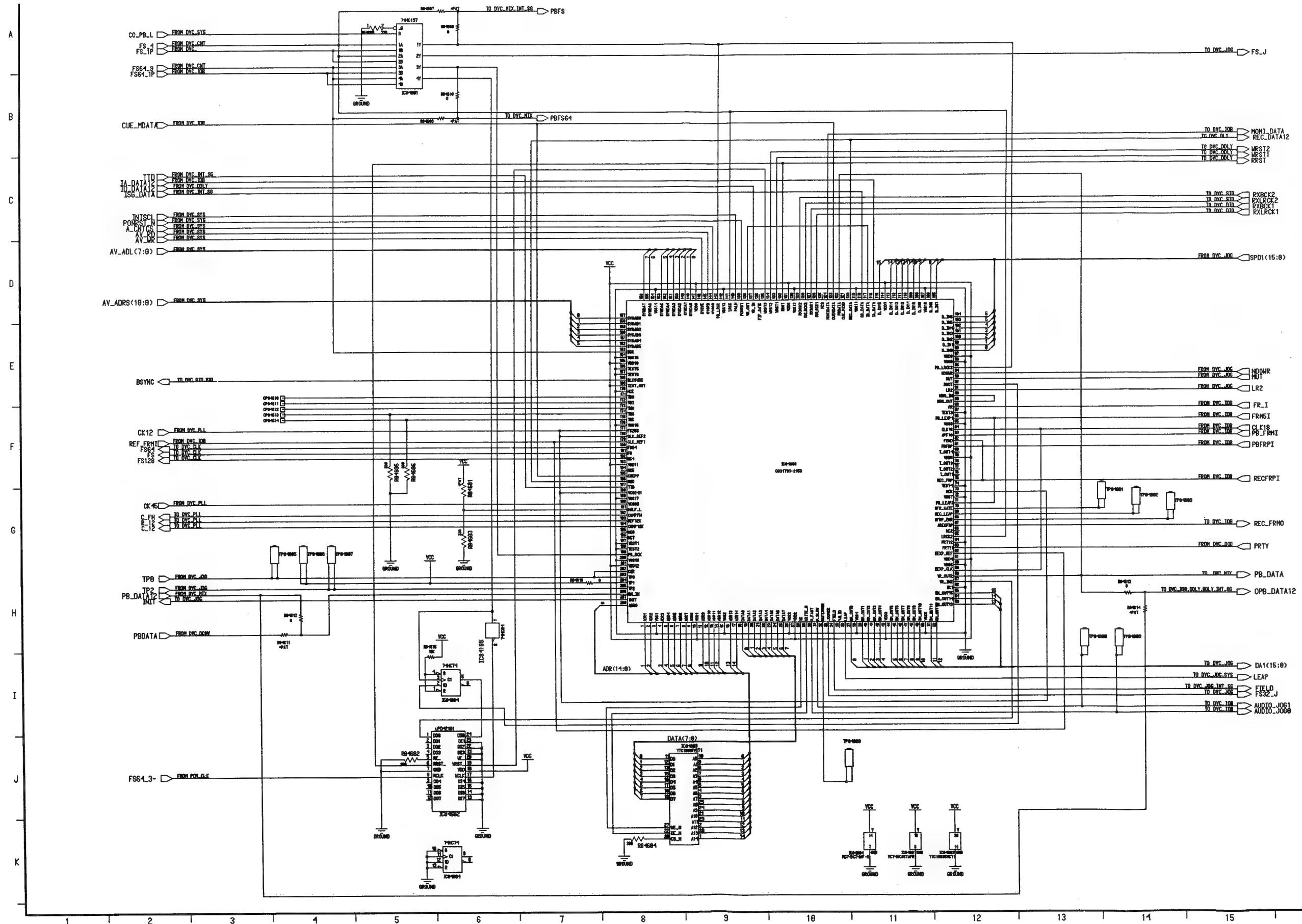
A
—
B
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D
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E
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F
—
G
—
H



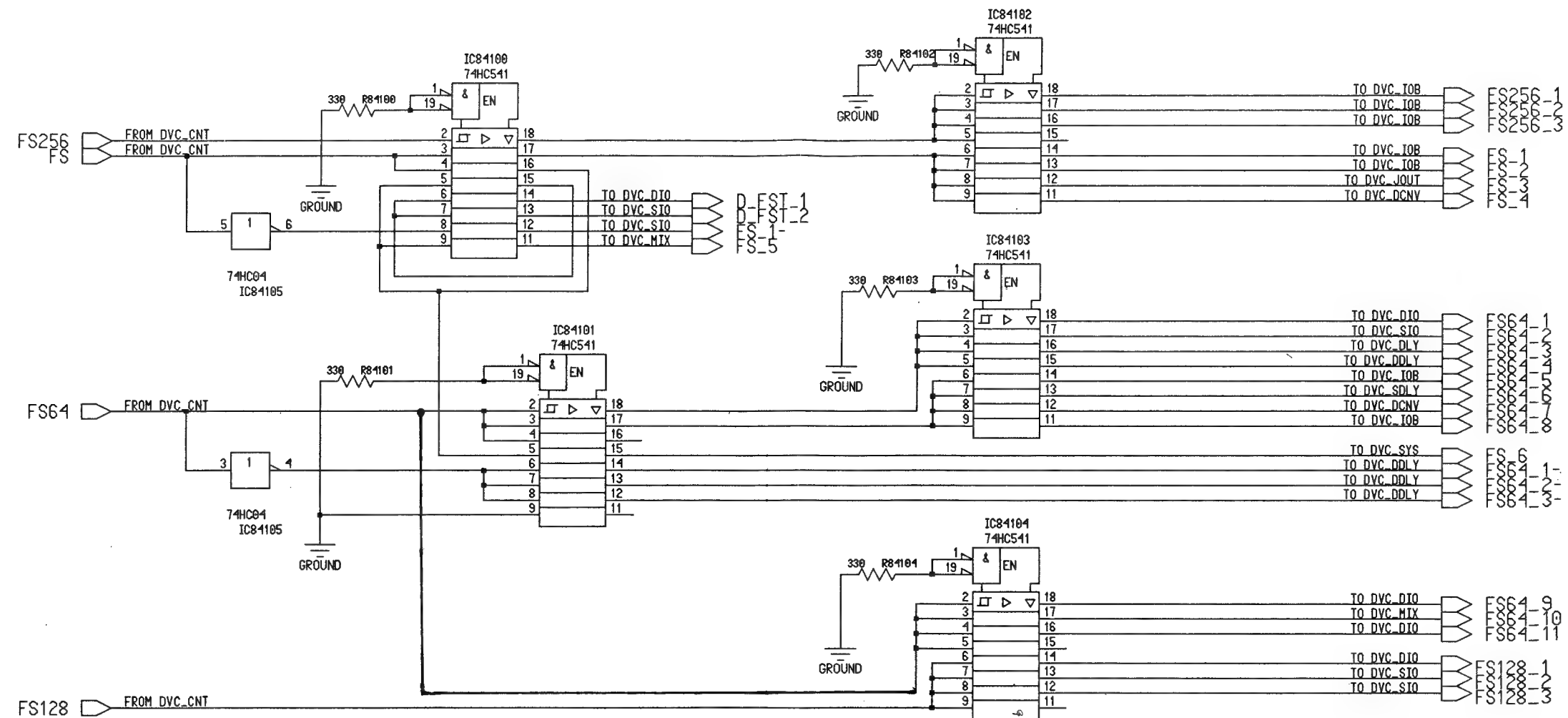
A PROC (F7 11/19) DVC INT SG SCHEMATIC DIAGRAM



A PROC (F7 12/19) DVC CNT SCHEMATIC DIAGRAM



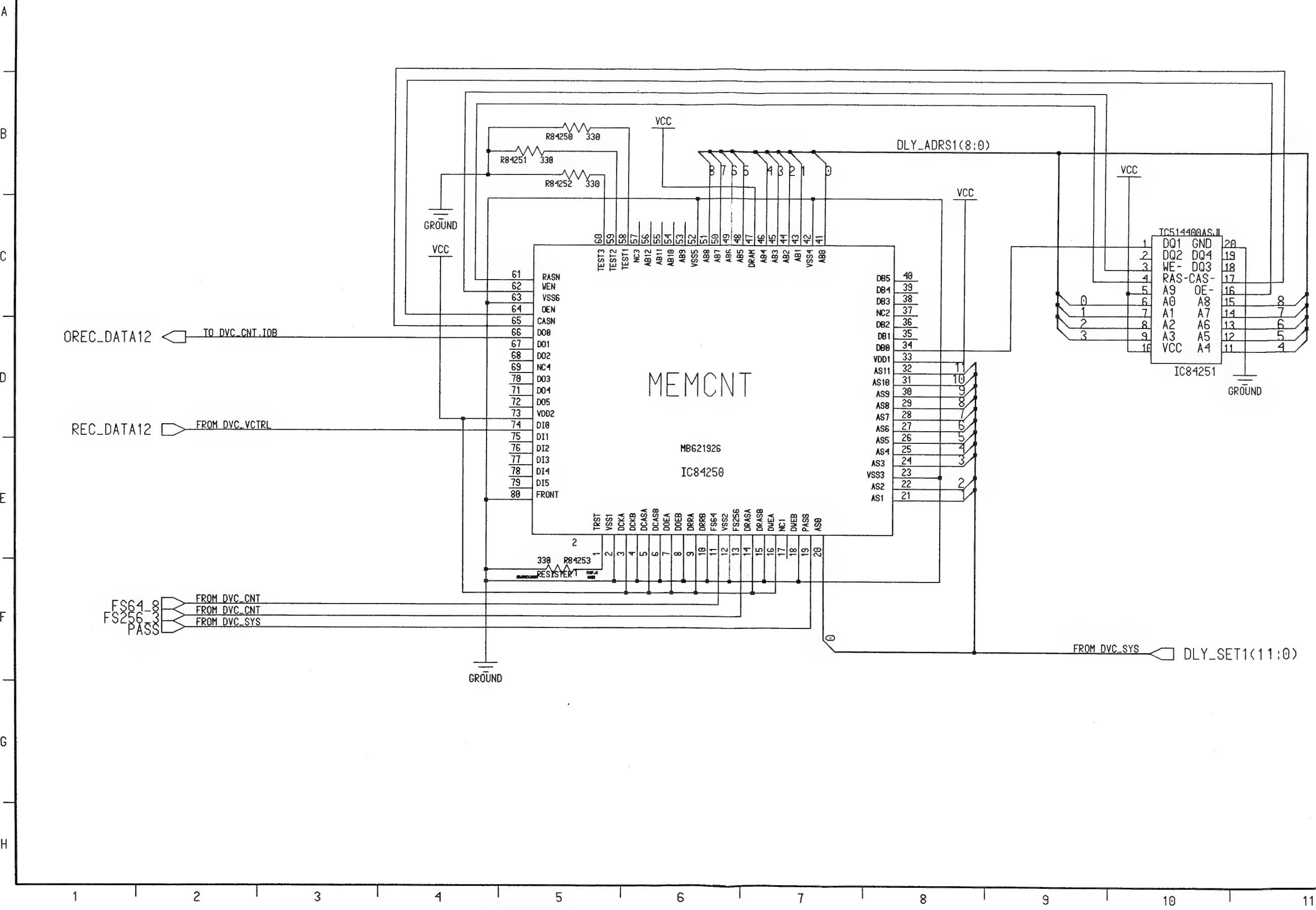
A PROC (F7 13/19) DVC CLK SCHEMATIC DIAGRAM



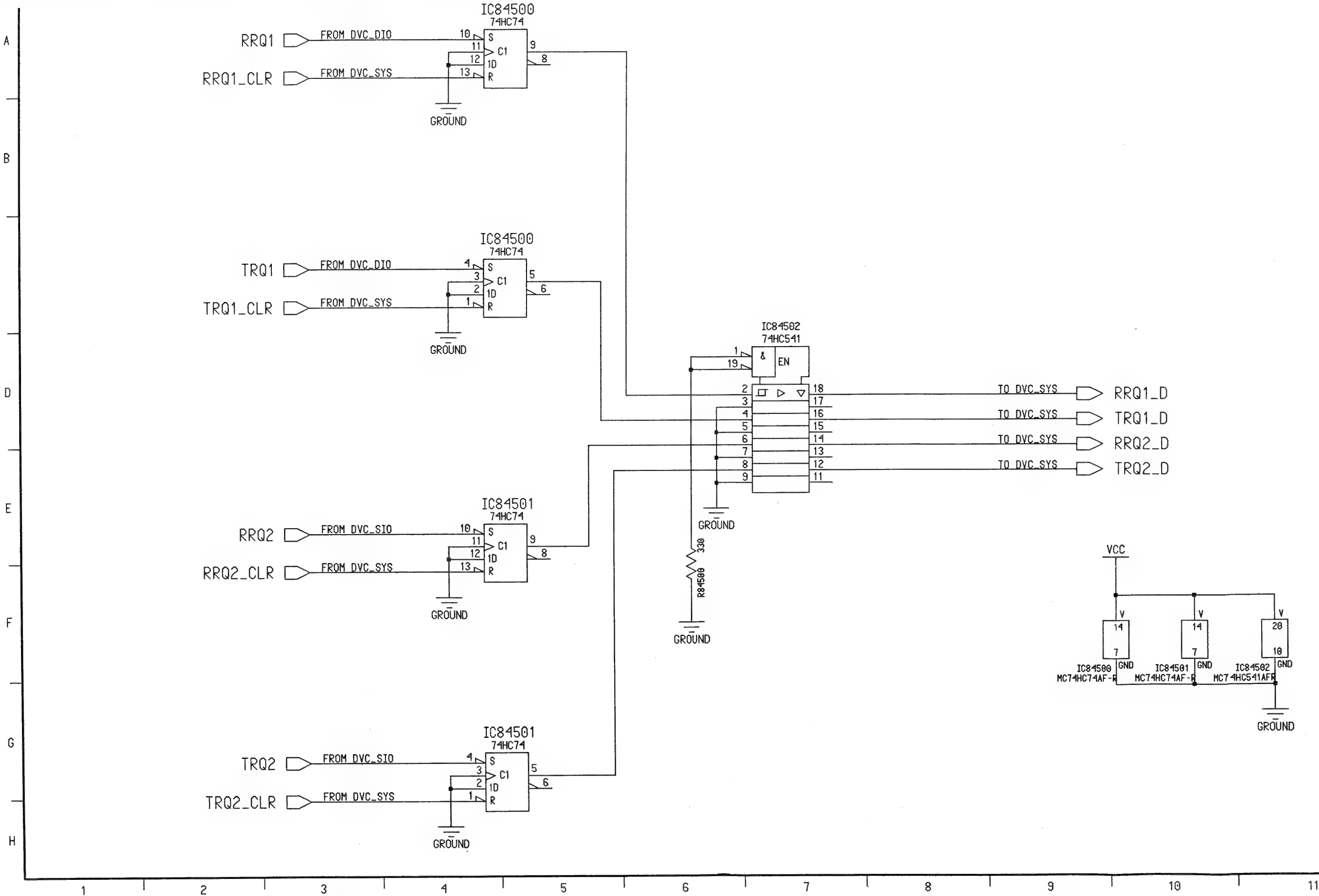
REVERSE SIDE

F7 A PROC 12/19

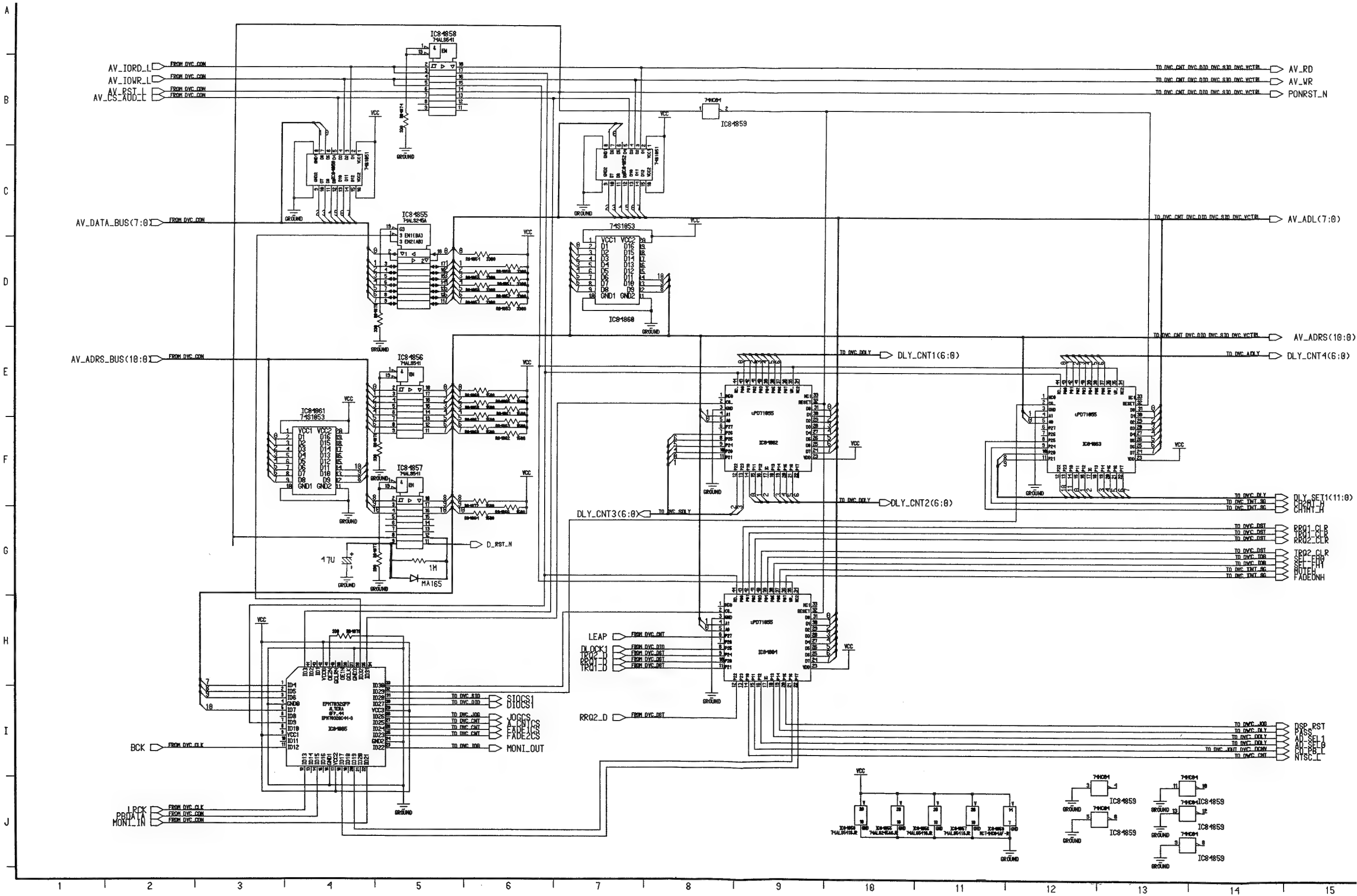
A PROC (F7 15/19) DVC DLY SCHEMATIC DIAGRAM



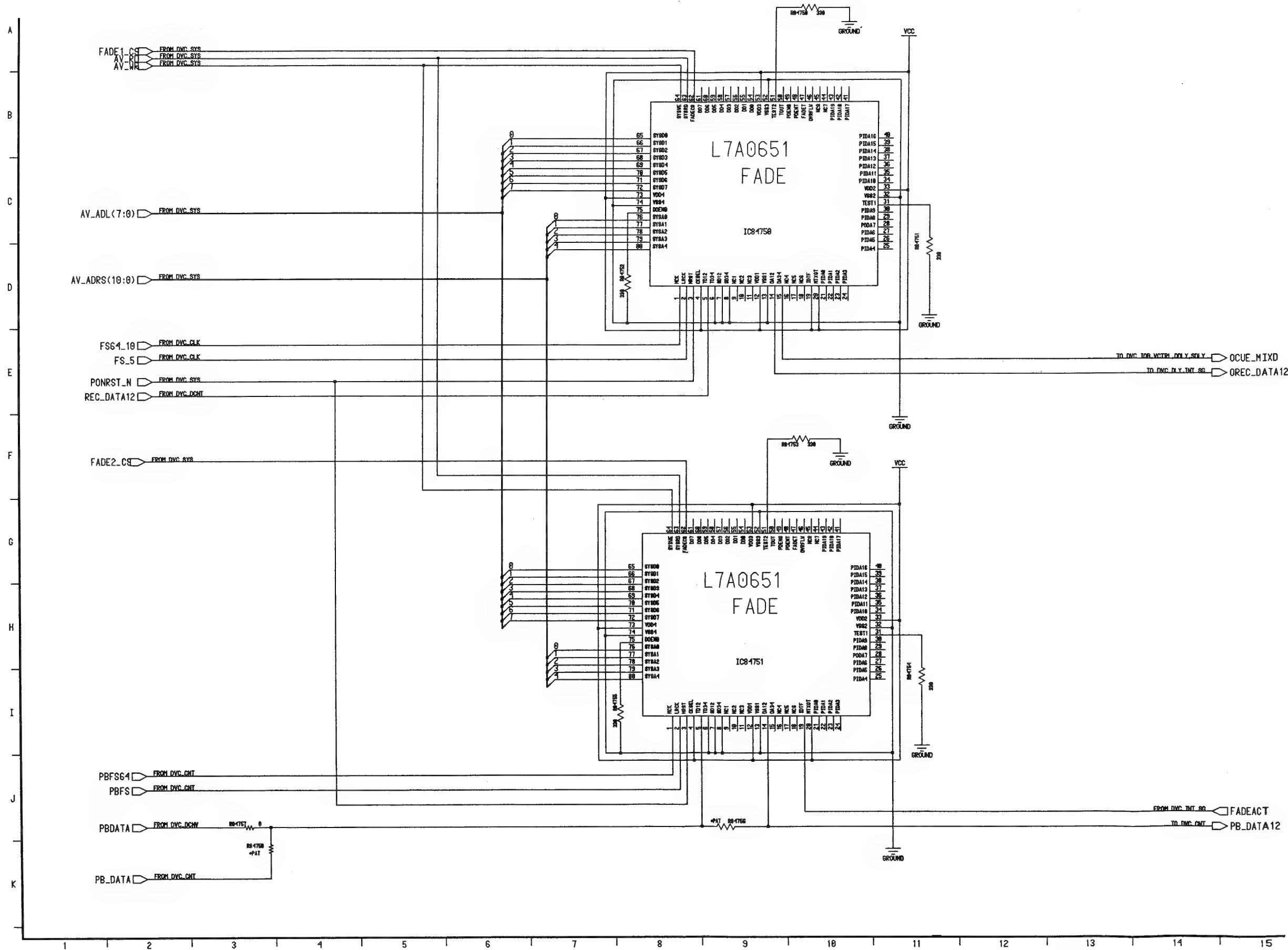
A PROC (F7 16/19) DVC DST SCHEMATIC DIAGRAM



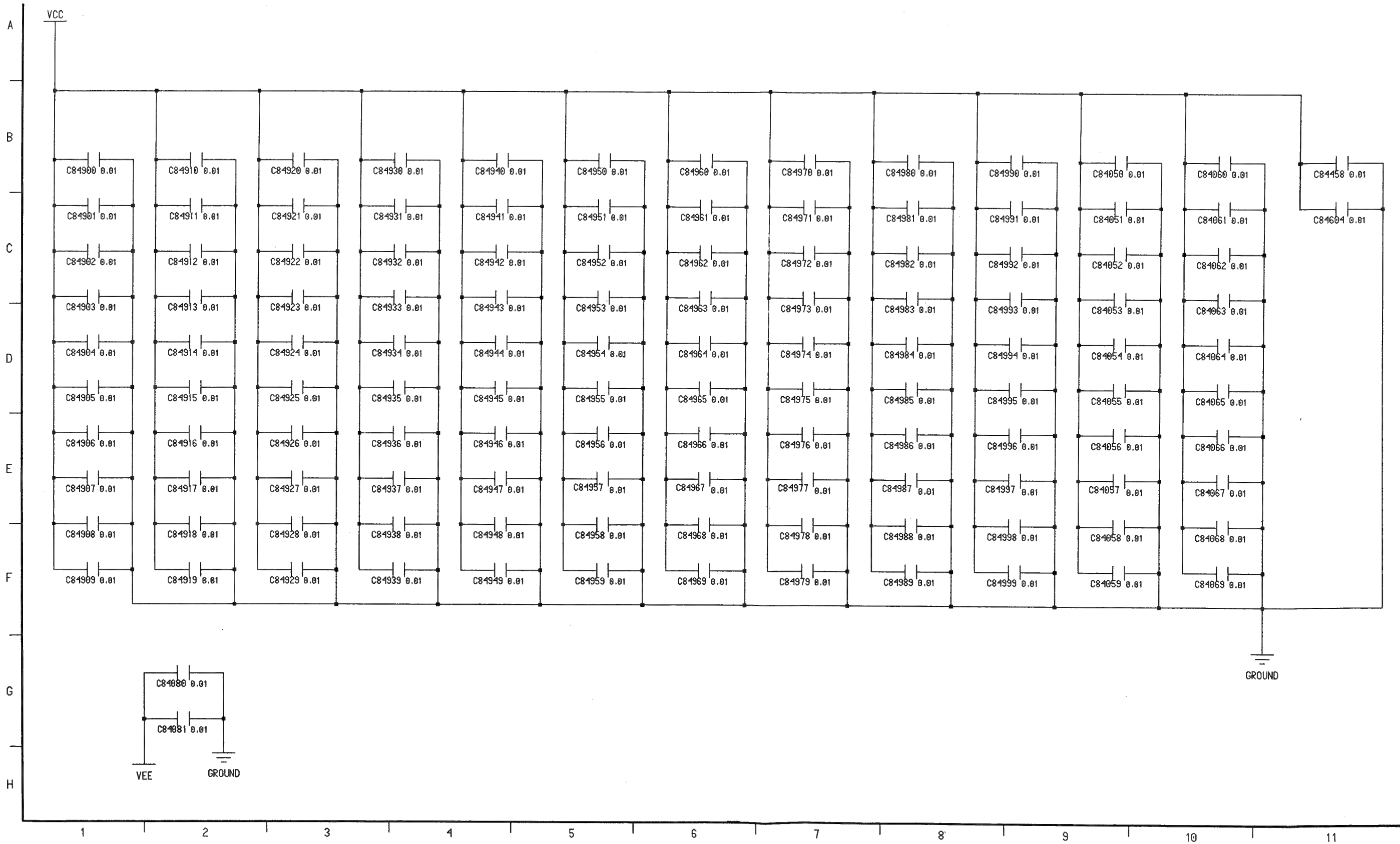
A PROC (F7 17/19) DVC SYS SCHEMATIC DIAGRAM



A PROC (F7 18/19) DVC MIX SCHEMATIC DIAGRAM



A PROC (F7 19/19) PASSCON SCHEMATIC DIAGRAM

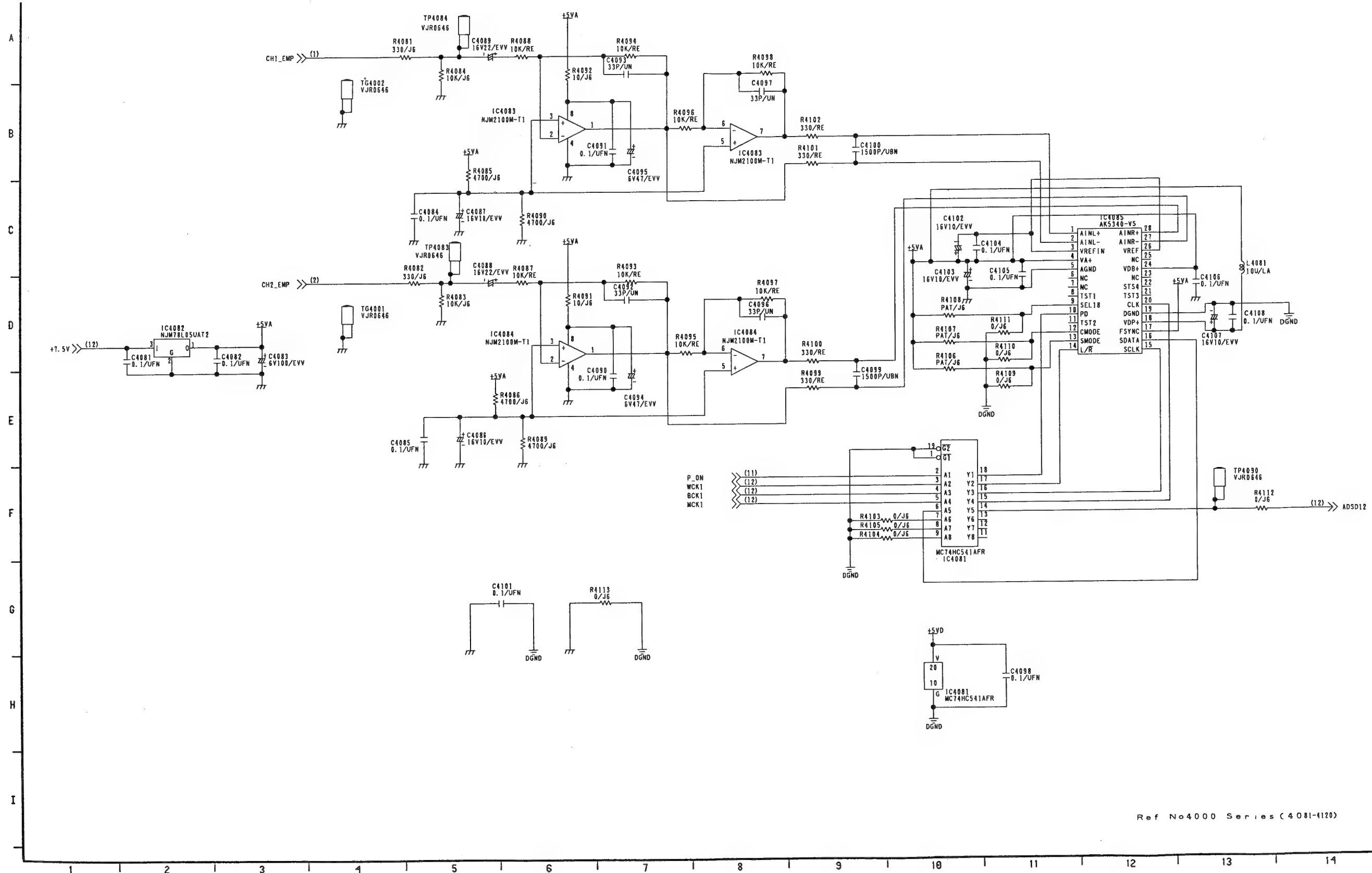


[illegible]

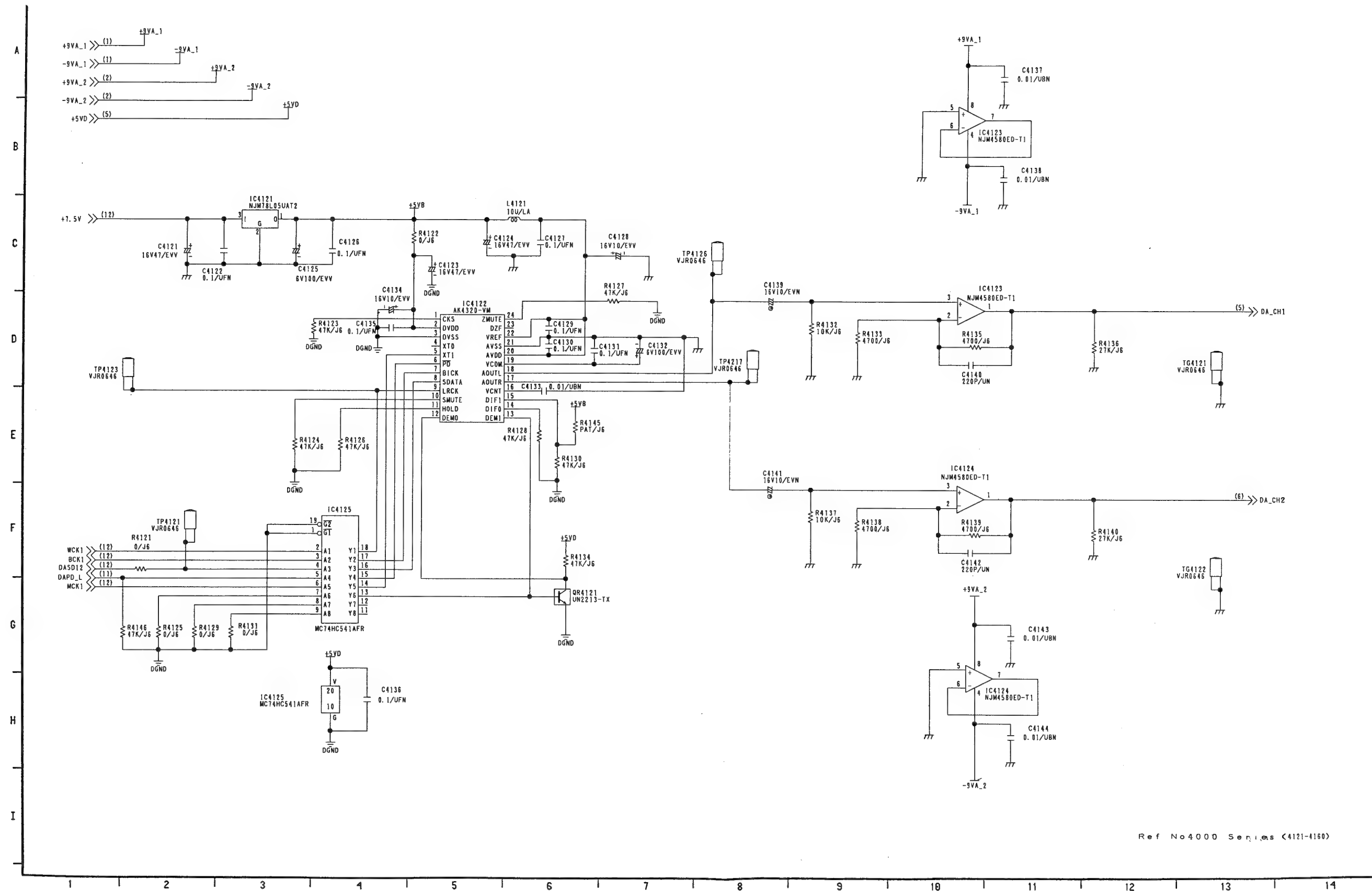
[illegible]

REVERSE SIDE
F8 ADDA 1/12

ADDA (F8 3/12) SCHEMATIC DIAGRAM

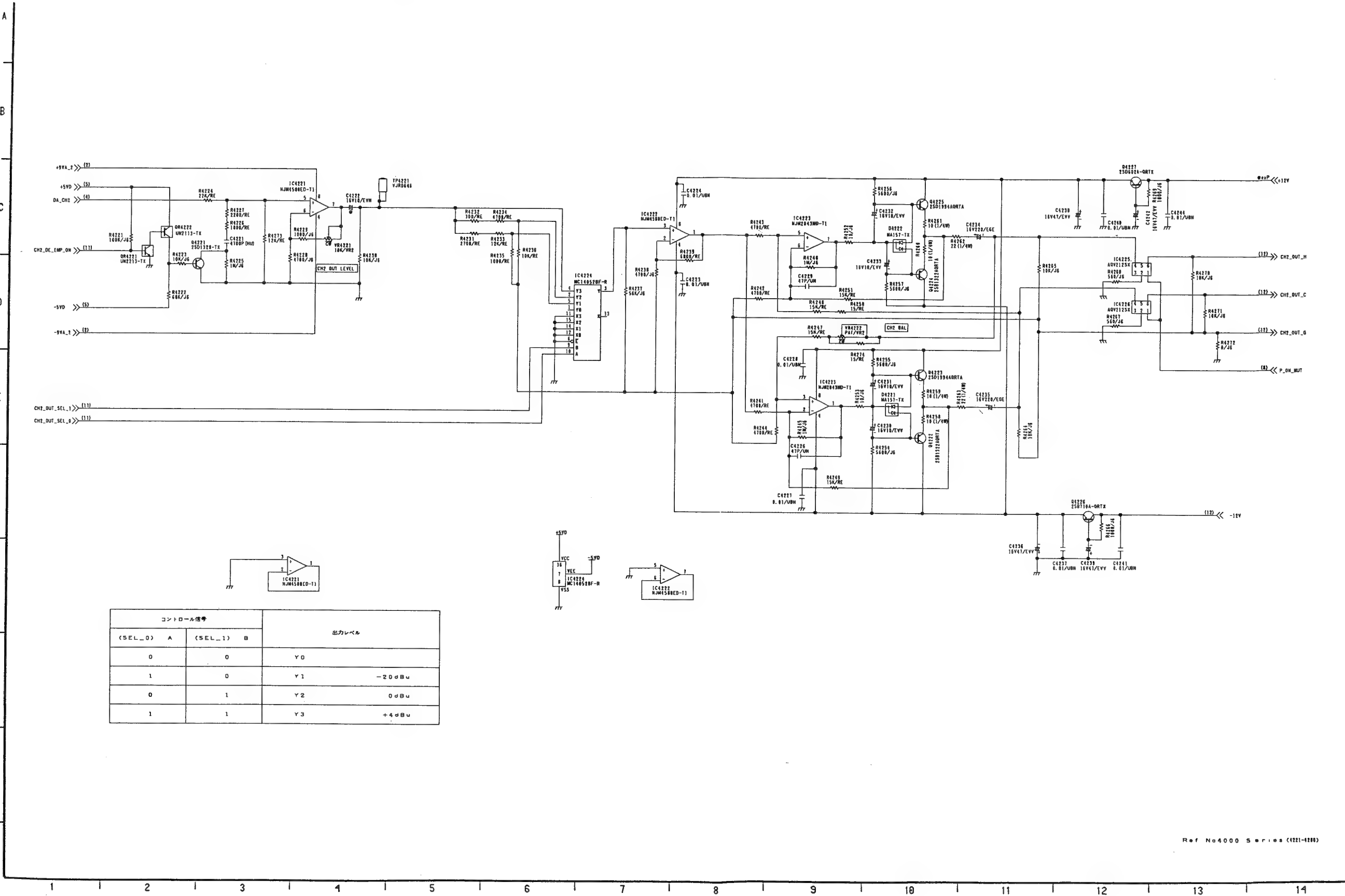


ADDA (F8 4/12) SCHEMATIC DIAGRAM



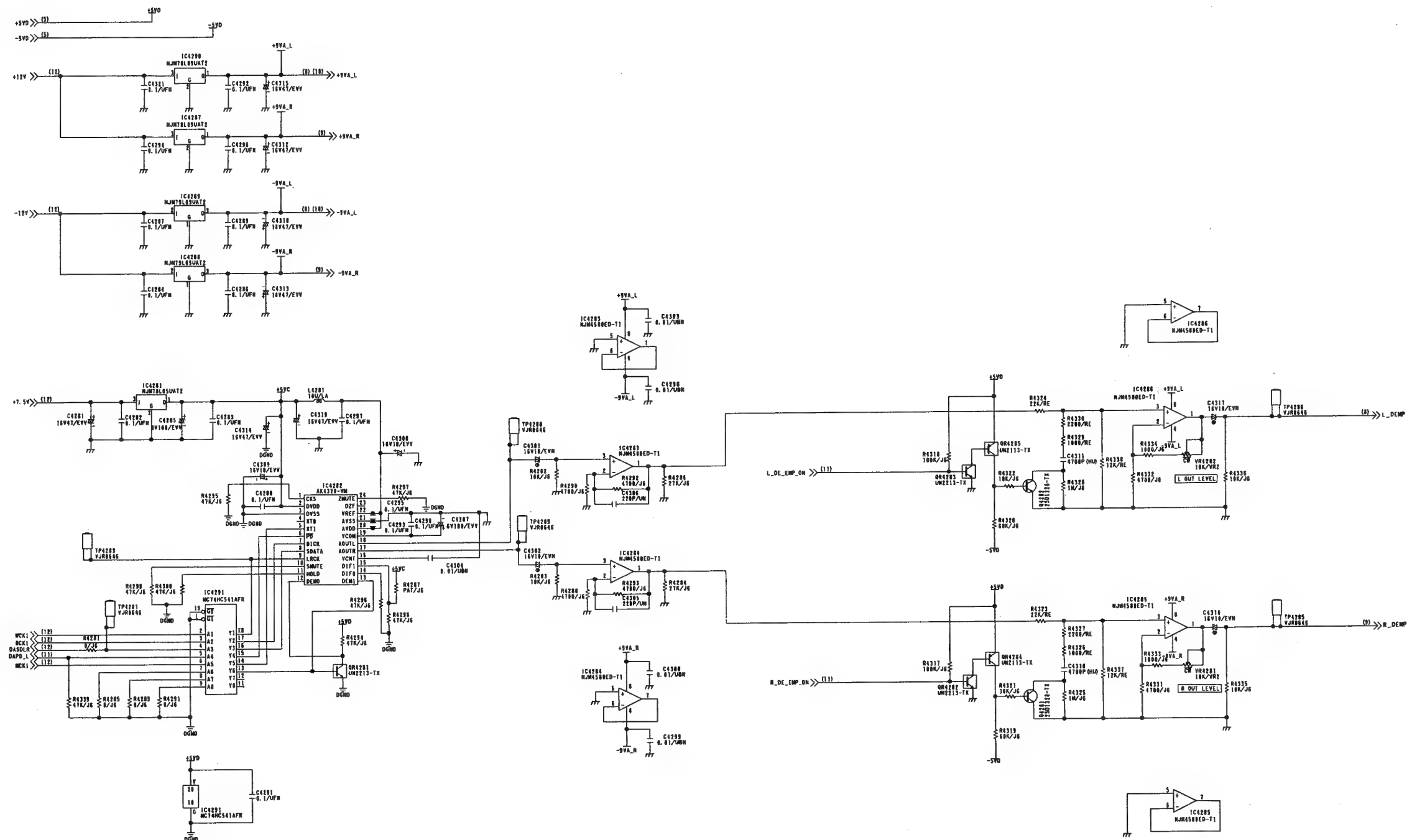
Ref No 4000 Series (4121-4160)

ADDA (F8 6/12) SCHEMATIC DIAGRAM



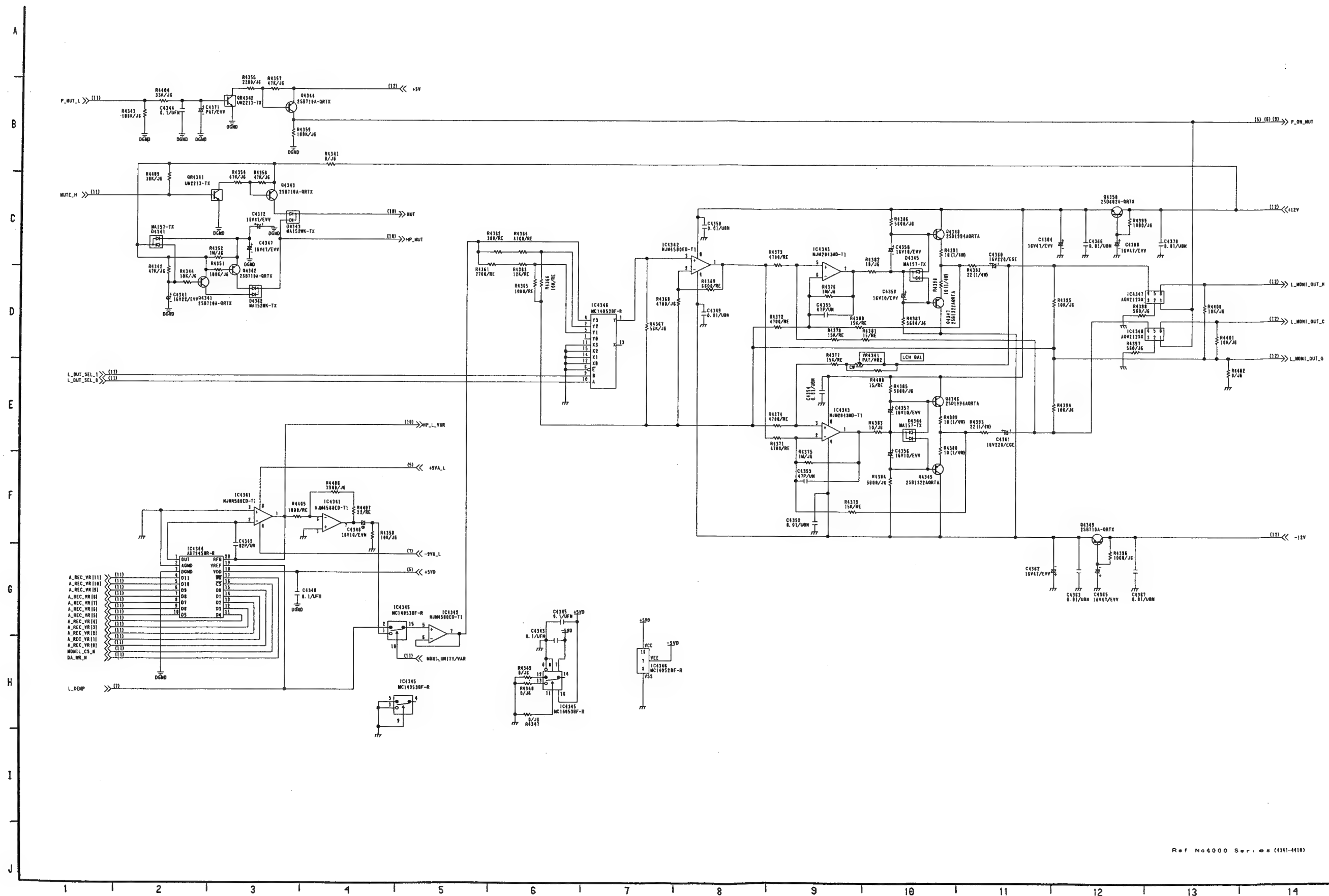
Ref No4000 Series (1221-1280)

ADDA (F8 7/12) SCHEMATIC DIAGRAM



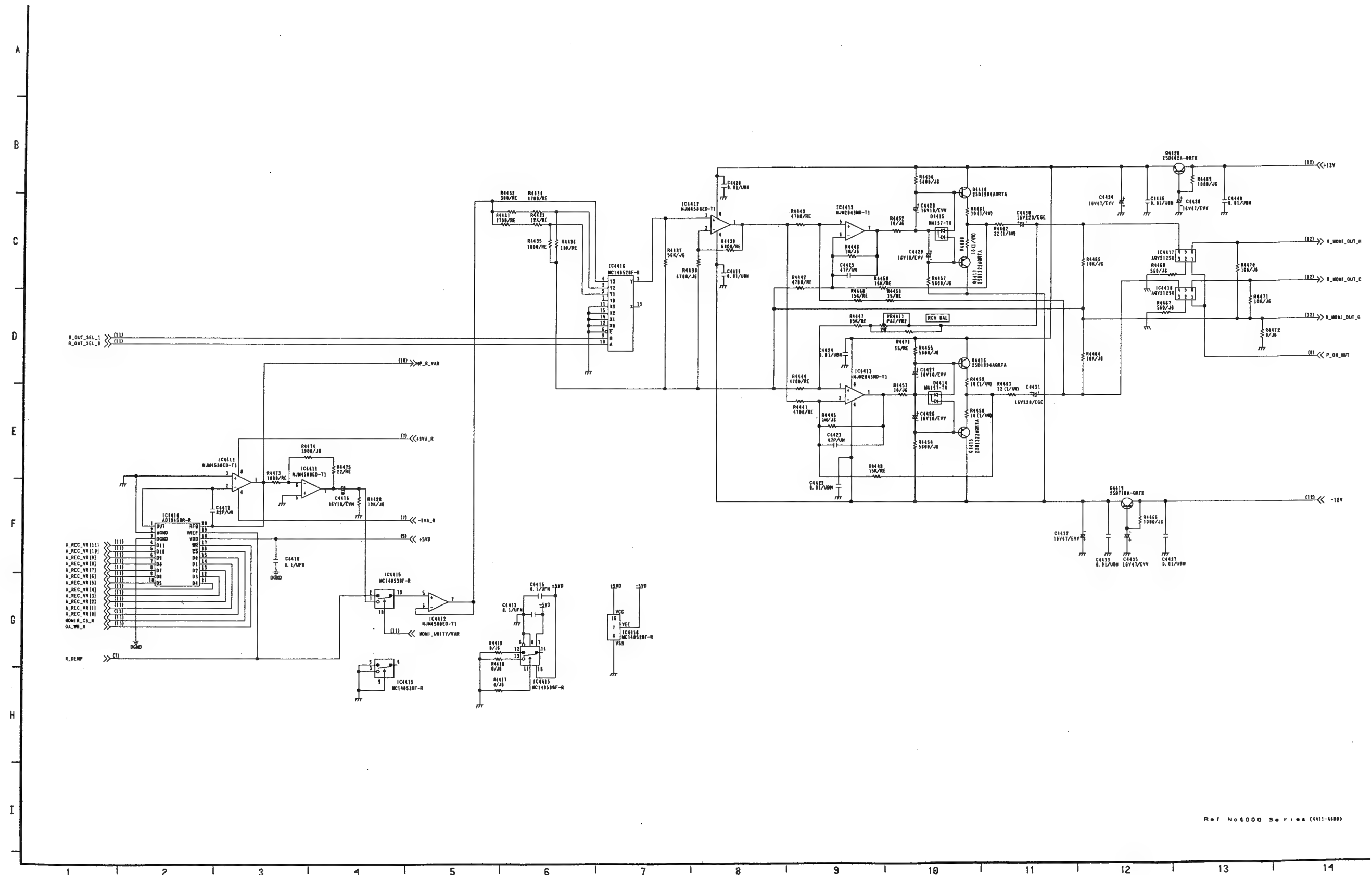
Ref No 4000 Serie (4281-4368)

ADDA (F8 8/12) SCHEMATIC DIAGRAM

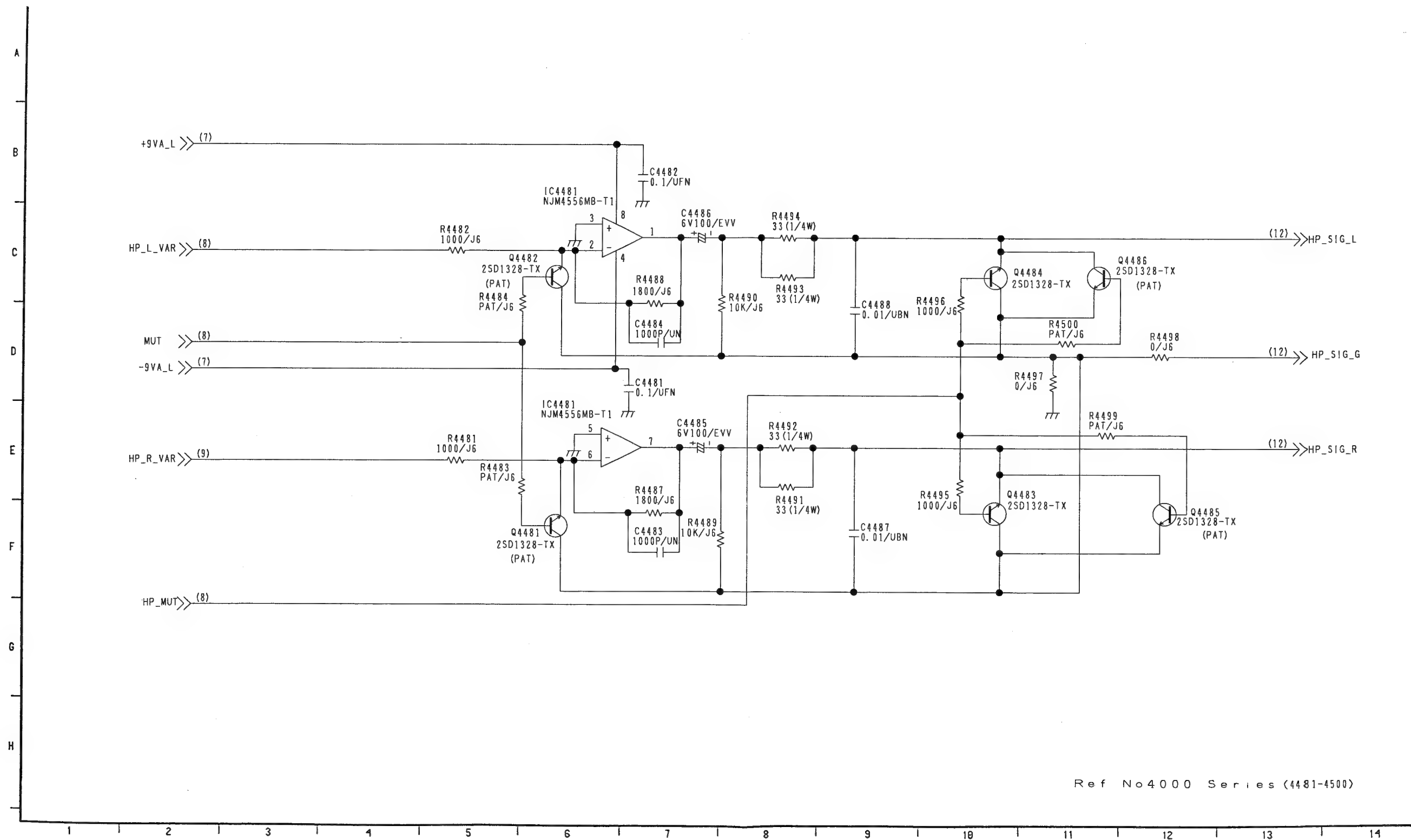


Ref No 4000 Series (4341-4348)

ADDA (F8 9/12) SCHEMATIC DIAGRAM

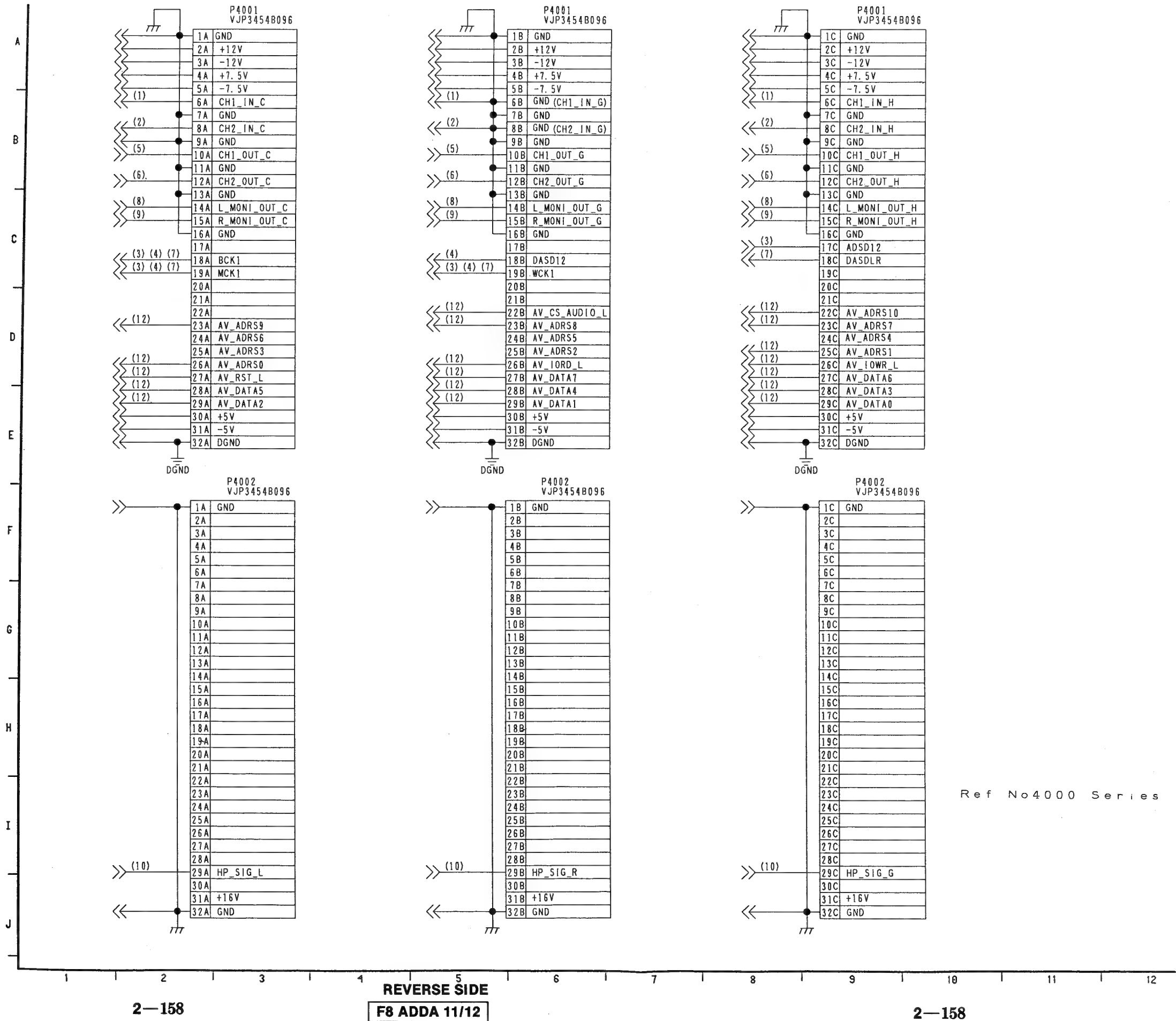


ADDA (F8 10/12) SCHEMATIC DIAGRAM



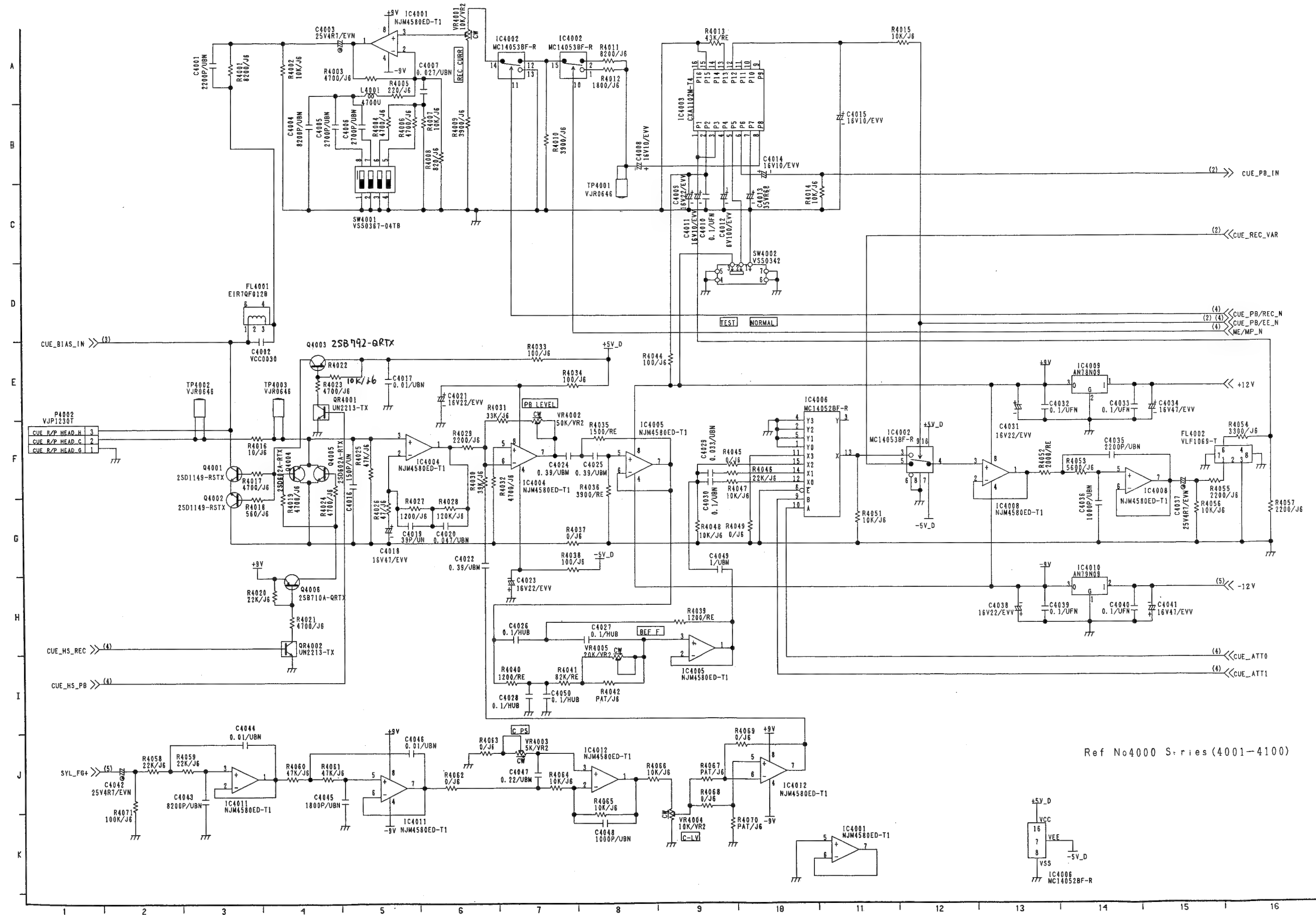
Ref No4000 Series (4481-4500)

ADDA (F8 12/12) CONNECTOR SCHEMATIC DIAGRAM

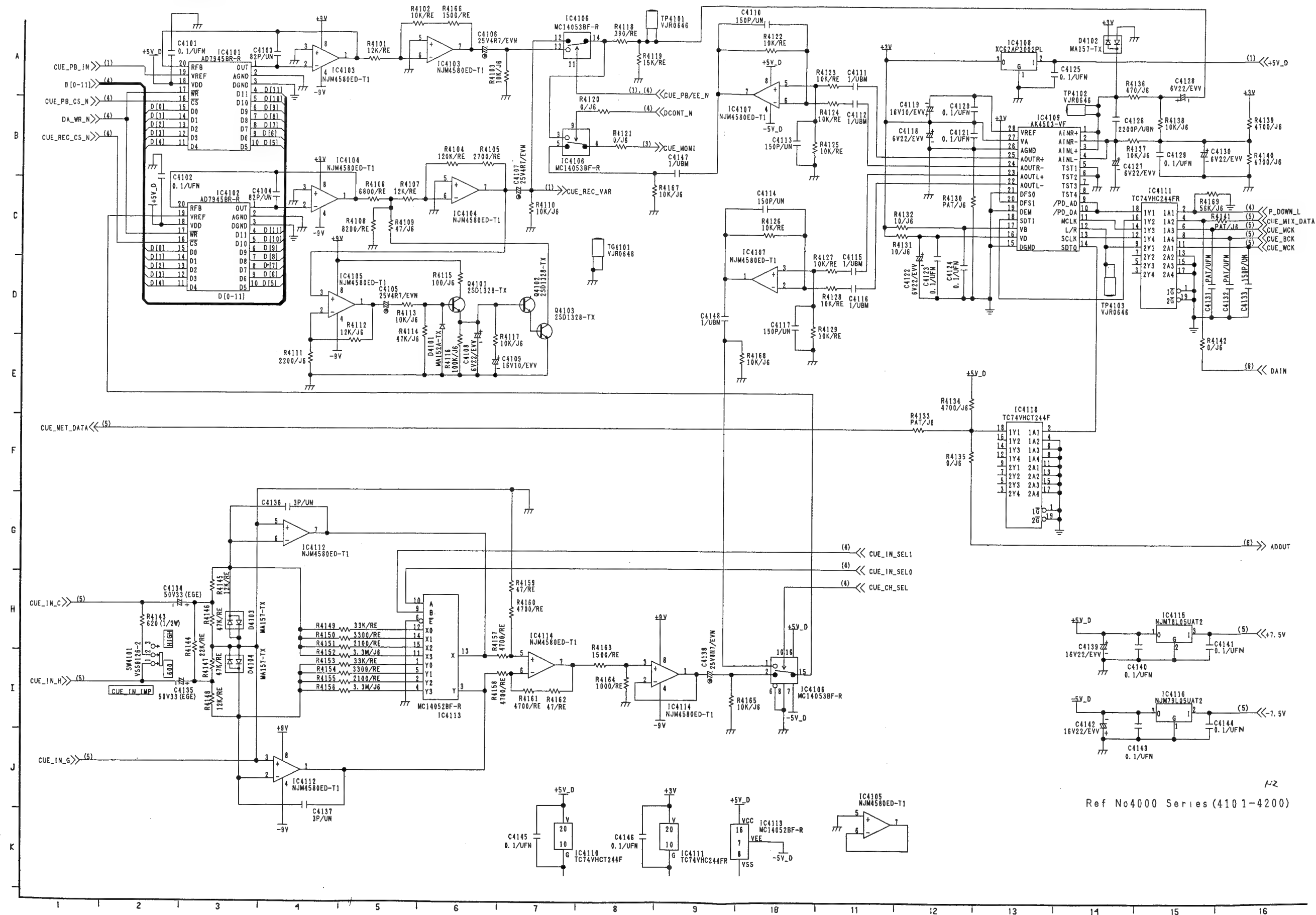


Ref No4000 Series

CUE (H2 1/6) SCHEMATIC DIAGRAM

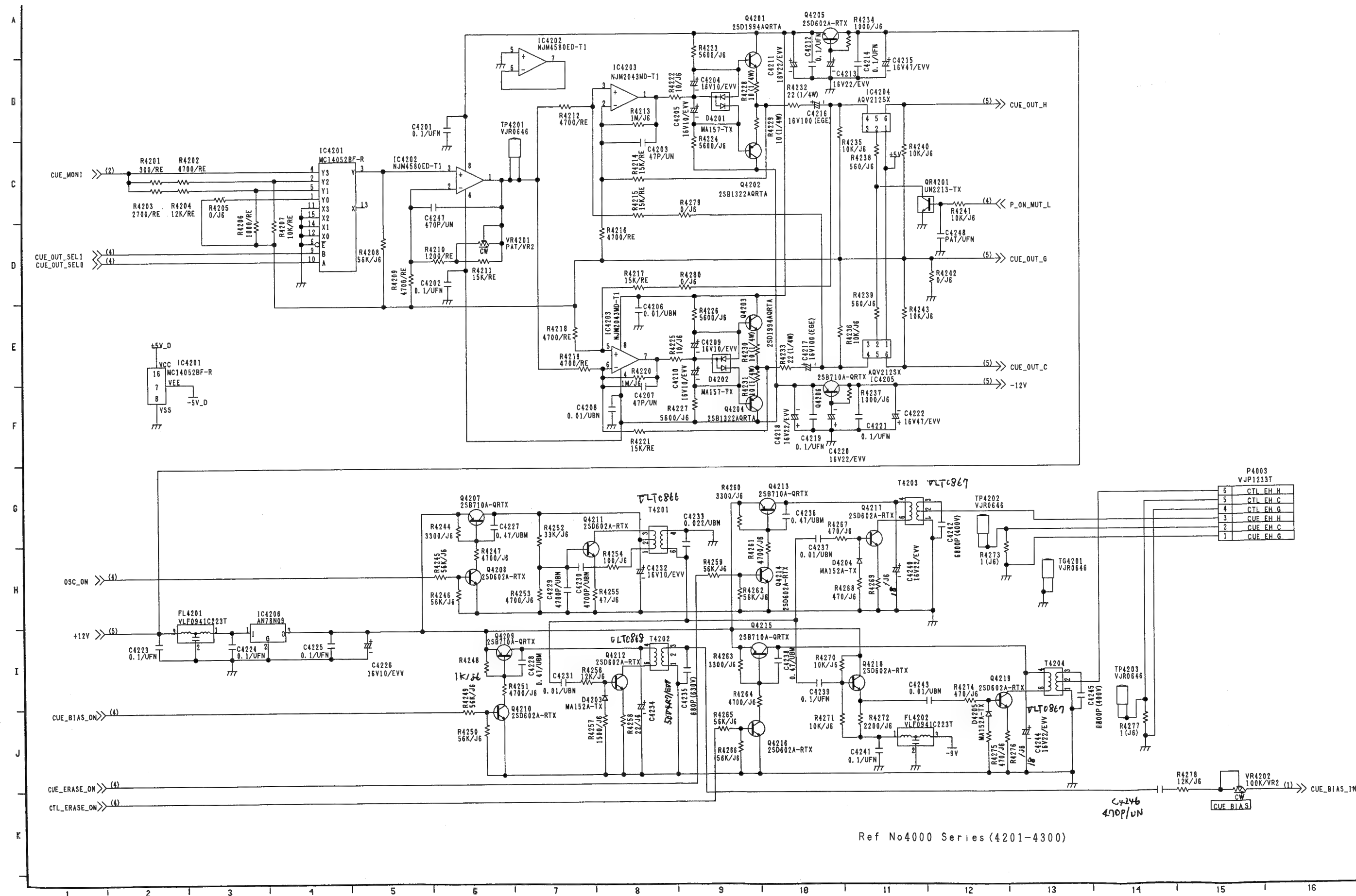


CUE (H2 2/6) SCHEMATIC DIAGRAM

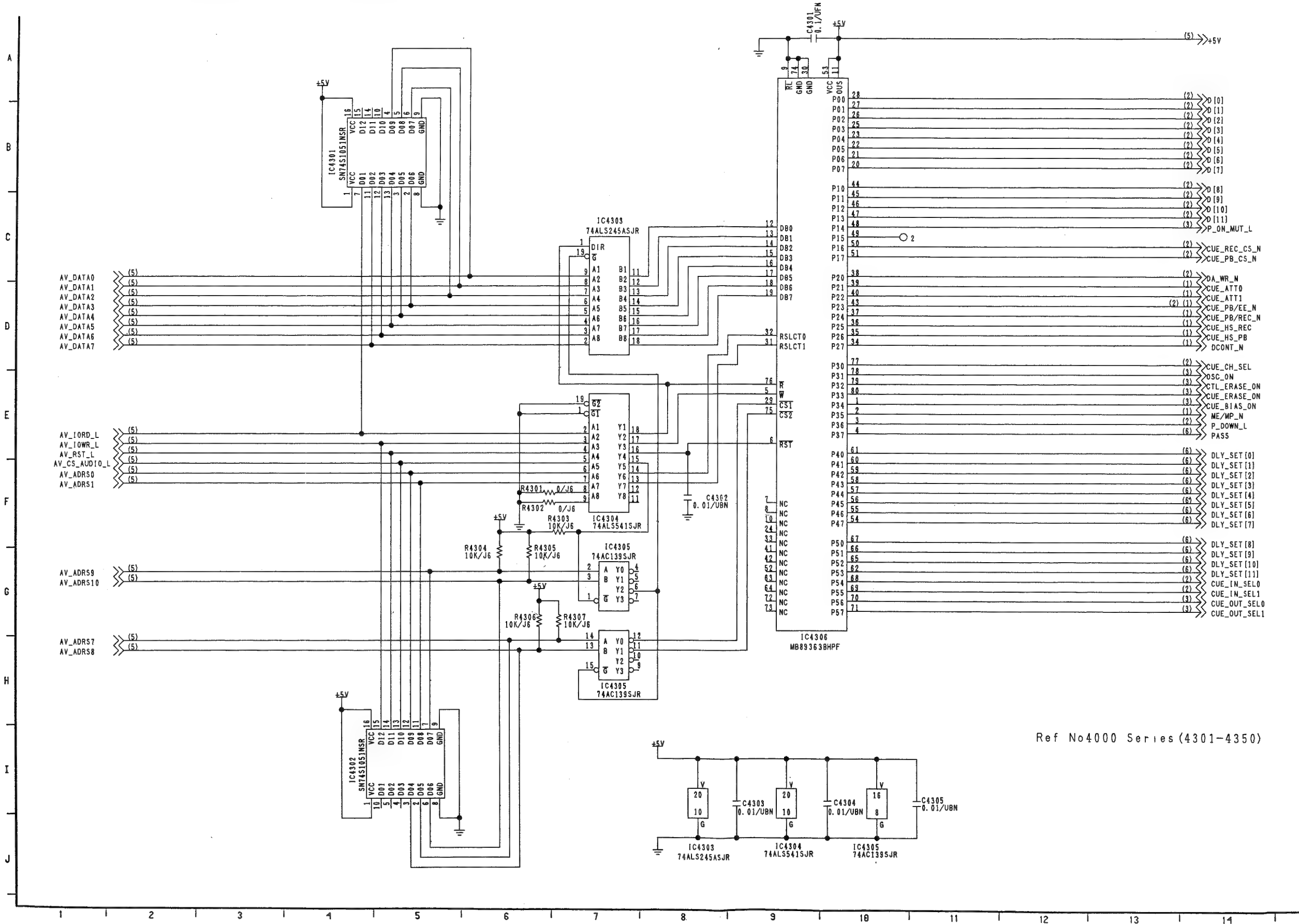


Ref No4000 Series (4101-4200)

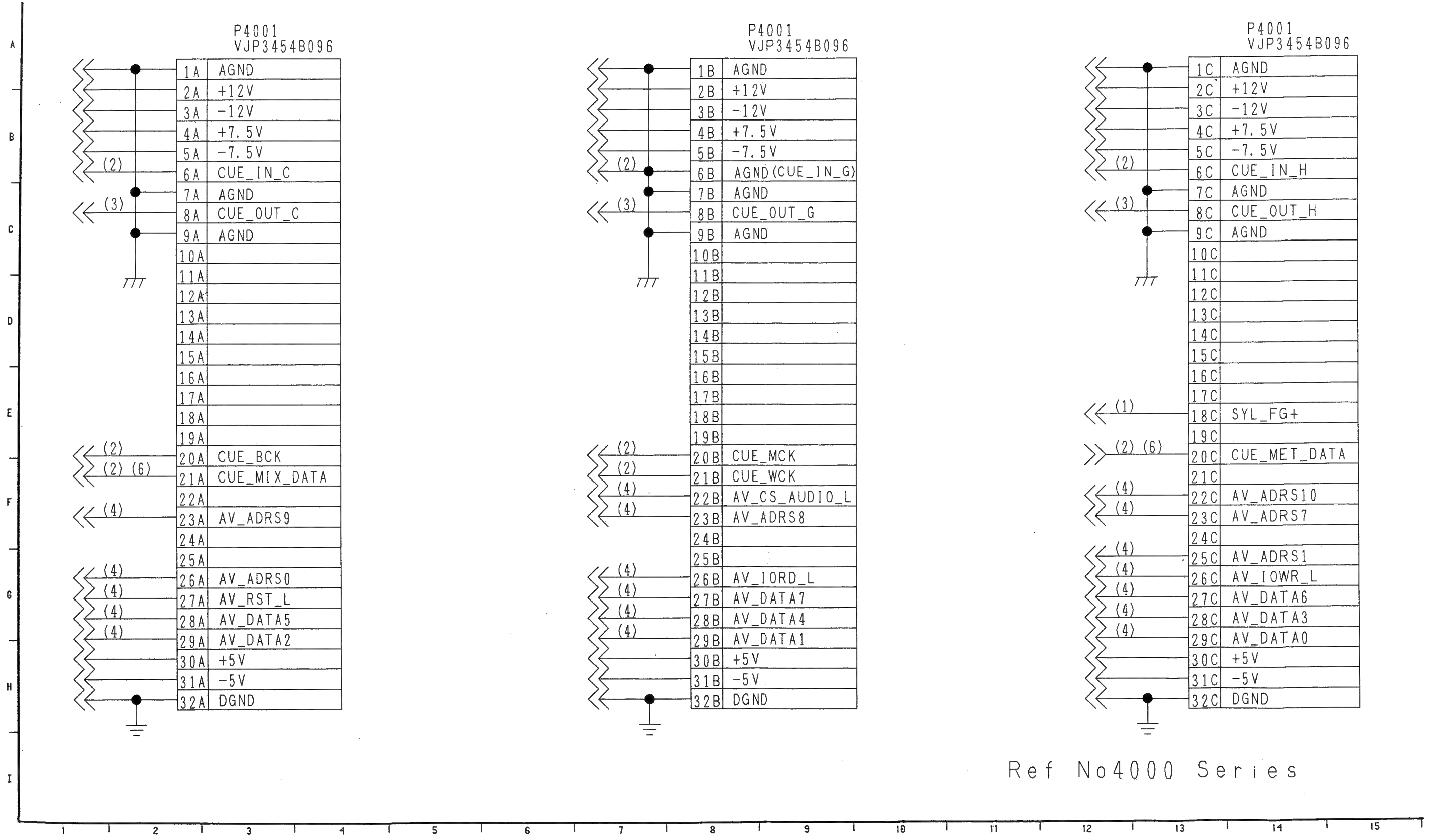
CUE (H2 3/6) SCHEMATIC DIAGRAM



CUE (H2 4/6) SCHEMATIC DIAGRAM

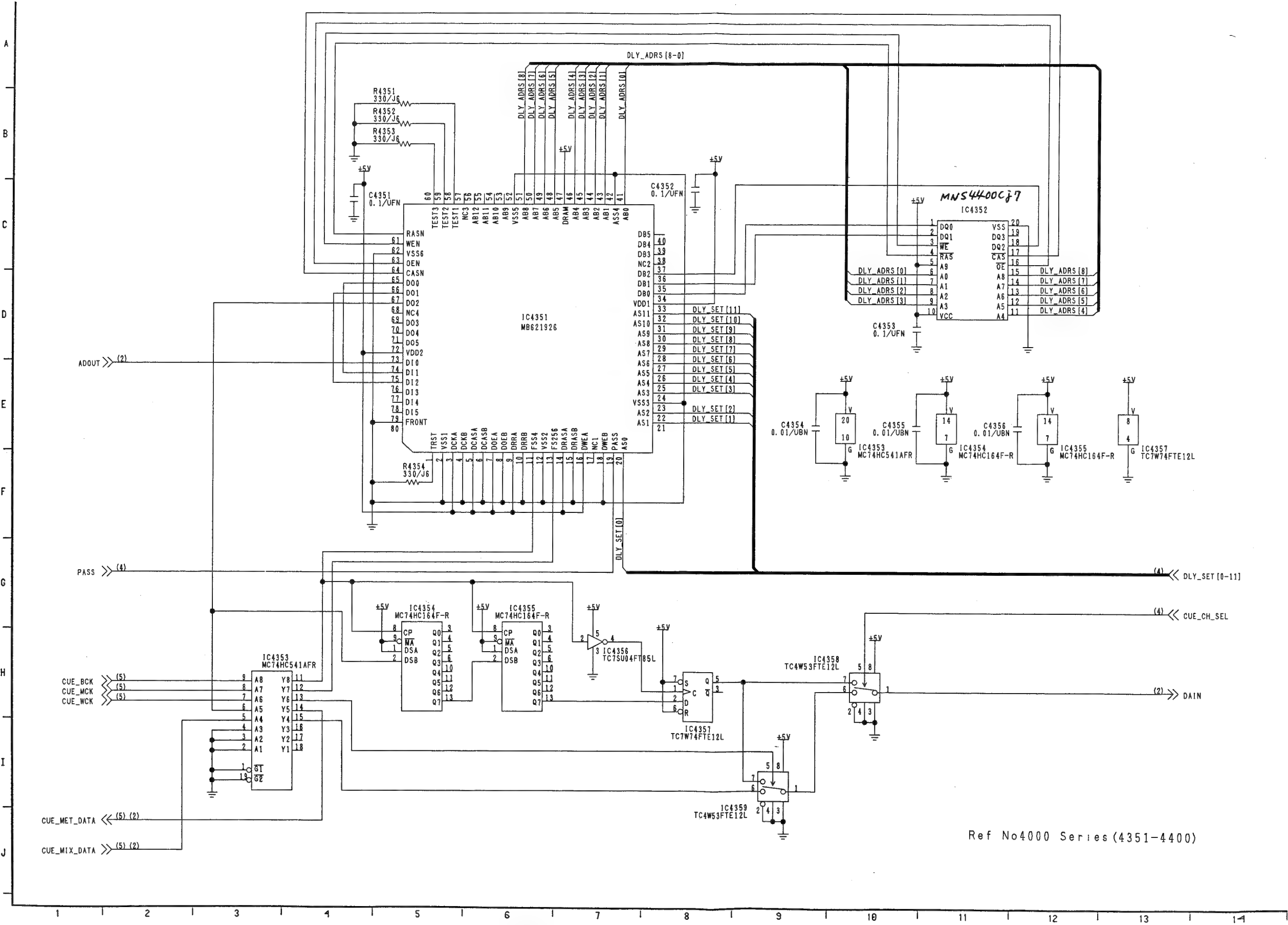


CUE (H2 5/6) SCHEMATIC DIAGRAM



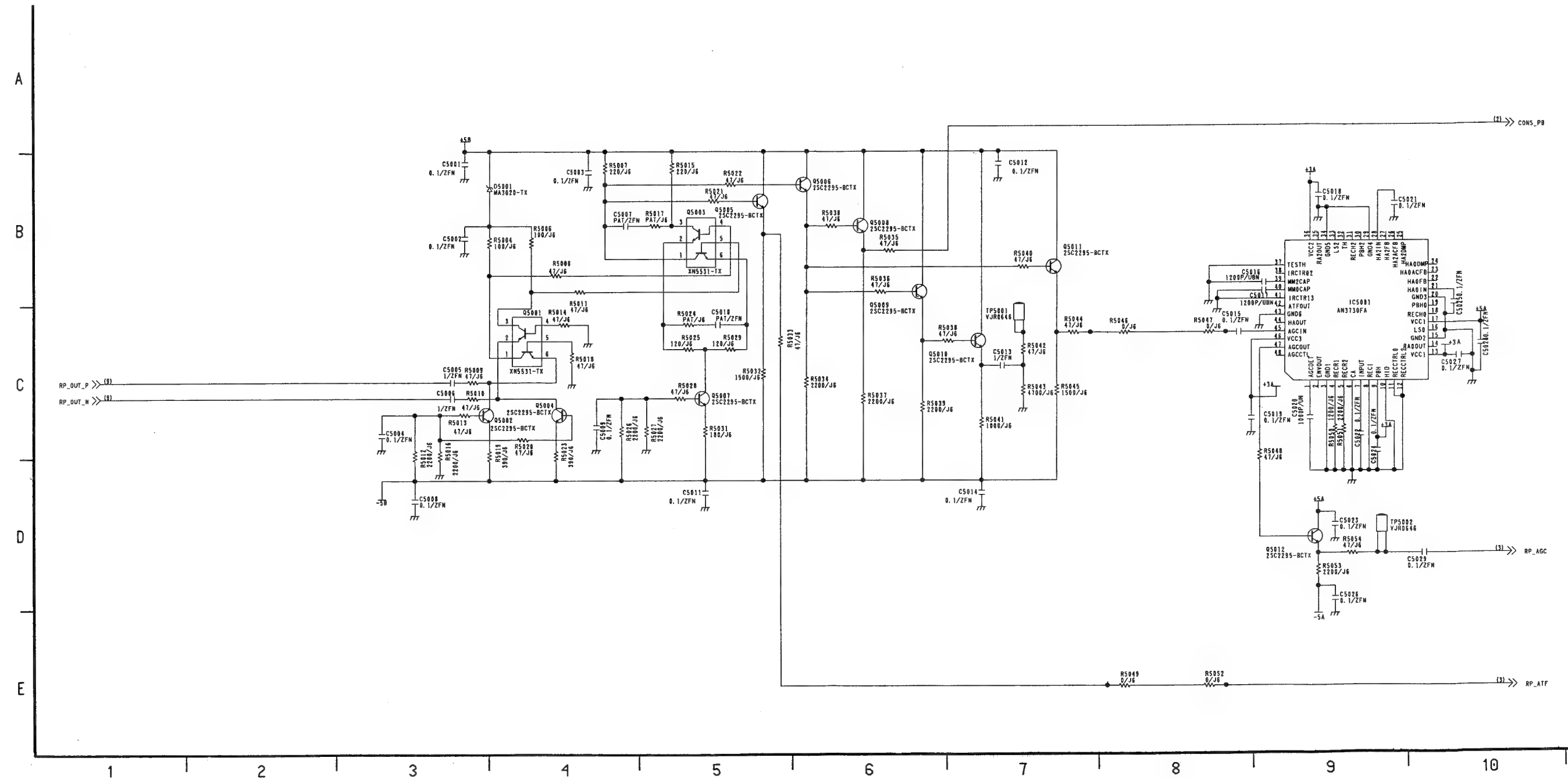
Ref No4000 Series

CUE (H2 6/6) SCHEMATIC DIAGRAM



Ref No4000 Series (4351-4400)

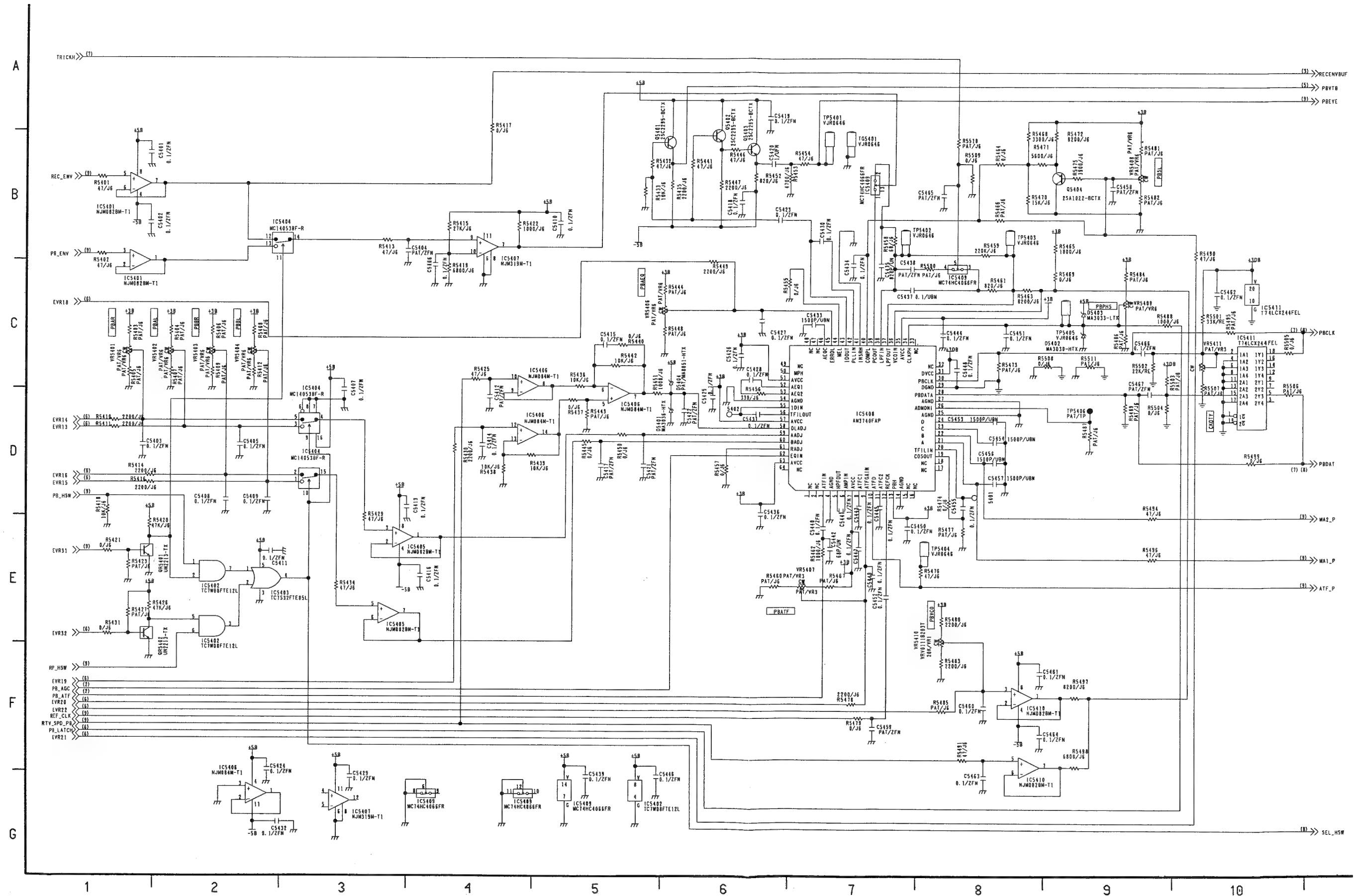
EQ (H3 1/9) SCHEMATIC DIAGRAM



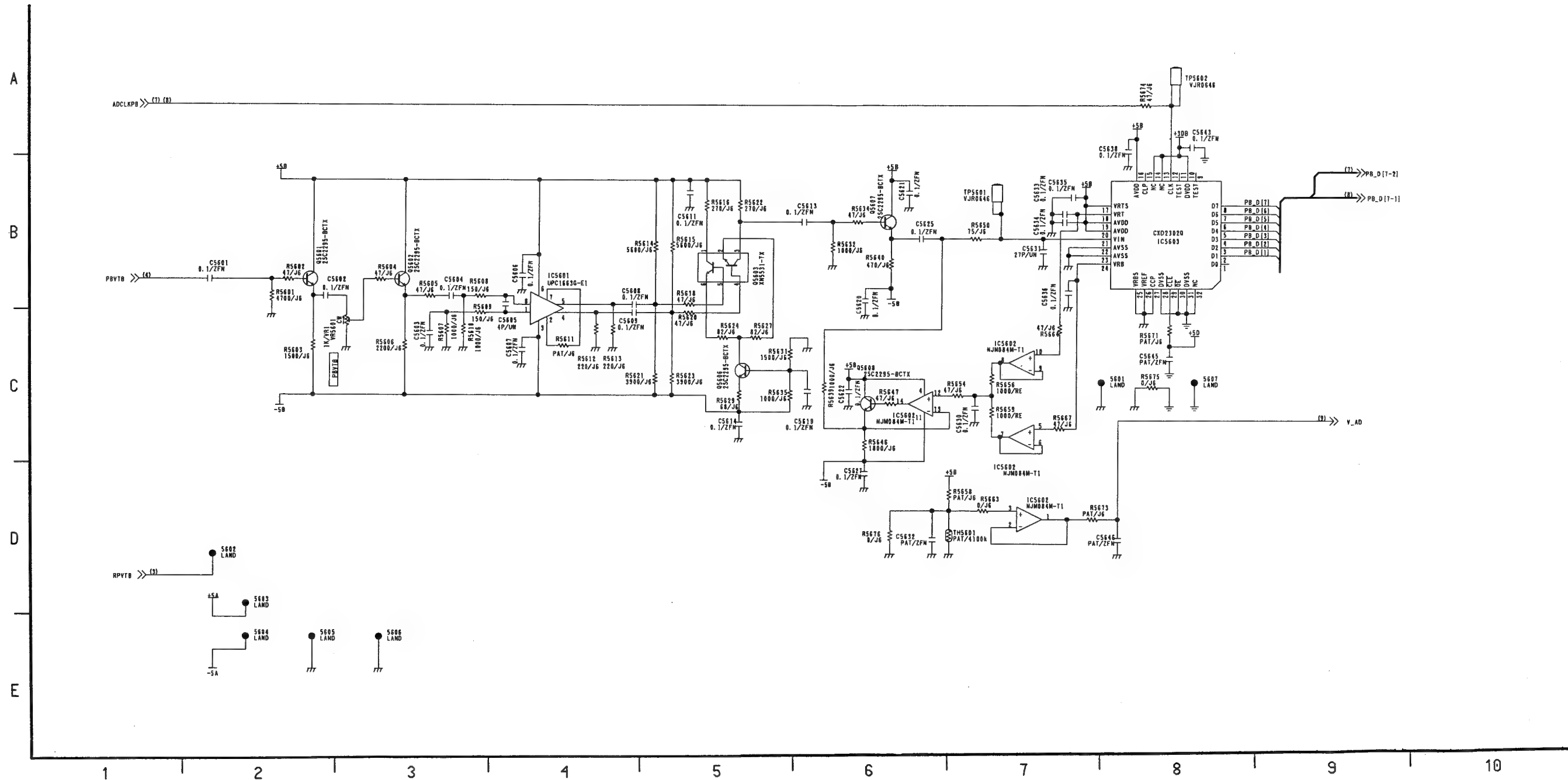
A



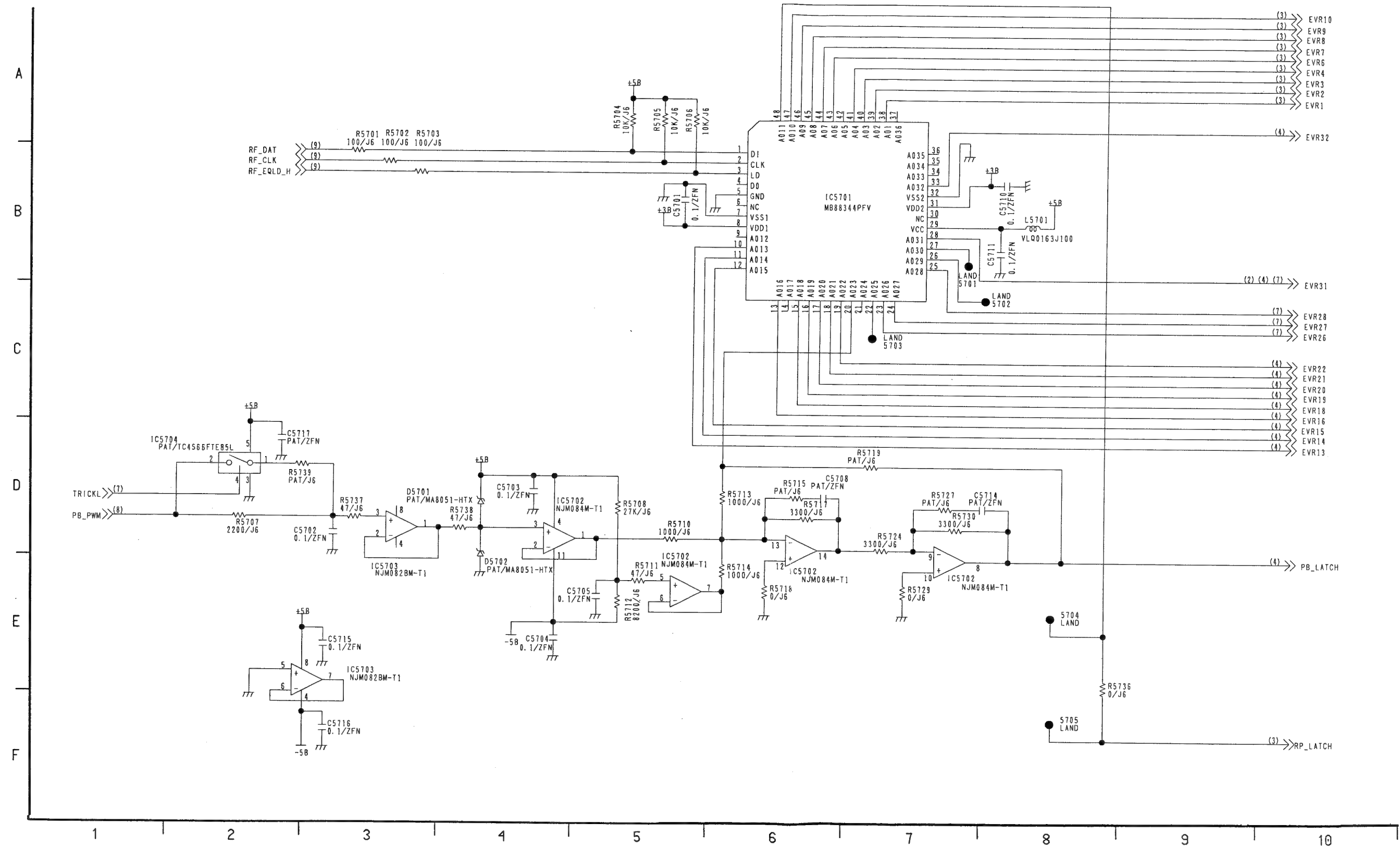
EQ (H3 4/9) SCHEMATIC DIAGRAM



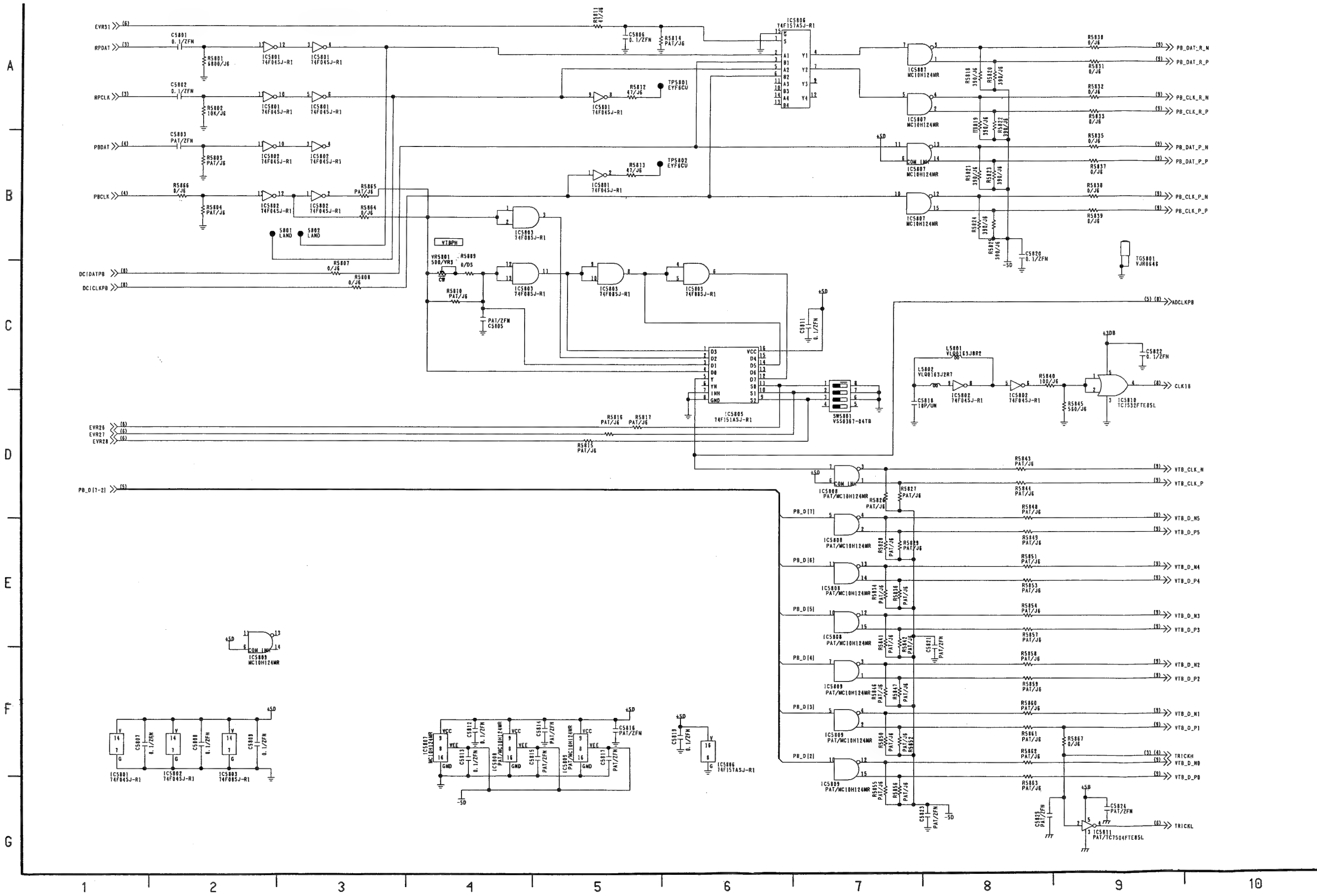
EQ (H3 5/9) SCHEMATIC DIAGRAM



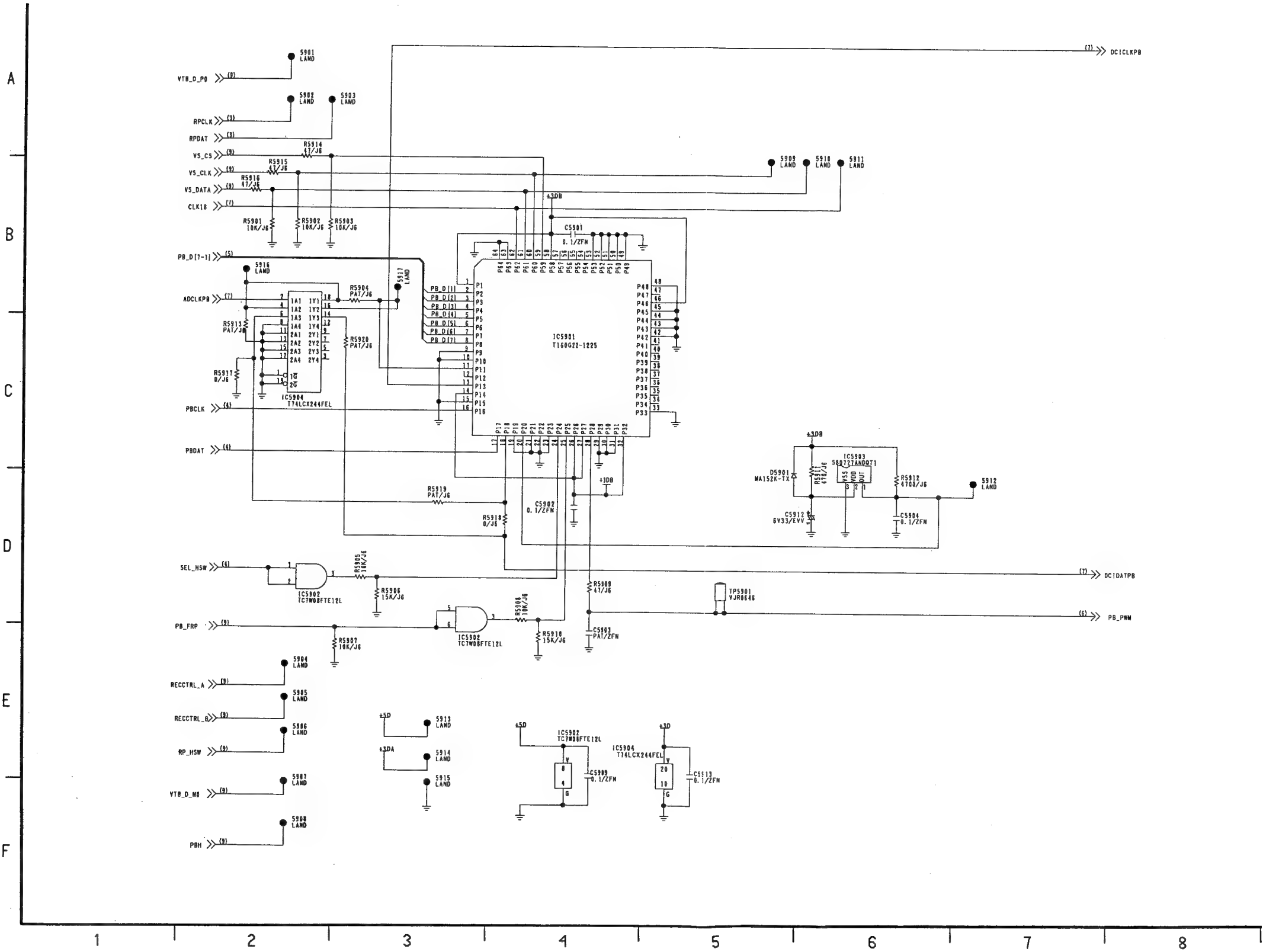
EQ (H3 6/9) SCHEMATIC DIAGRAM



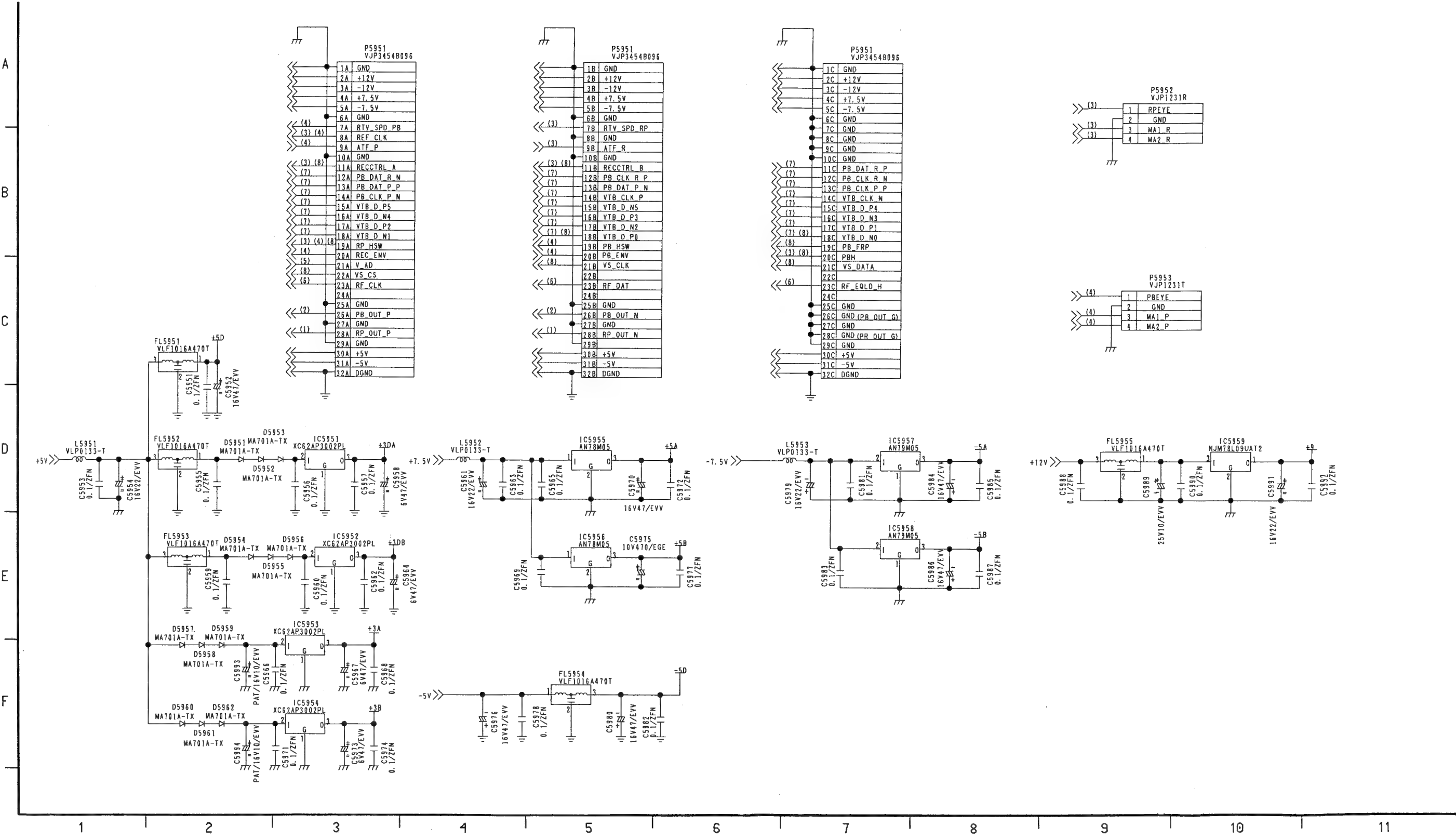
EQ (H3 7/9) SCHEMATIC DIAGRAM



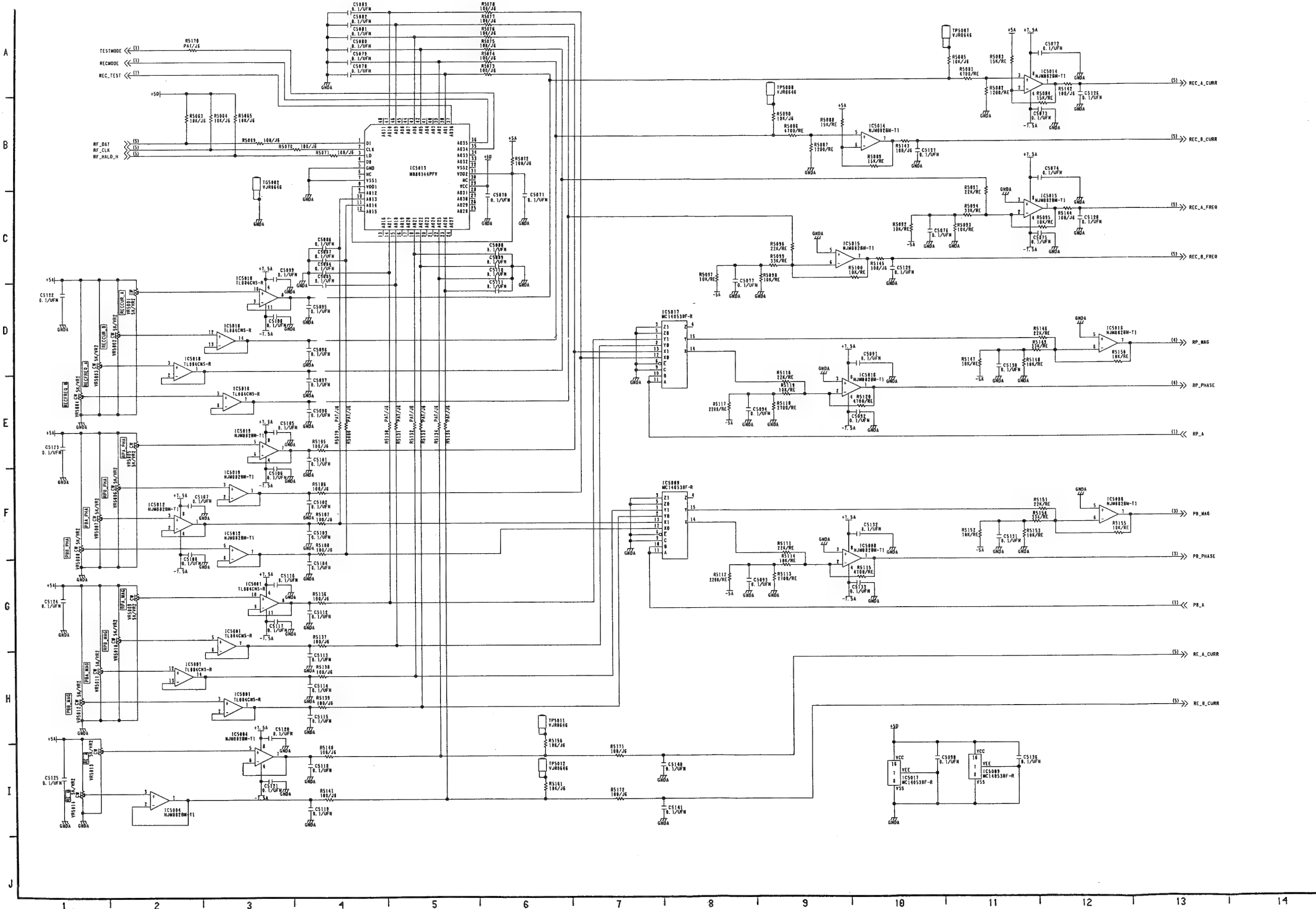
EQ (H3 8/9) SCHEMATIC DIAGRAM



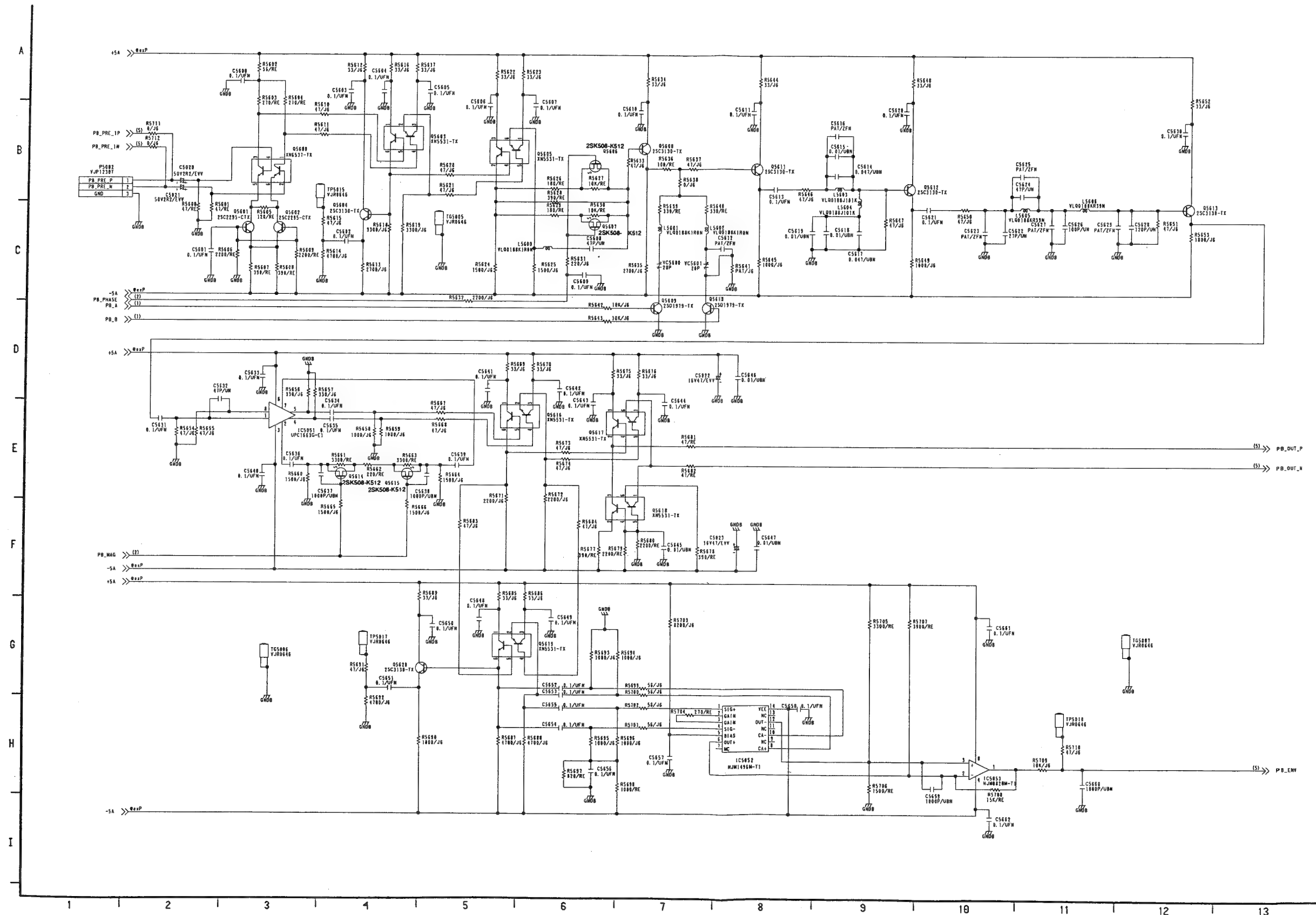
EQ (H3 9/9) SCHEMATIC DIAGRAM



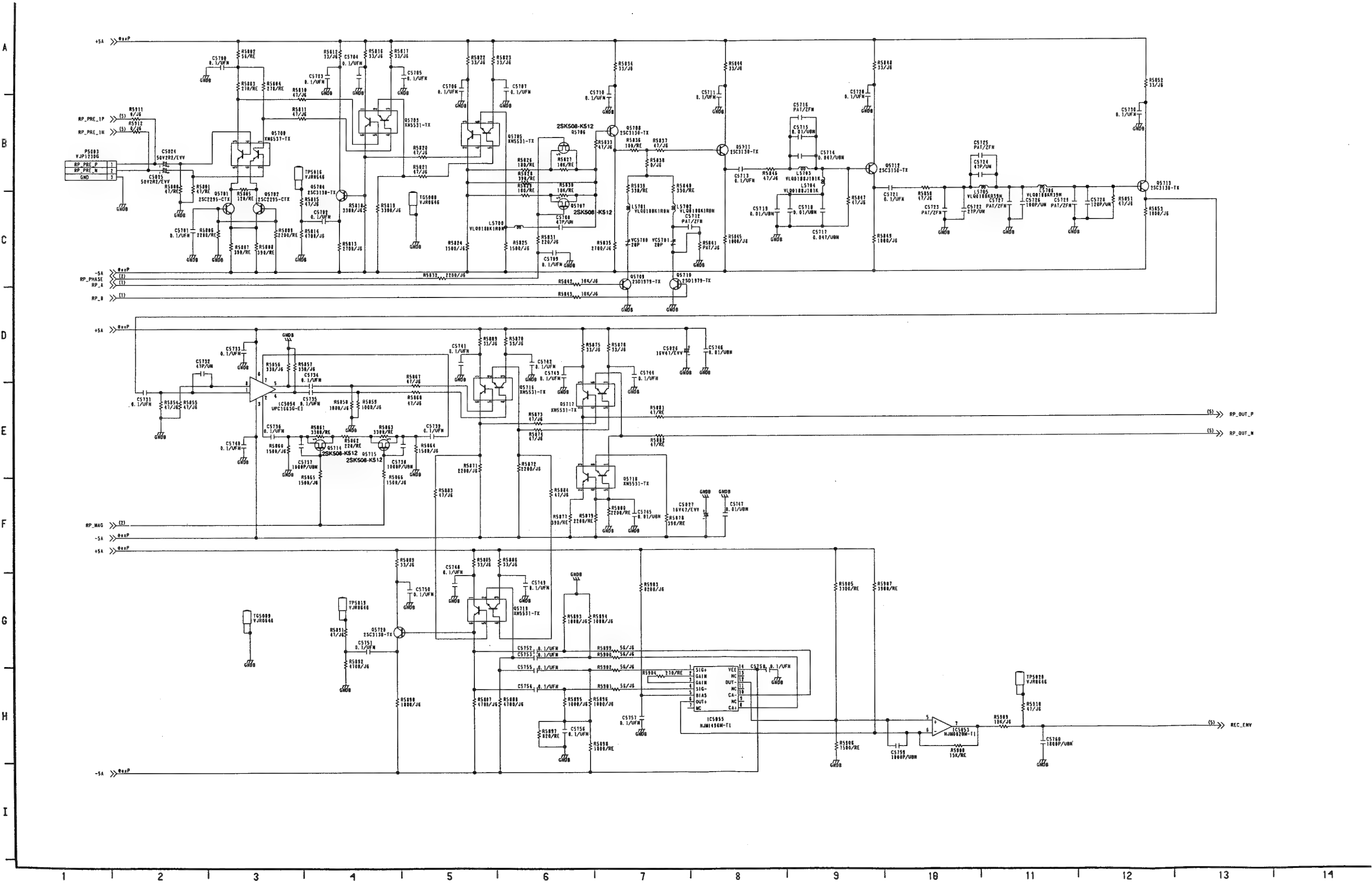
RF AMP (H4 2/5) SCHEMATIC DIAGRAM



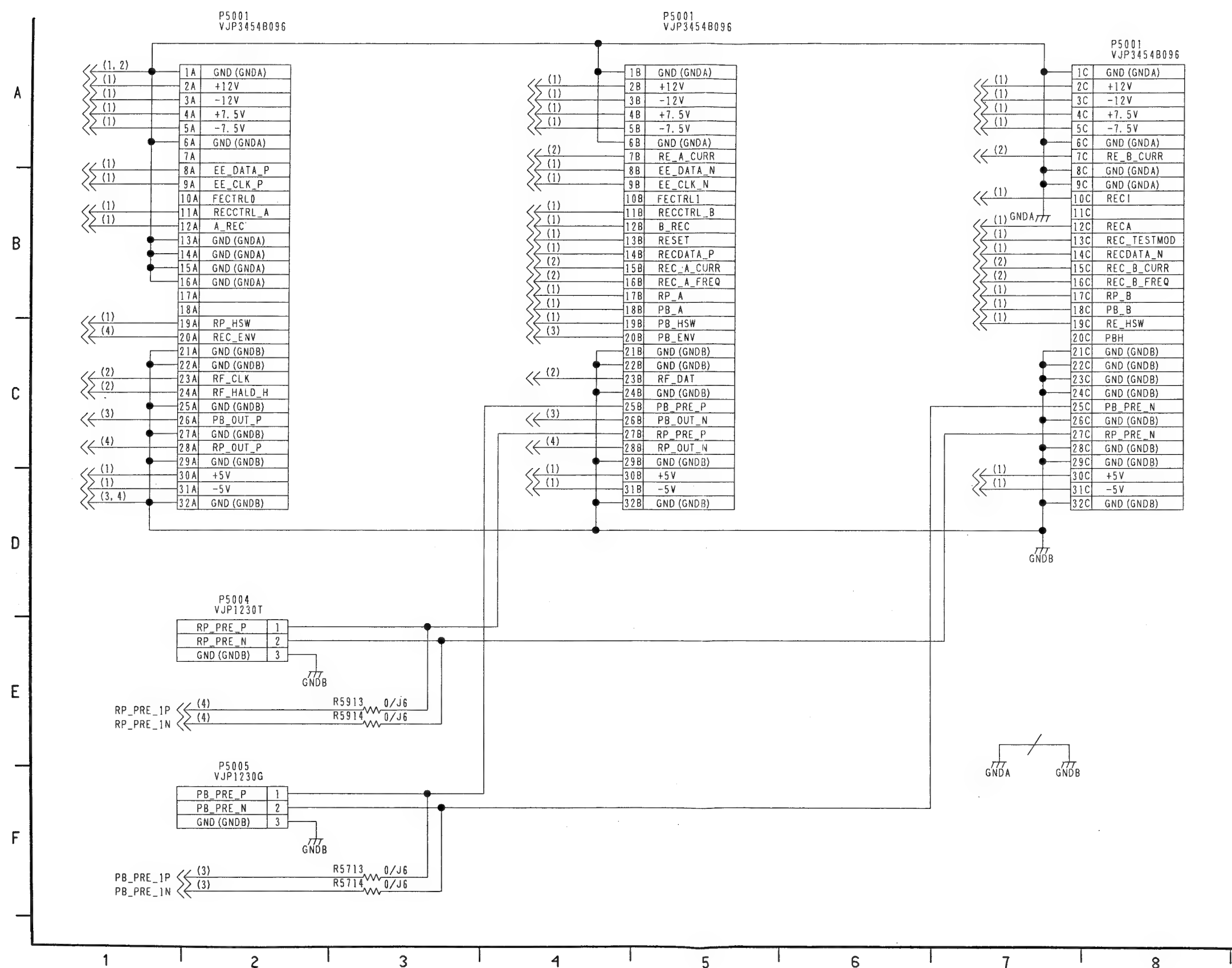
RF AMP (H4 3/5) SCHEMATIC DIAGRAM



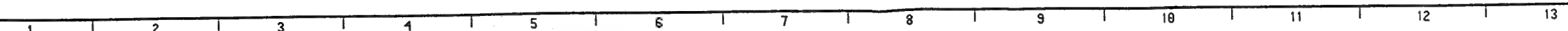
RF AMP (H4 4/5) SCHEMATIC DIAGRAM



RF AMP (H4 5/5) SCHEMATIC DIAGRAM

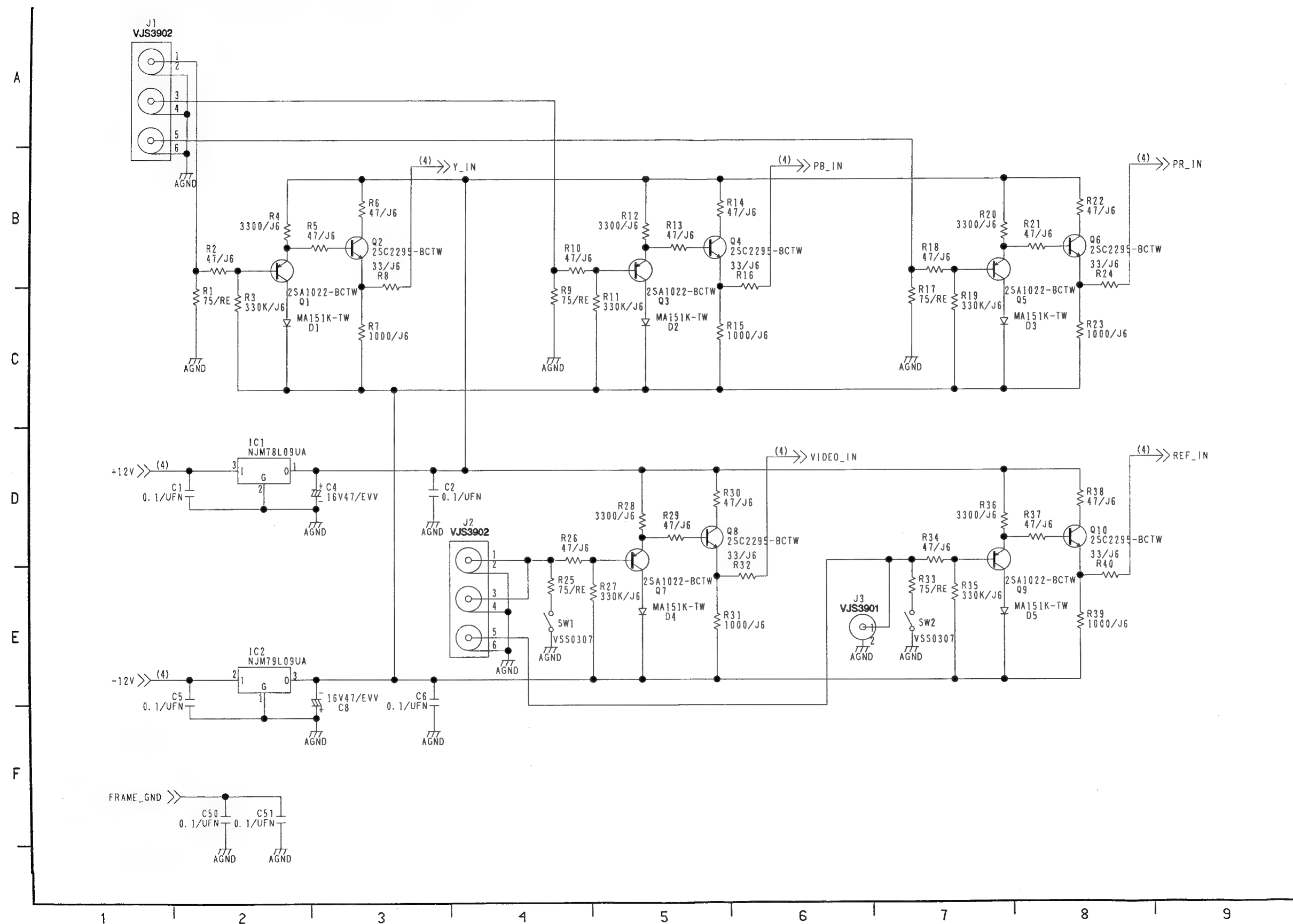


A vertical scale with labels A through J. The labels are positioned to the left of a vertical line, with horizontal tick marks extending from the line to each label. The labels are: A, B, C, D, E, F, G, H, I, J.

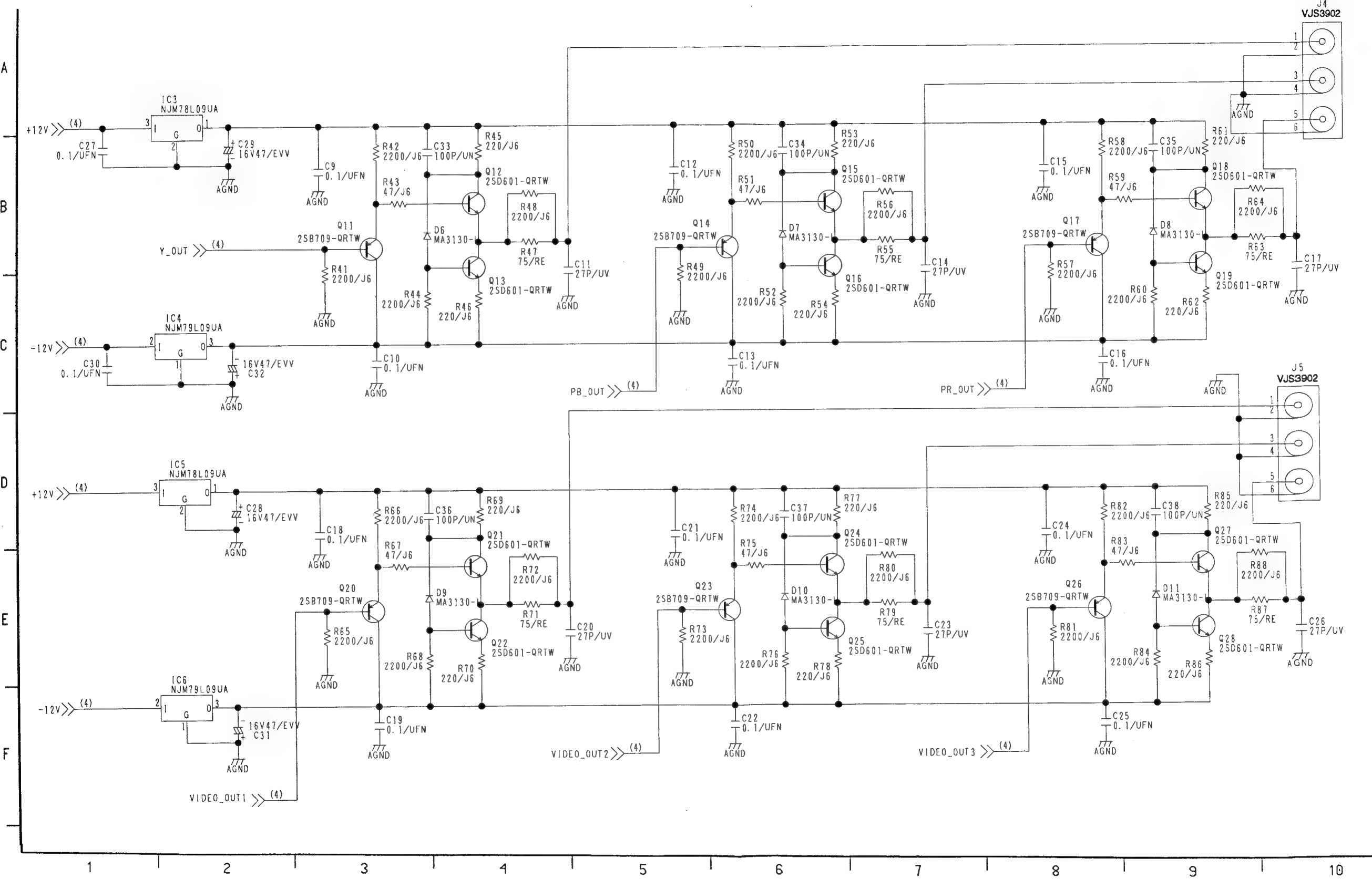


HEAD BUFFER 1/2

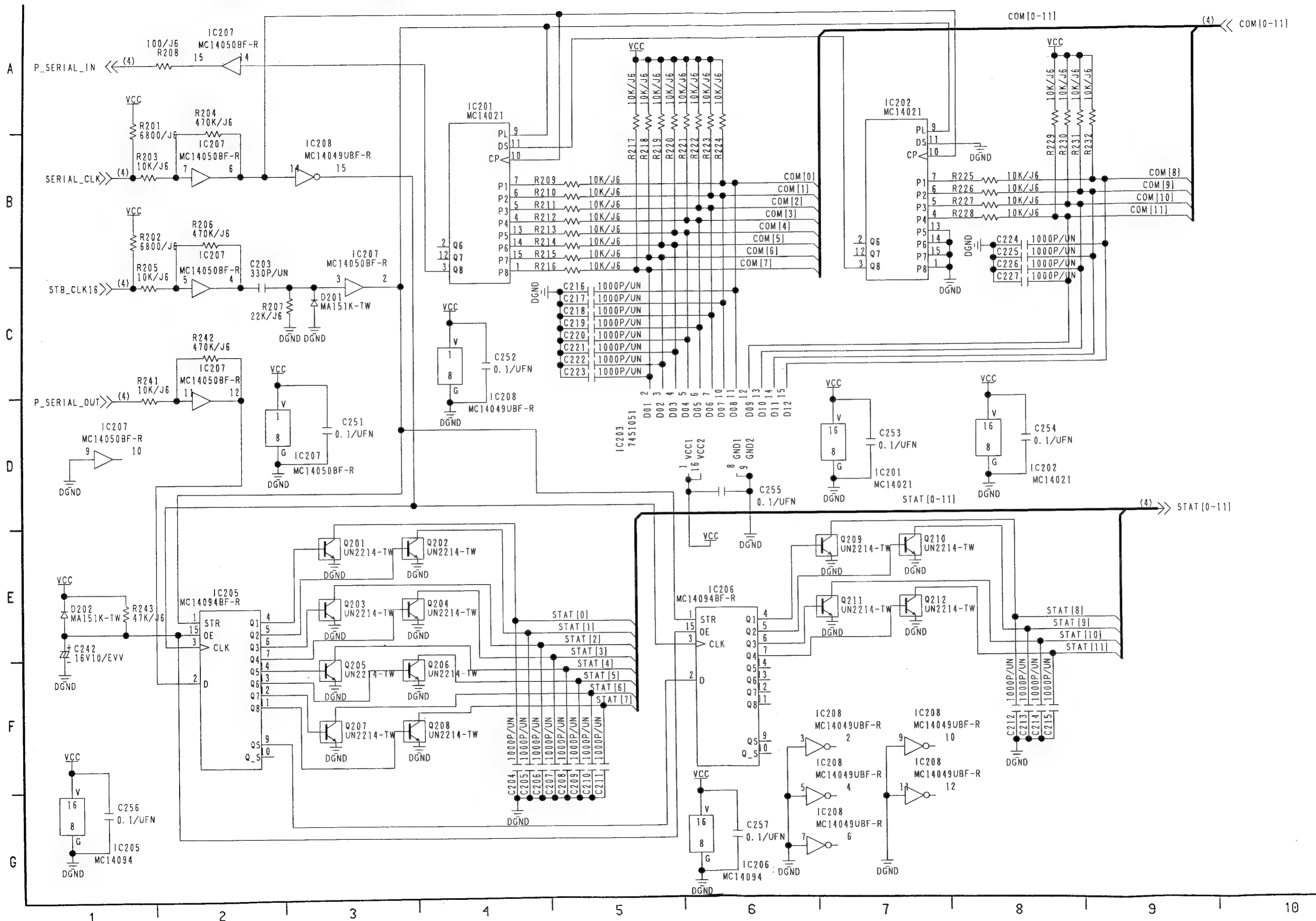
V/S JACK (1/4) SCHEMATIC DIAGRAM



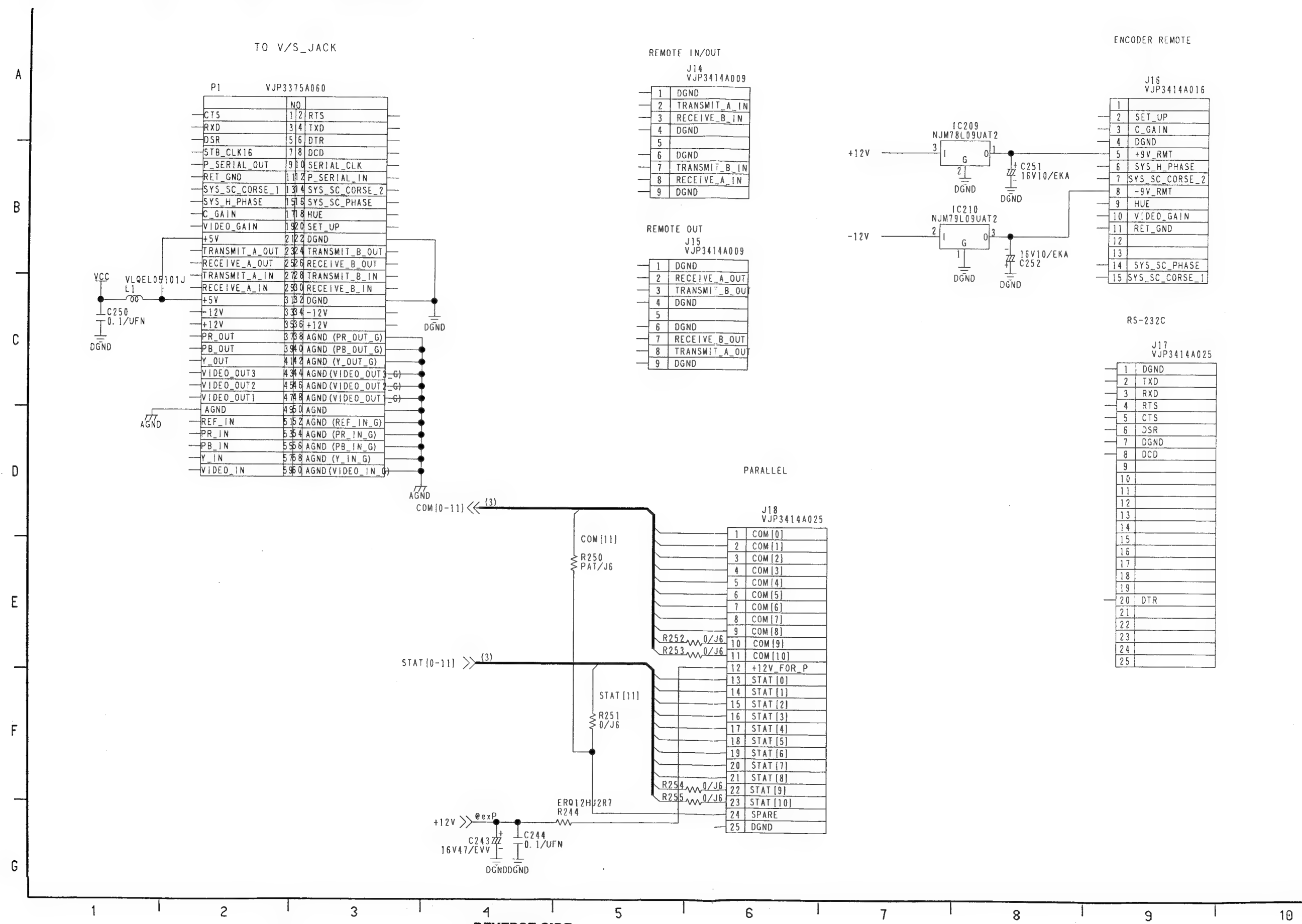
V/S JACK (2/4) SCHEMATIC DIAGRAM



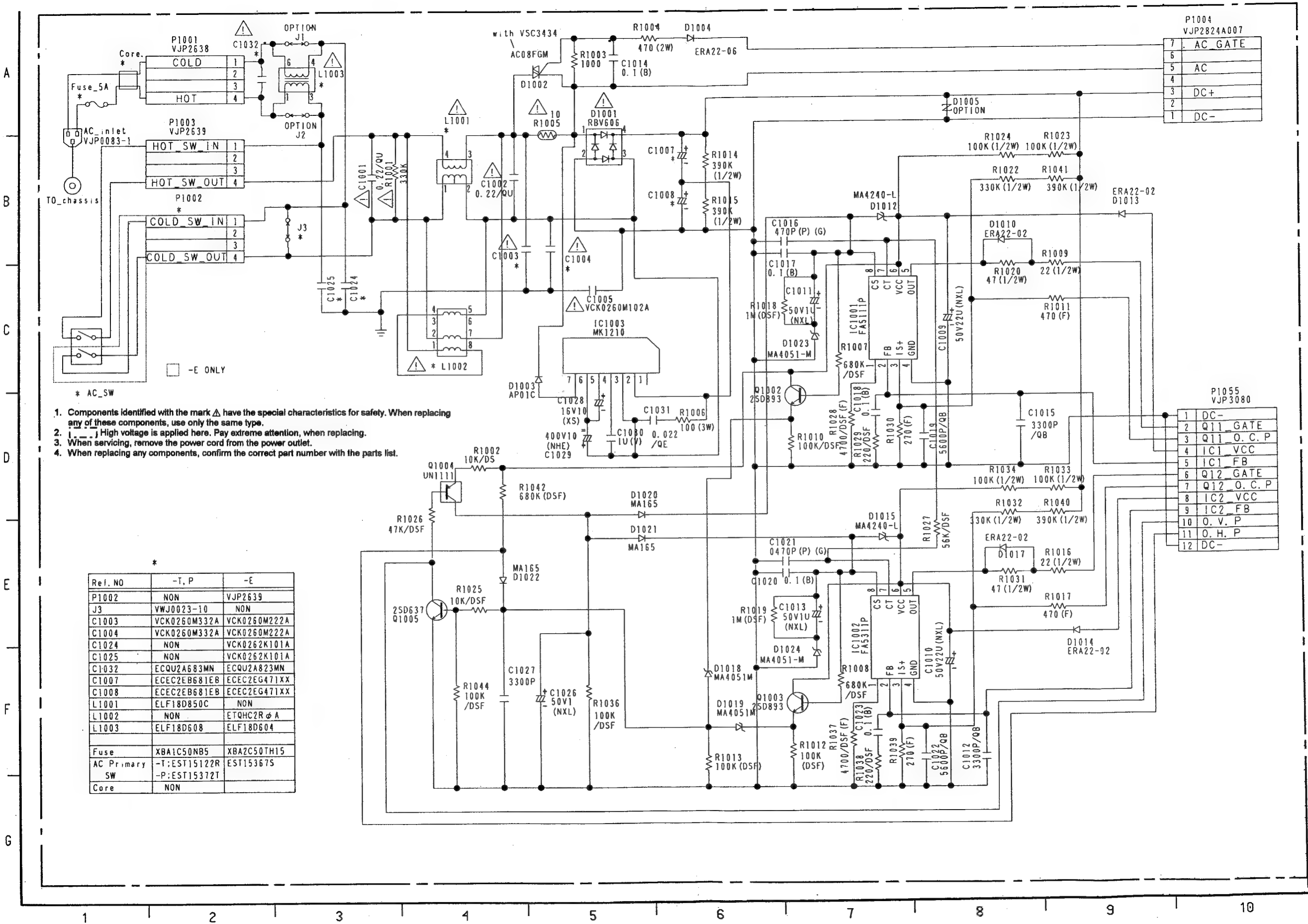
V/S JACK (3/4) SCHEMATIC DIAGRAM



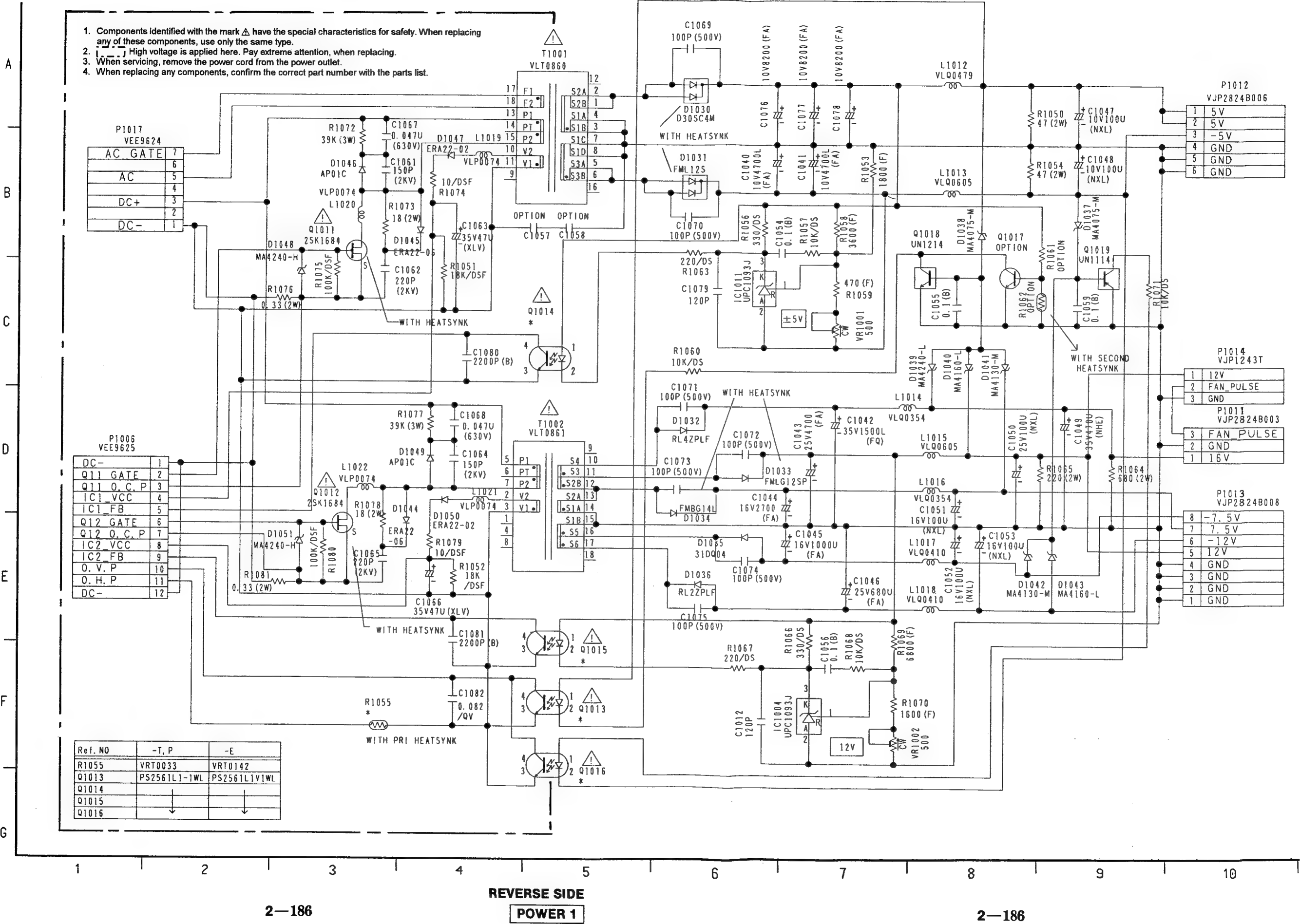
V/S JACK (4/4) SCHEMATIC DIAGRAM



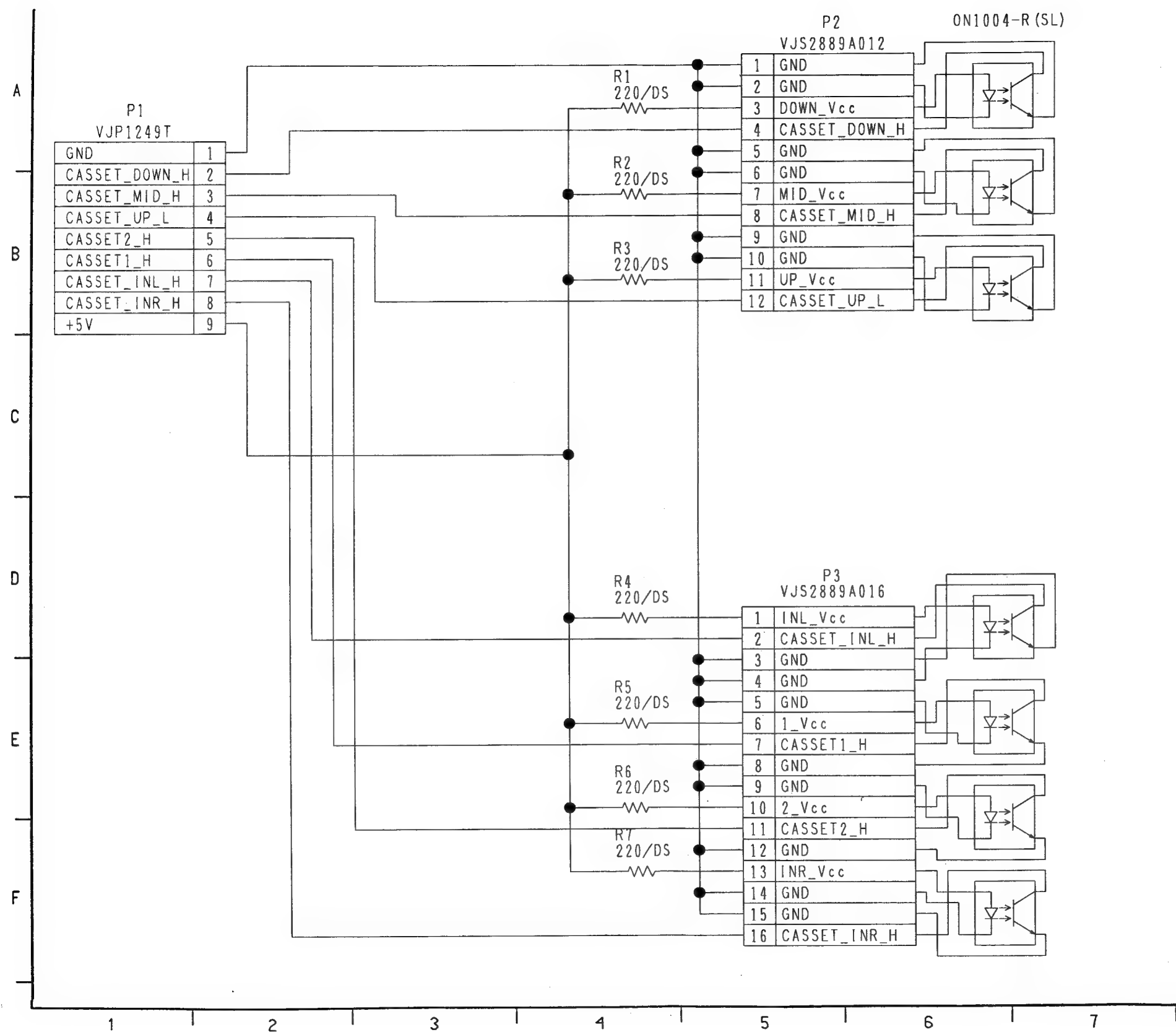
POWER 1 SCHEMATIC DIAGRAM



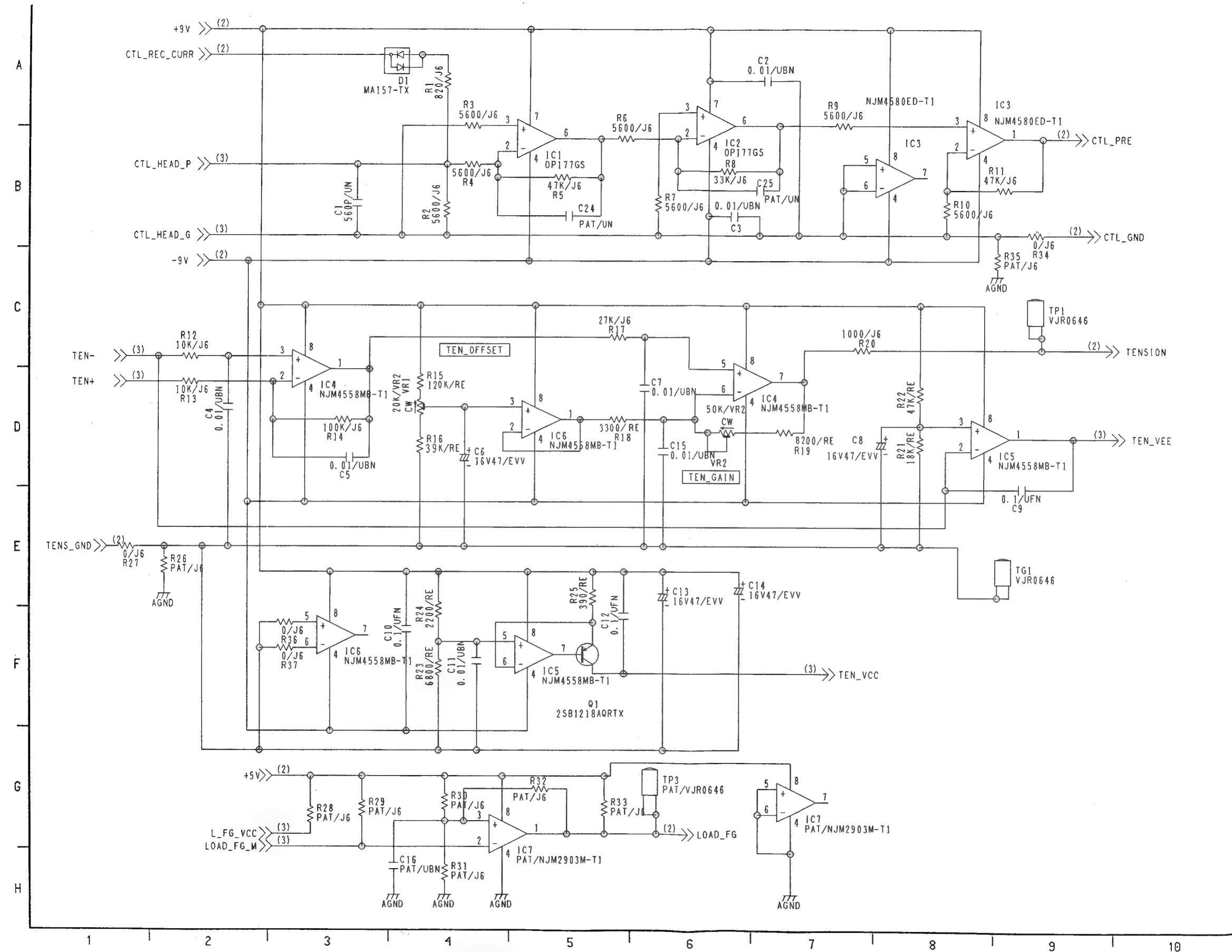
POWER 2 SCHEMATIC DIAGRAM



CARRIAGE SCHEMATIC DIAGRAM

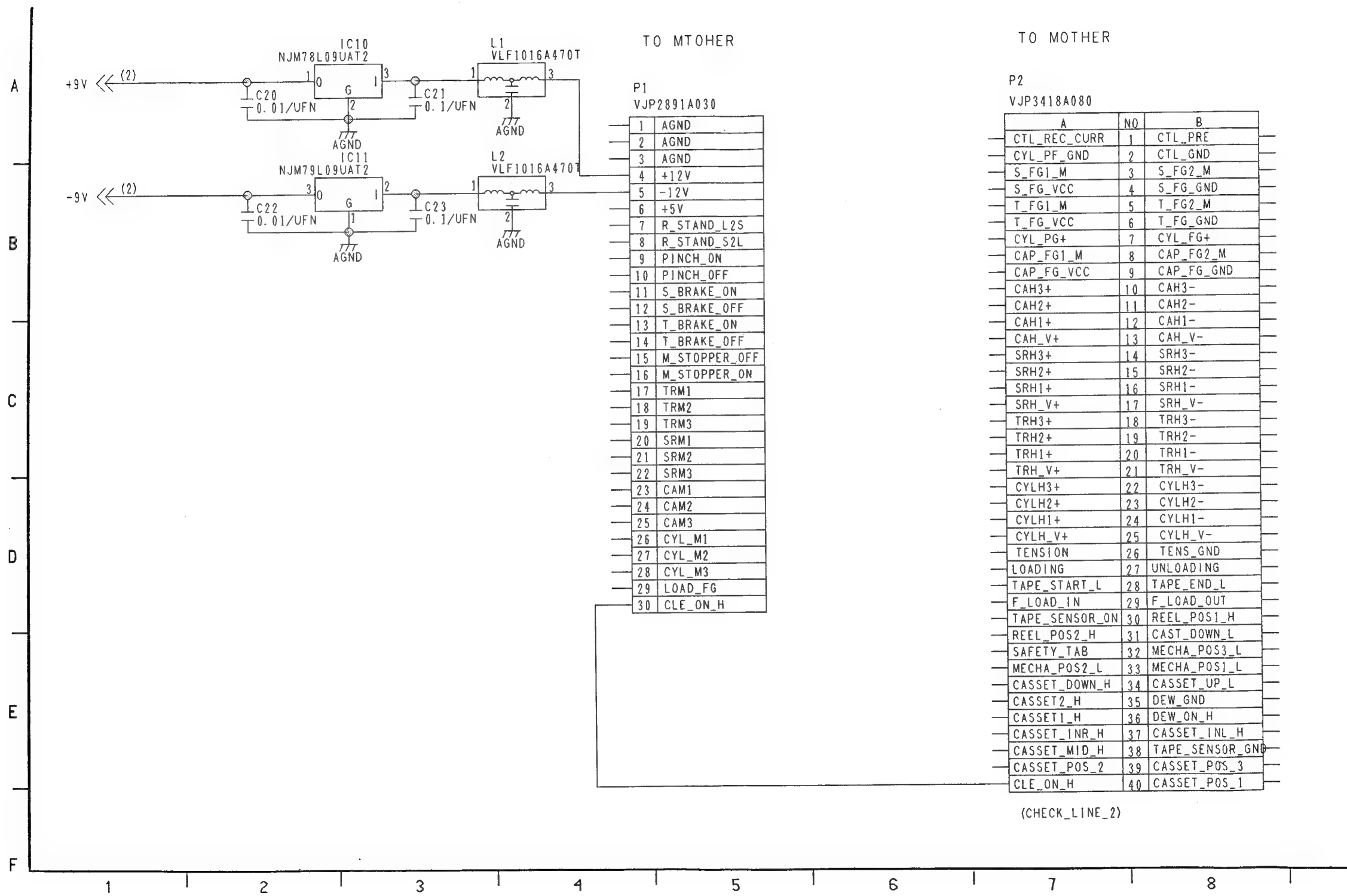


MECHA I/F (1/4) SCHEMATIC DIAGRAM



REVERSE SIDE
CARRIAGE

MECHA I/F (2/4) SCHEMATIC DIAGRAM



A

B

C

D

E

F

G

1

2

3

4

5

6

7

8

9

10

MIC UNIT
P17
VJS3801D010

1	
2	
3	SAFETY_TAB
4	AGND
5	CASSET_POS_1 (MIC1)
6	CASSET_POS_2 (MIC2)
7	CASSET_POS_3 (MIC3)
8	AGND (MIC4)
9	
10	

REEL STAND POS
P12
VJP3172D005

1	+5V
2	REEL_POS1_H
3	REEL_POS2_H
4	
5	AGND

MODE SW
P22
VJP3172D004

1	MECHA_POS1_L
2	MECHA_POS2_L
3	MECHA_POS3_L
4	AGND

LOADING MOTOR
P21
VJP3518D002

1	UNLOADING
2	LOADING

PINCH SOL
P20
VJP3518D003

1	PINCH_ON
2	
3	PINCH_OFF

M STOPPER SOL
P24
VJP3518D002

1	M_STOPPER_ON
2	M_STOPPER_OFF

T SENSOR
P19
VJP3172D002

1	TAPE_START_L
2	AGND

T BRK SOL
P18
VJP3518D002

1	T_BRAKE_ON
2	T_BRAKE_OFF

FRONT MOTOR
P25
VJP1230T

1	F_LOAD_IN
2	
3	F_LOAD_OUT

CARRIGE
P26
VJP1236T

1	+5V
2	CASSET_INR_H
3	CASSET_INL_H
4	CASSET1_H
5	CASSET2_H
6	CASSET_UP_L
7	CASSET_MID_H
8	CASSET_DOWN_H
9	AGND

REEL STAND MOTOR
P16
VJP3518D003

1	R_STAND_L2S
2	
3	R_STAND_S2L

S BRK SOL
P15
VJP3518D002

1	S_BRAKE_ON
2	S_BRAKE_OFF

TOHDAI
P14
VJP3172D003

1	TAPE_SENSOR_ON
2	
3	TAPE_SENSOR_GND

S SENSOR
P13
VJP3172D002

1	TAPE_END_L
2	AGND

DEW
P11
VJP3172D002

1	DEW_ON_H
2	DEW_GND

LOADING MOTOR FG
P23
VJP3172D004

1	L_FG_VCC
2	LOAD_FG_M
3	
4	AGND

T REEL
P35
VJS2889A017

1	T_FG_VCC
2	T_FG1_M
3	T_FG_GND
4	T_FG2_M
5	TRH_V-
6	TRH3-
7	TRH_V+
8	TRH3+
9	TRM1
10	TRH2-
11	TRH_V+
12	TRH2+
13	TRM3
14	TRH1-
15	TRH_V+
16	TRH1+
17	TRM2

S REEL
P34
VJS2889A017

1	S_FG_VCC
2	S_FG1_M
3	S_FG_GND
4	S_FG2_M
5	SRH_V-
6	SRH3-
7	SRH_V+
8	SRH3+
9	SRM1
10	SRH2-
11	SRH_V+
12	SRH2+
13	SRM3
14	SRH1-
15	SRH_V+
16	SRH1+
17	SRM2

CLEANING SOL
P48
VJP3125D002

1	CLEANING_GND
2	CLEANING_ON

CASSET DOWN
P41
VJP3172D002

1	CAST_DOWN_L
2	AGND

CYL
P33
VJS3406D015

1	CYLH3-
2	CYLH3+
3	CYLH2-
4	CYLH2+
5	CYLH1-
6	CYLH1+
7	CYLH_V-
8	CYLH_V+
9	CYL_FG+
10	CYL_PF_GND (CYL_FG-)
11	CYL_PG+
12	CYL_PF_GND (CYL_FG-)
13	CYL_M1
14	CYL_M2
15	CYL_M3

TENSION
P32
VJP3172D004

1	TEN_VCC
2	TEN+
3	TEN_VEE
4	TEN-

CTL
P30
VJP3172D003

1	CTL_HEAD_P
2	
3	CTL_HEAD_G

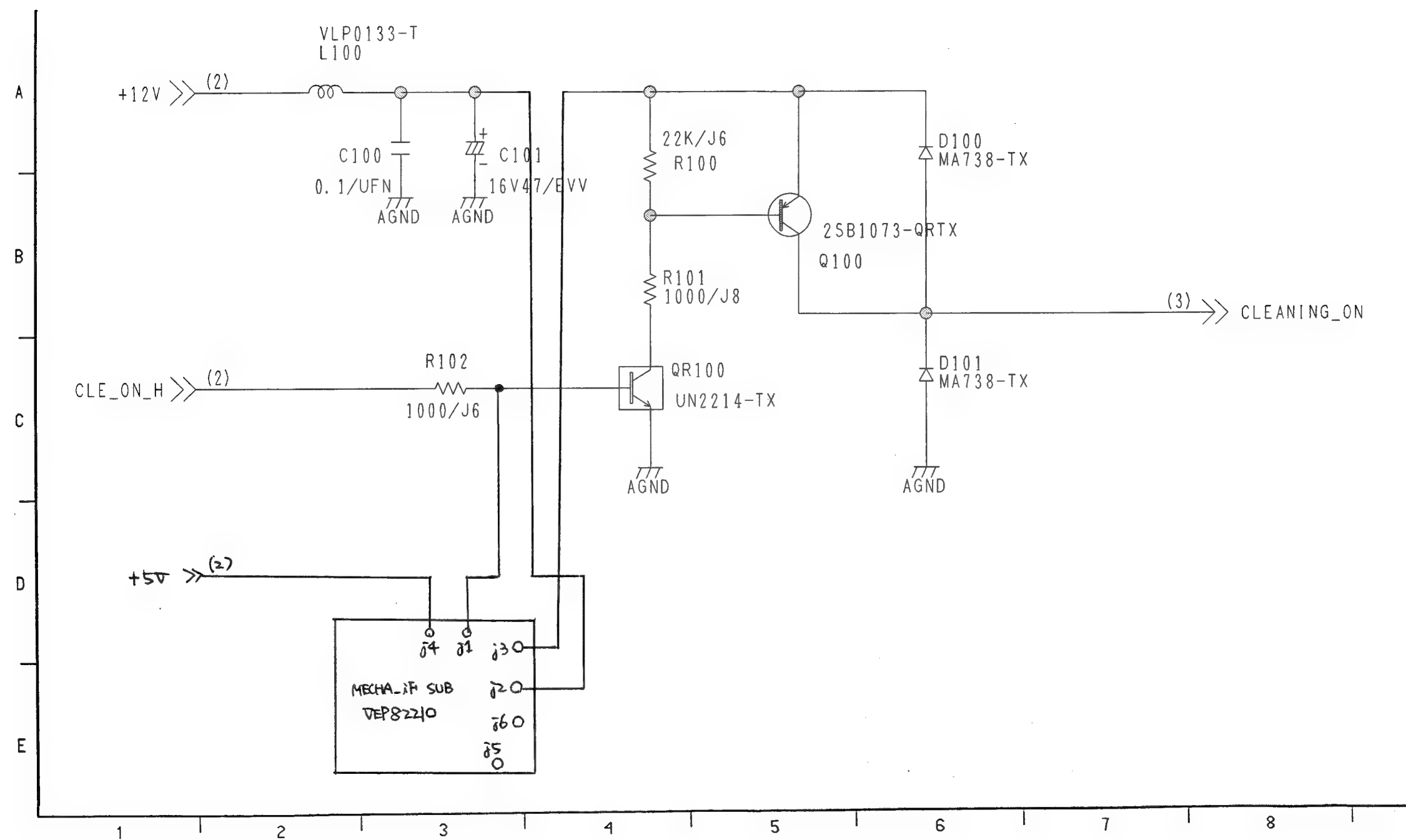
CAPSTAN
P36
VJS3406D019

1	CAP_FG2_M
2	CAP_FG_GND
3	CAP_FG1_M
4	CAP_FG_VCC
5	CAM3
6	CAM2
7	CAH_V+
8	CAH2+
9	CAH_V-
10	CAH2-
11	CAH1-
12	CAH_V+
13	CAH1+
14	CAH_V-
15	CAH_V-
16	CAH3-
17	CAH_V+
18	CAH3+
19	CAM1

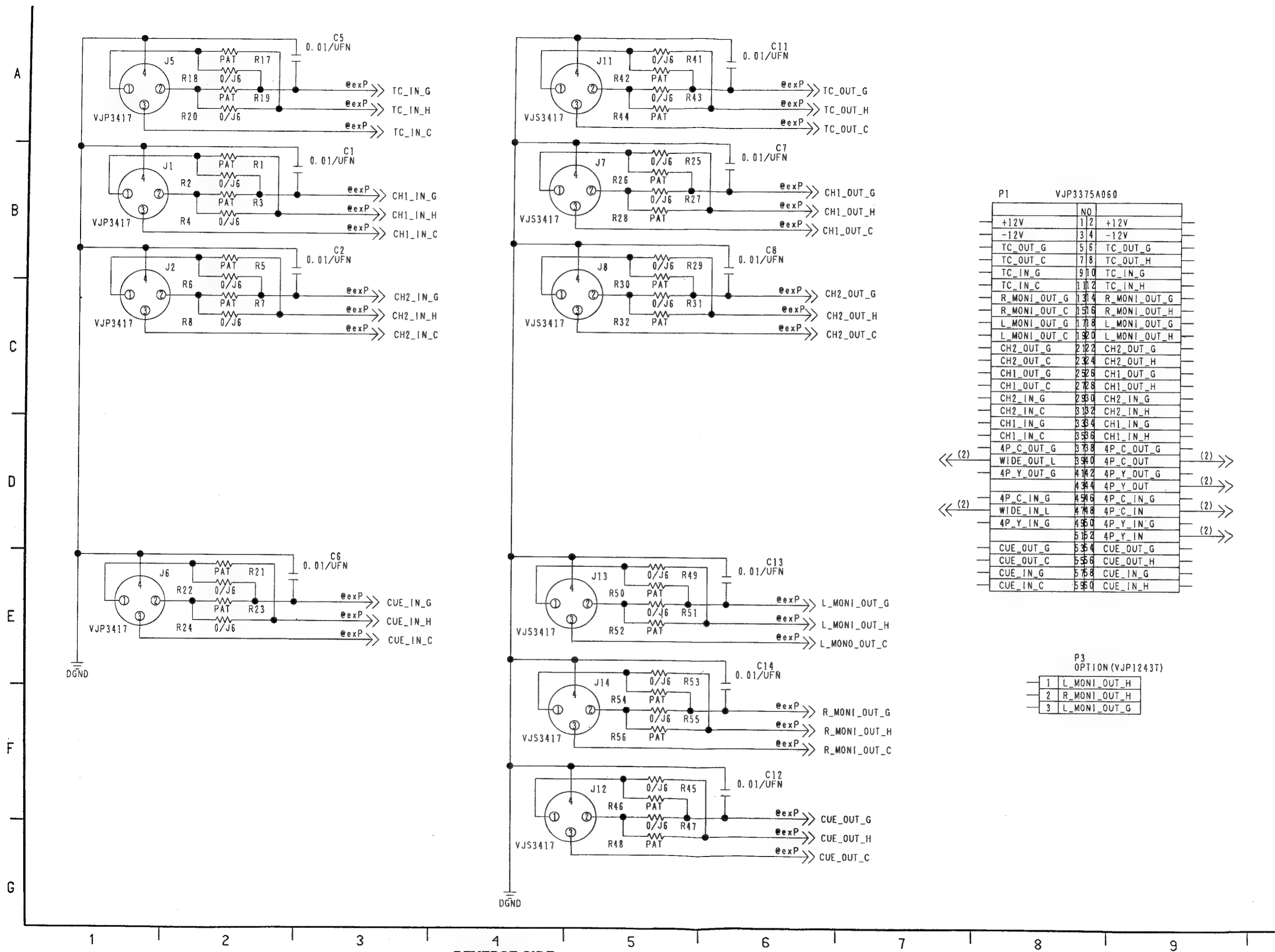
Wiring Details:

- Pin 10 of MIC UNIT is connected to Pin 5 of REEL STAND POS.
- Pin 4 of REEL STAND POS is connected to Pin 4 of MODE SW.
- Pin 4 of MODE SW is connected to Pin 4 of LO

MECHA I/F (4/4) SCHEMATIC DIAGRAM



A JACK (1/2) SCHEMATIC DIAGRAM



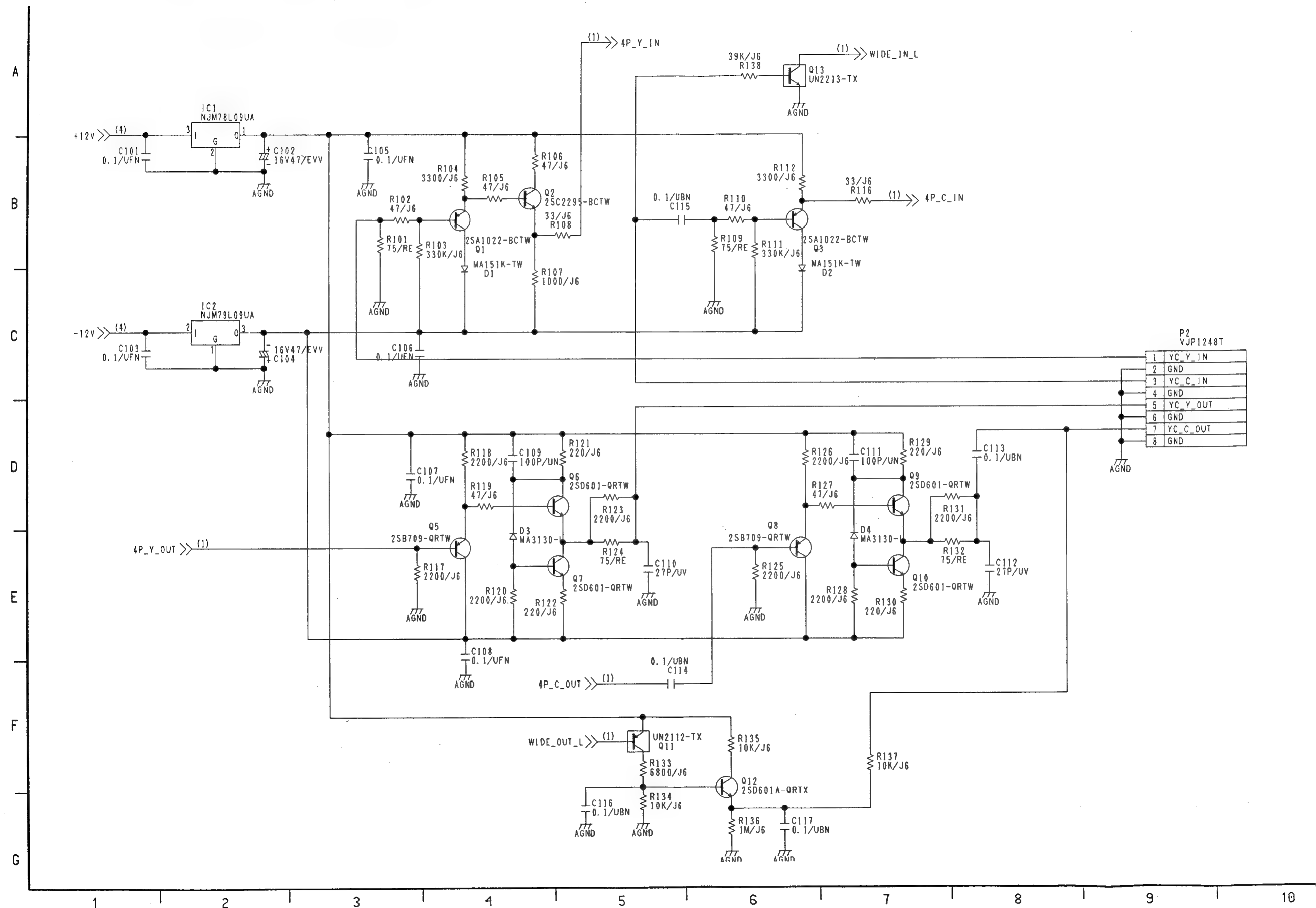
P1 VJP3375A060

+12V	1 2	+12V
-12V	3 4	-12V
TC_OUT_G	5 6	TC_OUT_G
TC_OUT_C	7 8	TC_OUT_H
TC_IN_G	9 10	TC_IN_G
TC_IN_C	11 12	TC_IN_H
R_MONI_OUT_G	13 14	R_MONI_OUT_G
R_MONI_OUT_C	15 16	R_MONI_OUT_H
L_MONI_OUT_G	17 18	L_MONI_OUT_G
L_MONI_OUT_C	19 20	L_MONI_OUT_H
CH2_OUT_G	21 22	CH2_OUT_G
CH2_OUT_C	23 24	CH2_OUT_H
CH1_OUT_G	25 26	CH1_OUT_G
CH1_OUT_C	27 28	CH1_OUT_H
CH2_IN_G	29 30	CH2_IN_G
CH2_IN_C	31 32	CH2_IN_H
CH1_IN_G	33 34	CH1_IN_G
CH1_IN_C	35 36	CH1_IN_H
4P_C_OUT_G	37 38	4P_C_OUT_G
WIDE_OUT_L	39 40	4P_C_OUT
4P_Y_OUT_G	41 42	4P_Y_OUT_G
4P_Y_OUT	43 44	4P_Y_OUT
4P_C_IN_G	45 46	4P_C_IN_G
WIDE_IN_L	47 48	4P_C_IN
4P_Y_IN_G	49 50	4P_Y_IN_G
4P_Y_IN	51 52	4P_Y_IN
CUE_OUT_G	53 54	CUE_OUT_G
CUE_OUT_C	55 56	CUE_OUT_H
CUE_IN_G	57 58	CUE_IN_G
CUE_IN_C	59 60	CUE_IN_H

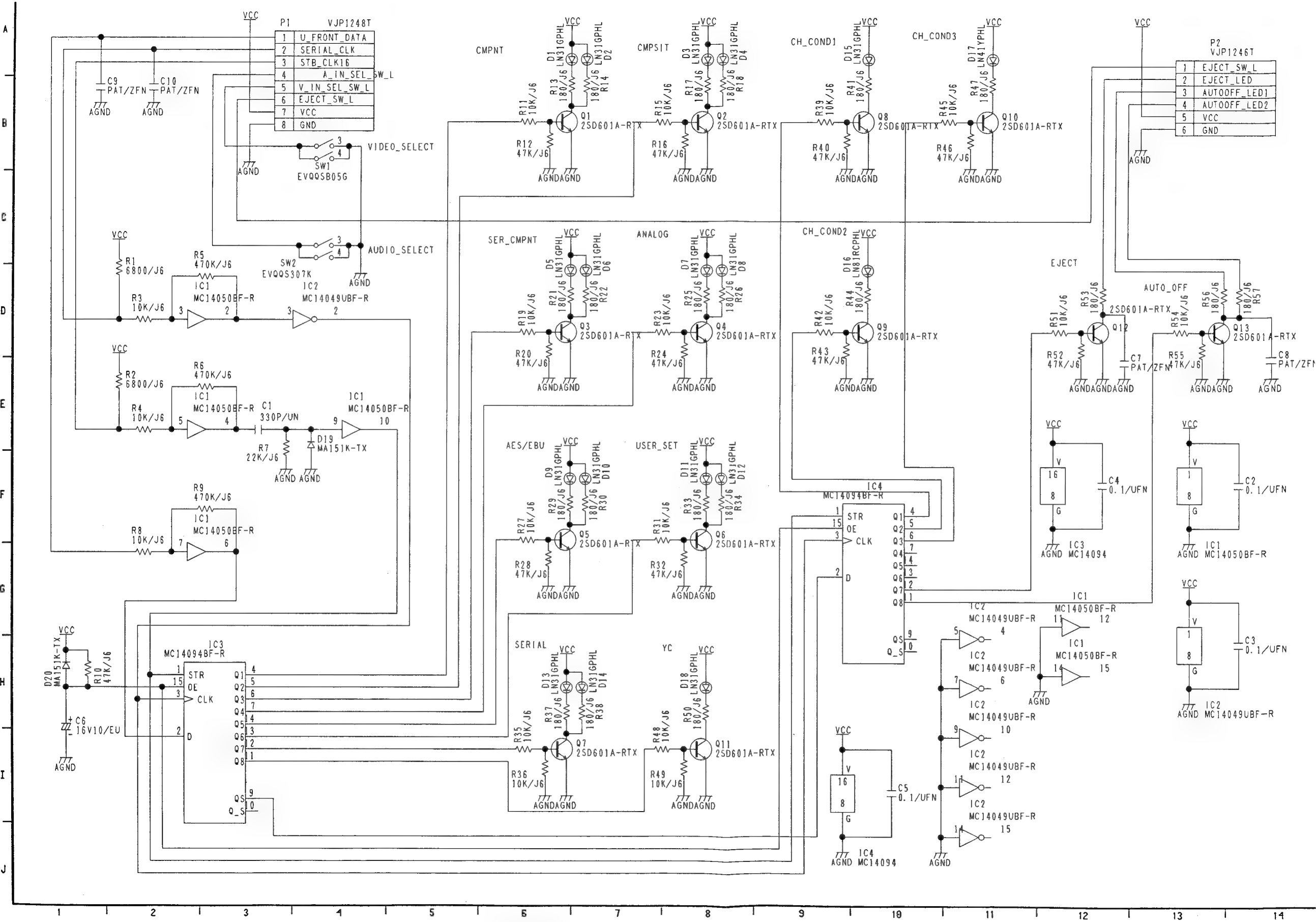
P3 OPTION (VJP1243T)

1	L_MONI_OUT_H
2	R_MONI_OUT_H
3	L_MONI_OUT_G

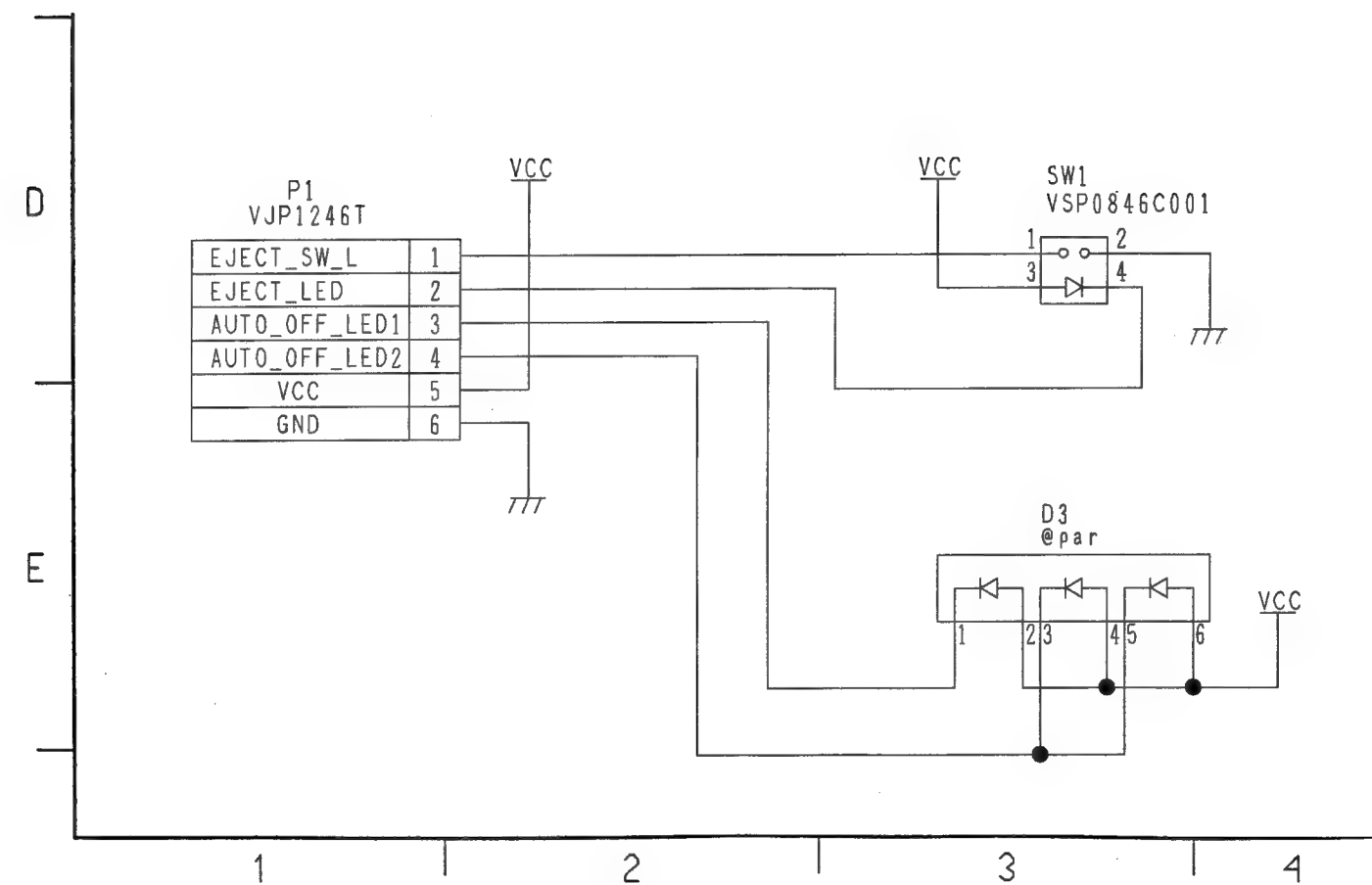
A JACK (2/2) SCHEMATIC DIAGRAM



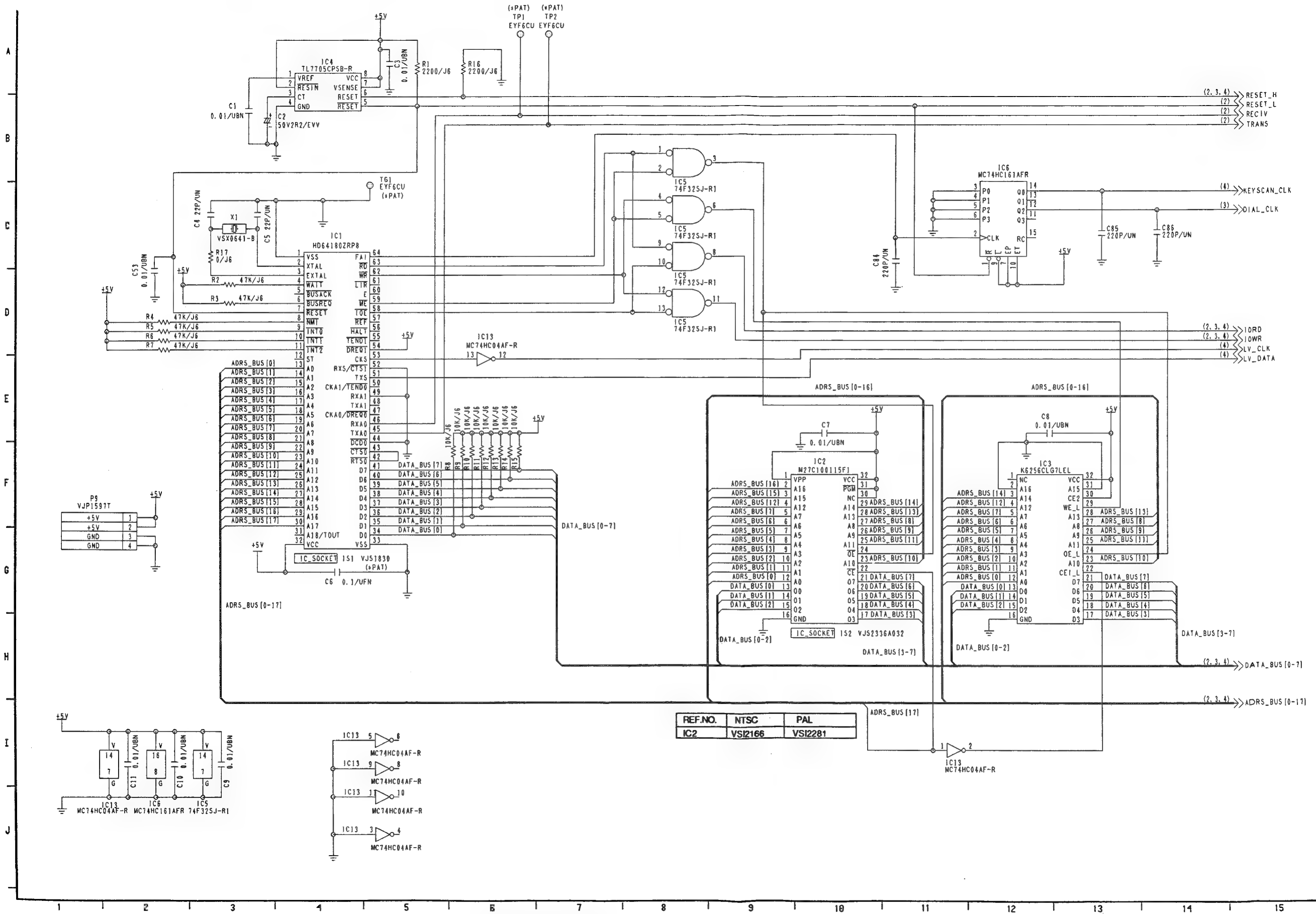
UP FRONT 1 SCHEMATIC DIAGRAM



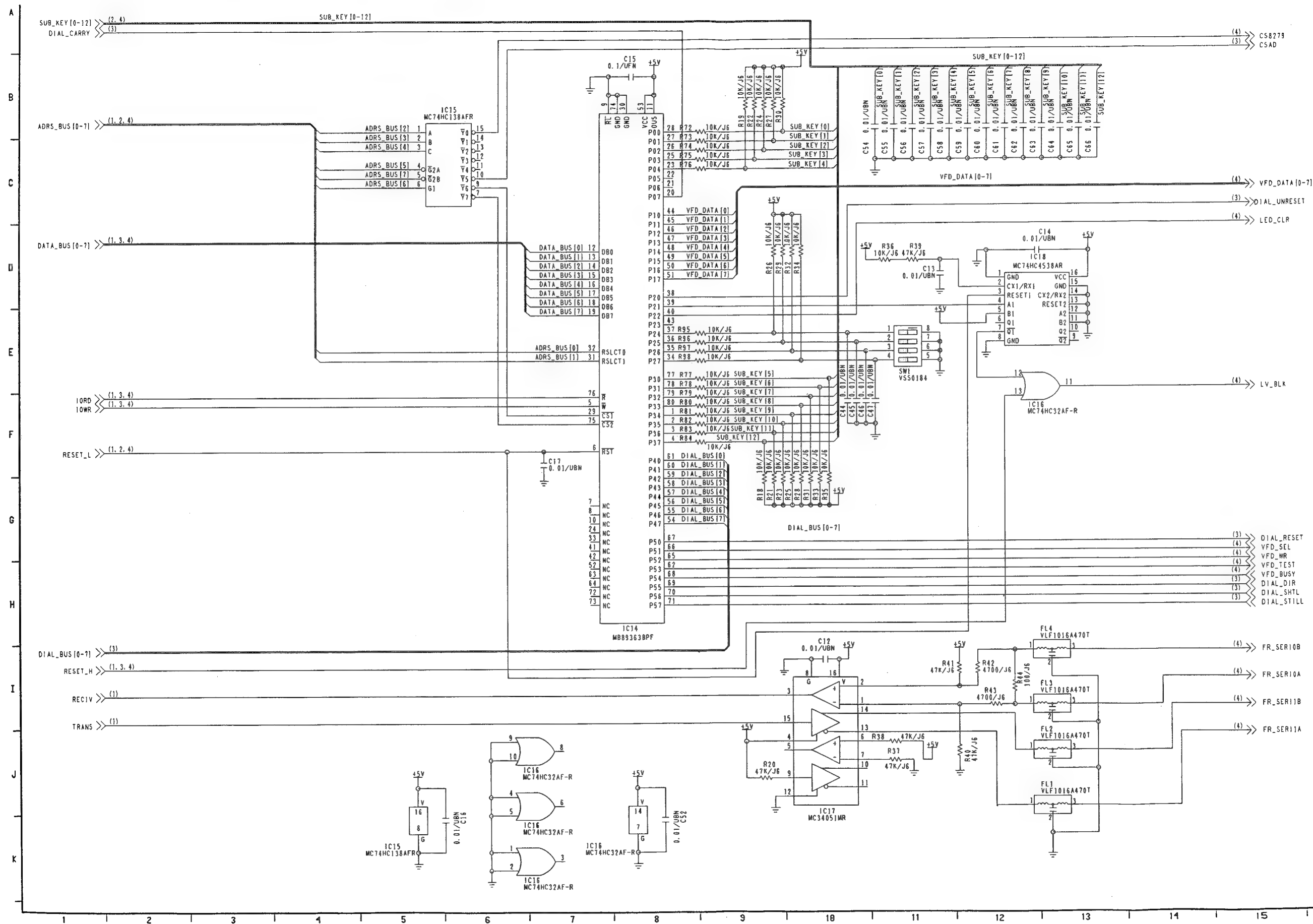
UP FRONT 2 SCHEMATIC DIAGRAM



FRONT CPU (1/4) CPU SCHEMATIC DIAGRAM



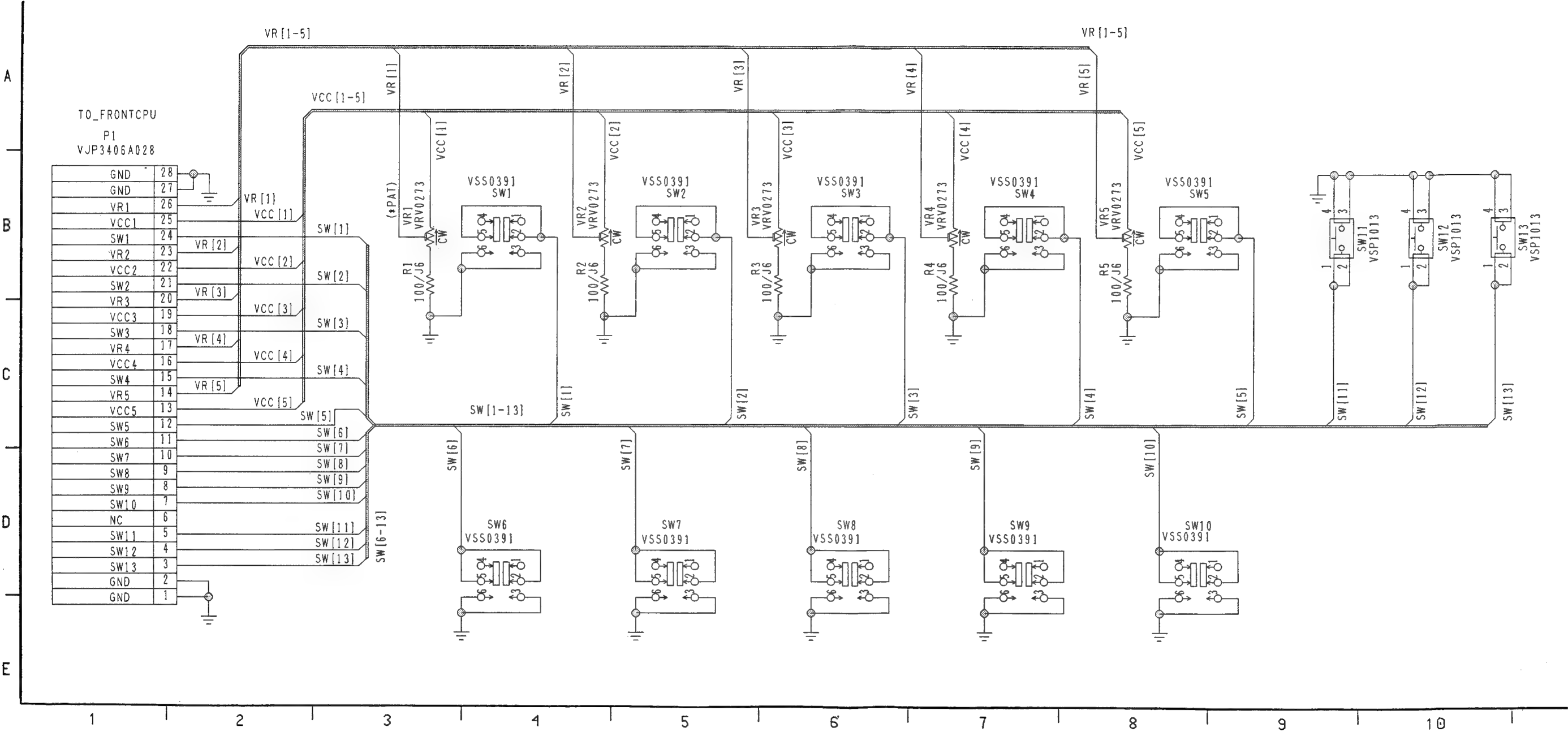
FRONT CPU (2/4) PIO SCHEMATIC DIAGRAM



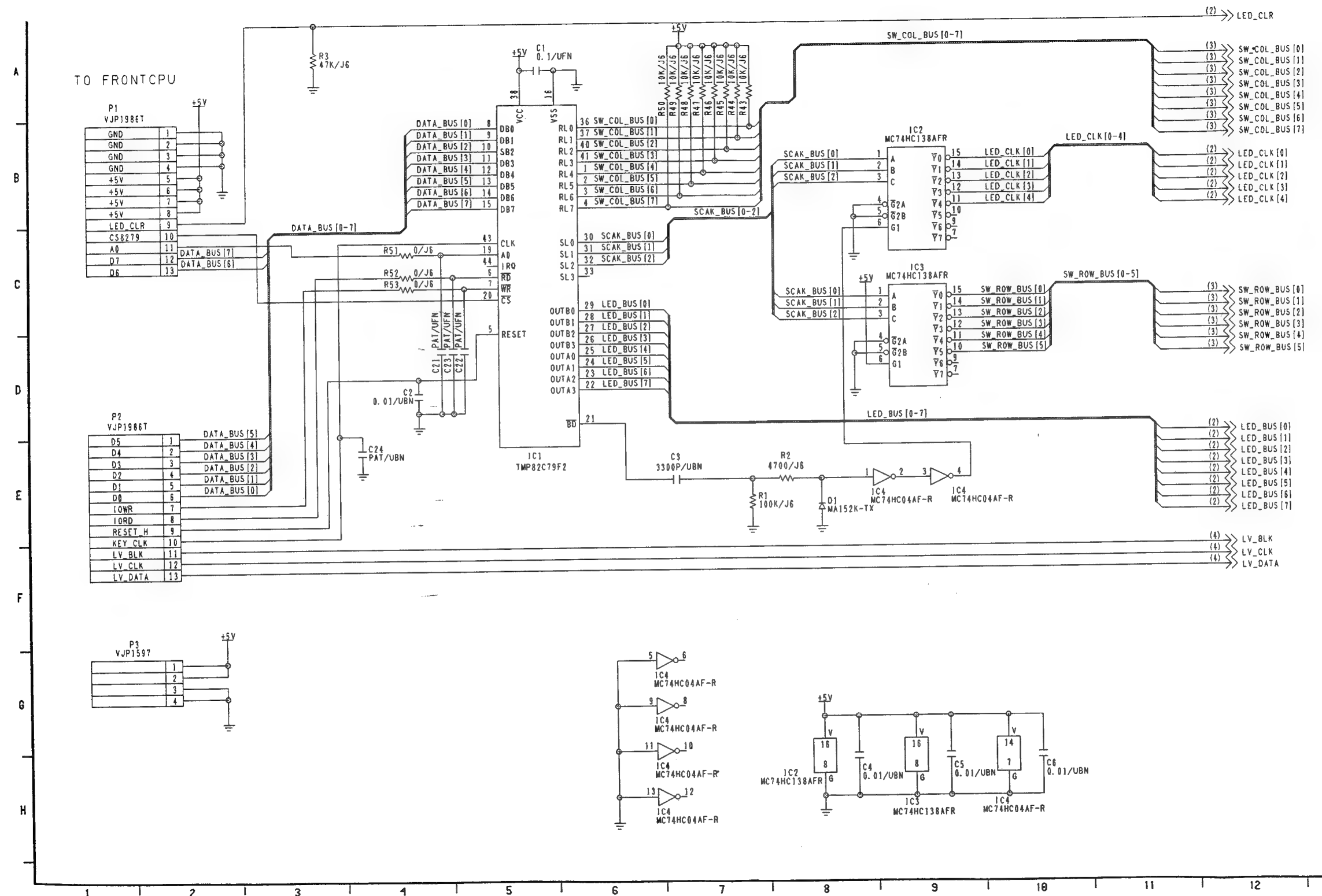
The schematic diagram illustrates the electrical connections for a device, organized into sections A through I. Key components and connections include:

- Connectors:**
 - P1 VJP1942T:** Pins 1-13 connected to GND, +5V, LED_CLR, CS8279, ADRS_BUS[0], DATA_BUS[6-7], and DATA_BUS[16].
 - P2 VJP1942T:** Pins 1-13 connected to DATA_BUS[5], DATA_BUS[4], DATA_BUS[3], DATA_BUS[2], DATA_BUS[1], DATA_BUS[0], IOWR, IORD, RESET_H, KEYSKAN_CLK, LV_BLK, LV_CLK, and LV_DATA.
 - P3 VJP3440A016:** Pins 1-16 connected to VR_SW[2], VR_SW[1], VR_SW[3], VR_SW[0], VR_SW[4], GND, VR_A[5], VR_A[4], VR_A[0], VR_A[3], VR_A[1], VR_A[11], REGA+5V, REGA+5V, GND, and VR_A[2].
 - P4 TO_FRONTVR2 VJP3440A016:** Pins 1-16 connected to VR_SW[6], VR_SW[7], HP_R, VR_SW[8], HP_L, VR_SW[9], VR_SW[5], GND, VR_B[0], VR_B[4], HP_G2, VR_B[3], REGB+5V, REGB+5V, VR_B[1], and VR_B[2].
 - P5 VJP2891A016:** Pins 1-16 connected to HP_G, HP_R, HP_L, HP_G, GND, GND, AGND, FR_SERI1B, FR_SERI1A, FR_SERI0B, FR_SERI0A, +5V, +5V, +7.5, and +5V.
 - P6 VJS3281A020:** Pins 1-20 connected to VFD_DATA[7], +5V, VFD_DATA[6], +5V, VFD_DATA[5], +5V, VFD_DATA[4], VFD_TEST, VFD_DATA[3], GND, VFD_DATA[2], GND, VFD_DATA[1], GND, VFD_DATA[0], VFD_WR, VFD_SEL, and VFD_BUSY.
 - P7 VJS2698A028:** Pins 1-28 connected to GND, GND, SUB_KEY[12], SUB_KEY[11], SUB_KEY[10], SUB_KEY[9], SUB_KEY[8], SUB_KEY[7], SUB_KEY[6], SUB_KEY[5], SUB_KEY[4], REGB+5V, VR_B[7], SUB_KEY[3], REGB+5V, VR_B[6], SUB_KEY[2], REGB+5V, VR_B[5], SUB_KEY[1], REGA+5V, VR_A[7], SUB_KEY[0], REGA+5V, VR_A[16], GND, and GND.
 - P8 VJP1233T:** Pins 1-6 connected to +5V, D_STILL, D_SHTL, D_DATA0, D_DATA1, and GND.
- Components and Signals:**
 - Resistors:** R99, R100, R124, R125, R126, R127, R128, R105, R106, R107, R71.
 - Capacitors:** C48, C38, C39, C83.
 - Inductors:** L1, L2.
 - Transformer:** VLP0133-T.
 - Signals:** LED_CLR, CS8279, ADRS_BUS[0], DATA_BUS[0-7], IOWR, IORD, RESET_H, KEYSKAN_CLK, LV_BLK, LV_CLK, LV_DATA, VR_SW[0-9], VR_A[0-7], VR_B[0-7], SUB_KEY[0-12], VFD_DATA[0-7], VFD_TEST, VFD_WR, VFD_SEL, VFD_BUSY.

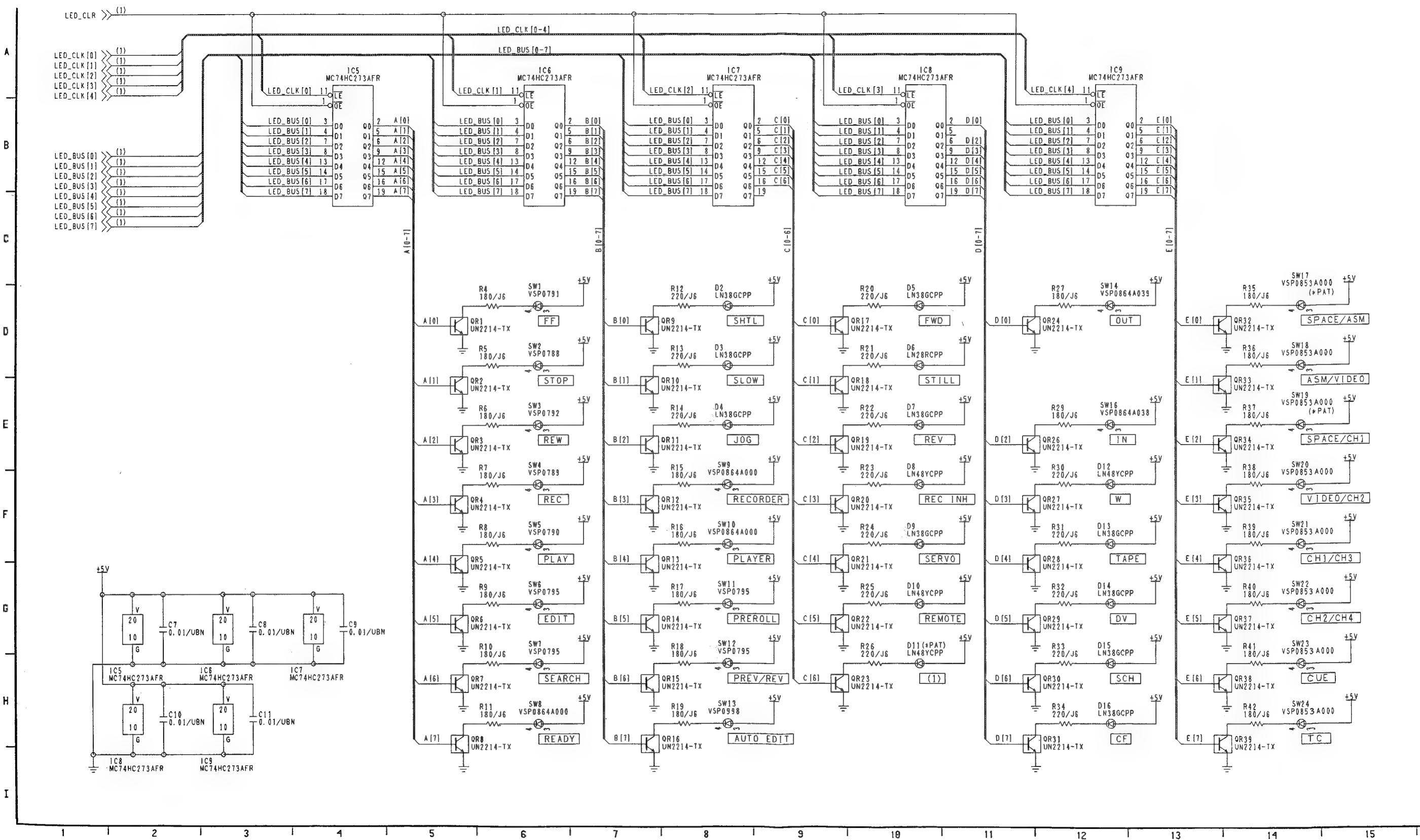
FRONT CPU SUB SCHEMATIC DIAGRAM



FRONT SW (1/4) CONTROL SCHEMATIC DIAGRAM

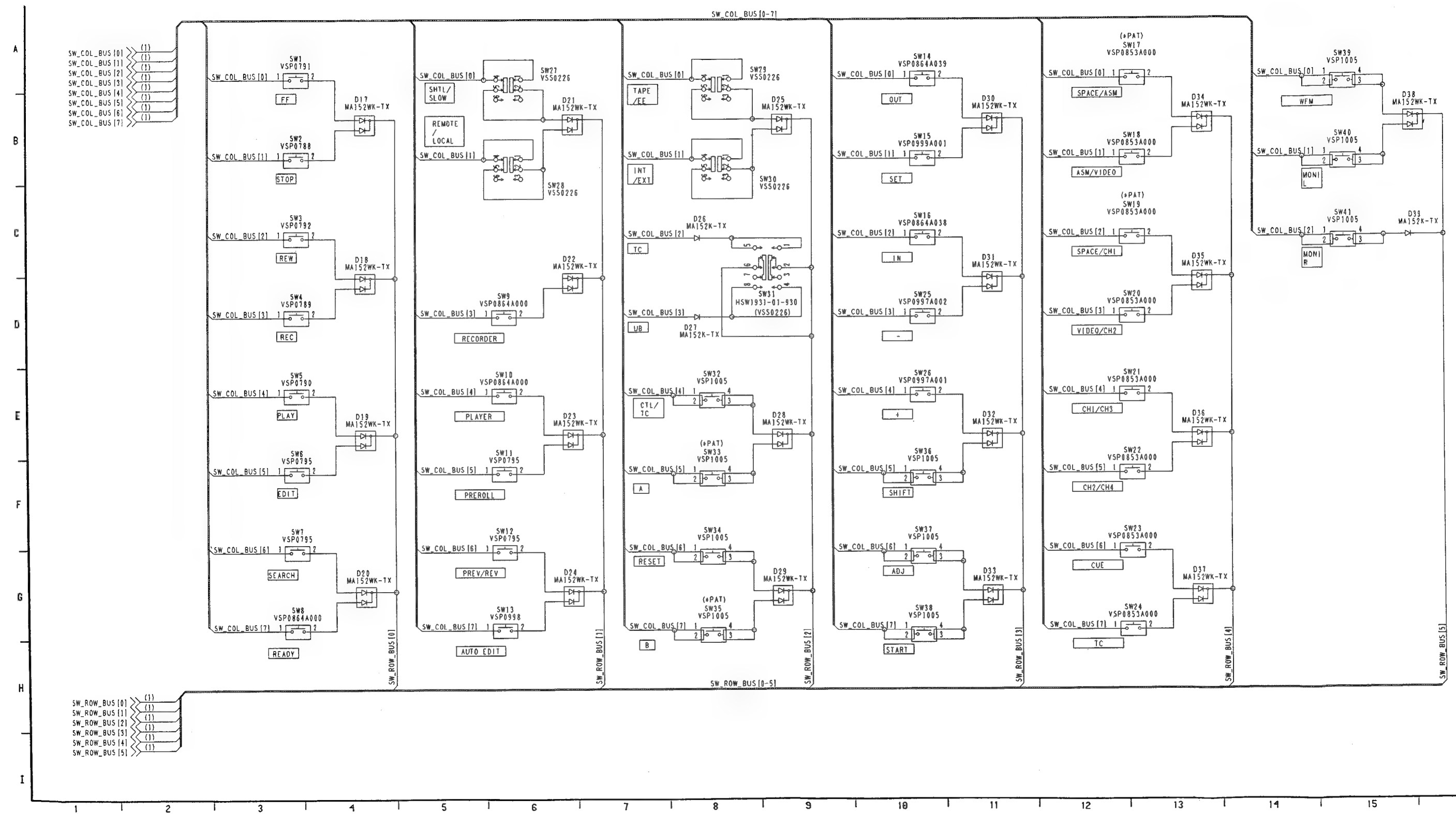


FRONT SW (2/4) LED SCHEMATIC DIAGRAM

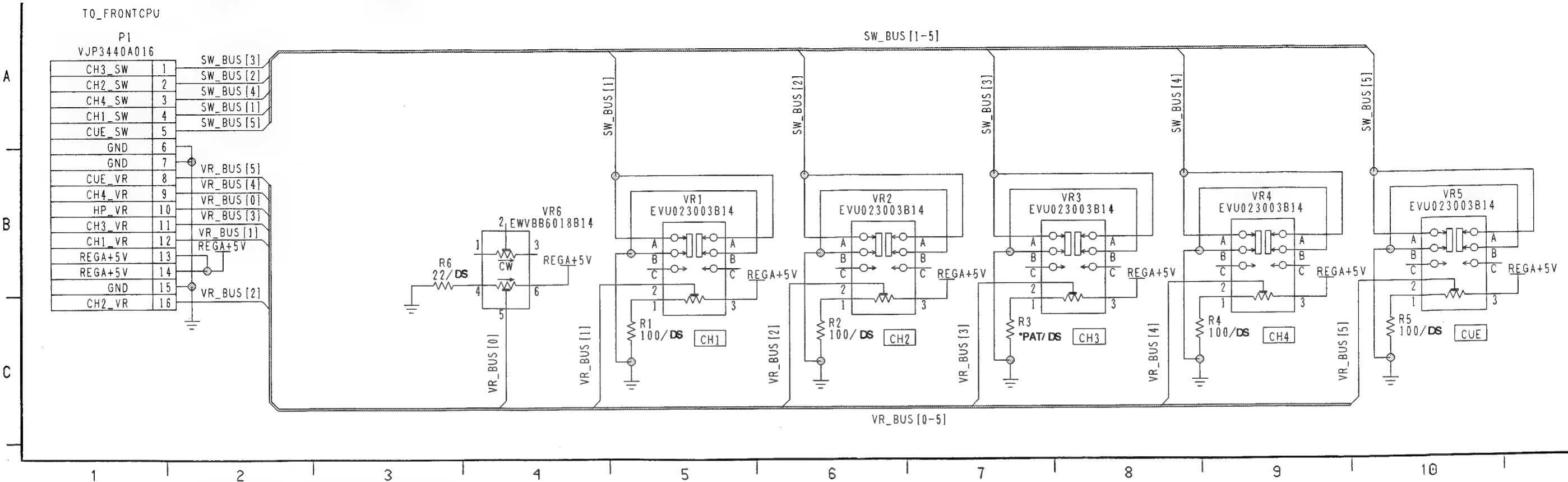


REVERSE SIDE
FRONT SW 1/4

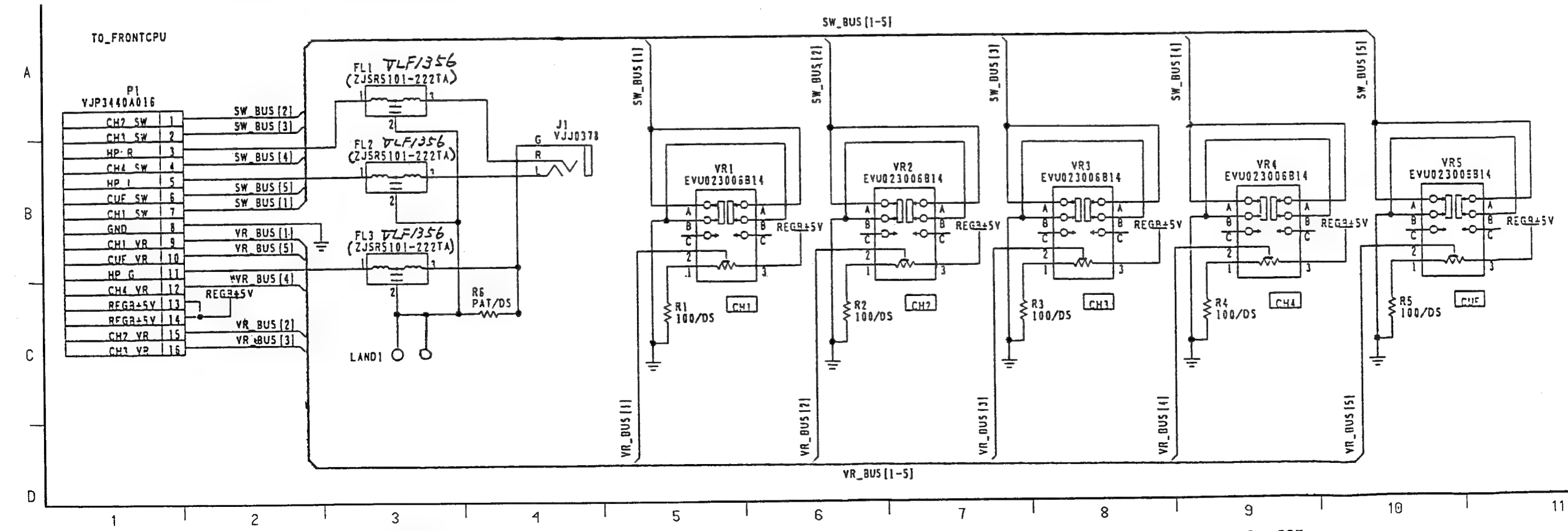
FRONT SW (3/4) SW SCHEMATIC DIAGRAM



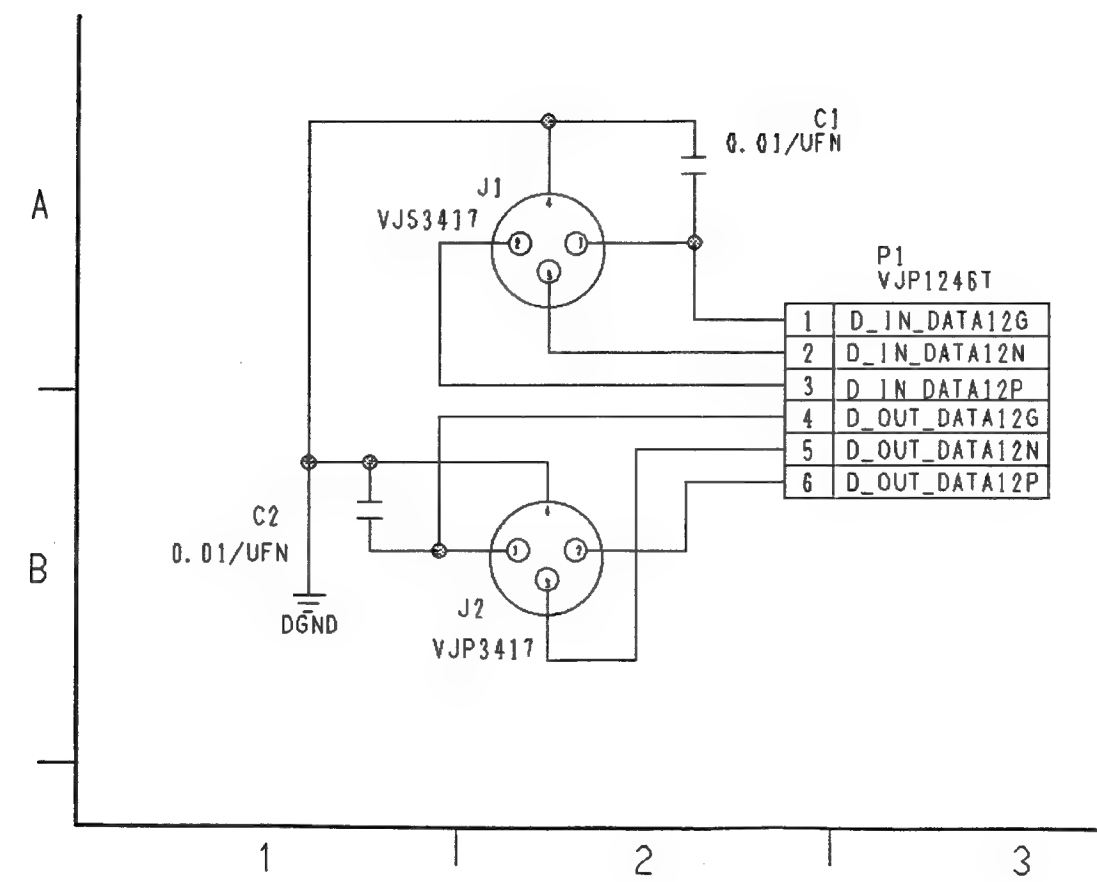
FRONT VR 1 SCHEMATIC DIAGRAM



FRONT VR 2 SCHEMATIC DIAGRAM



AES/EBU SCHEMATIC DIAGRAM



SECTION 3

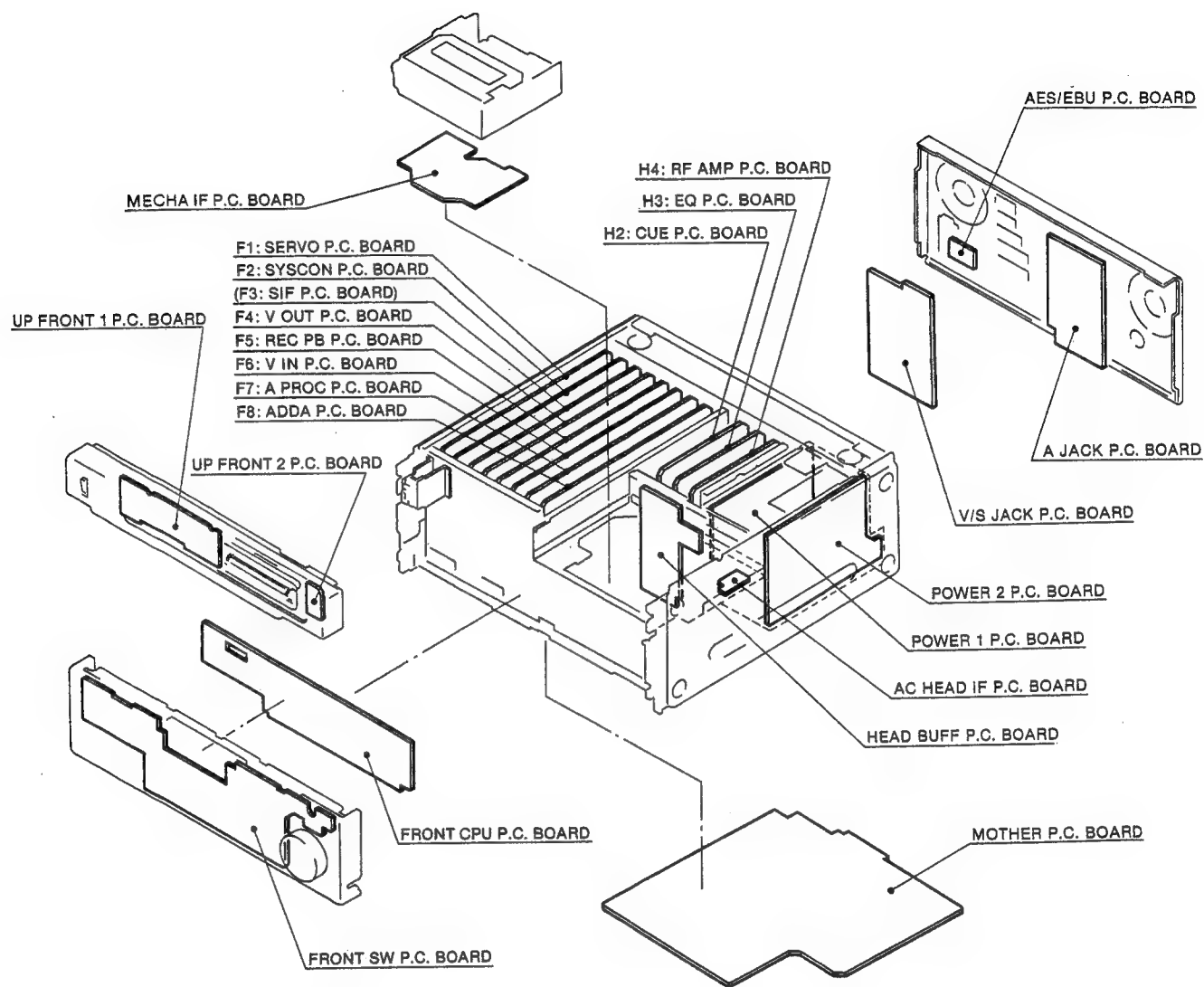
CIRCUIT BOARDS

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CIRCUIT BOARD LOCATION

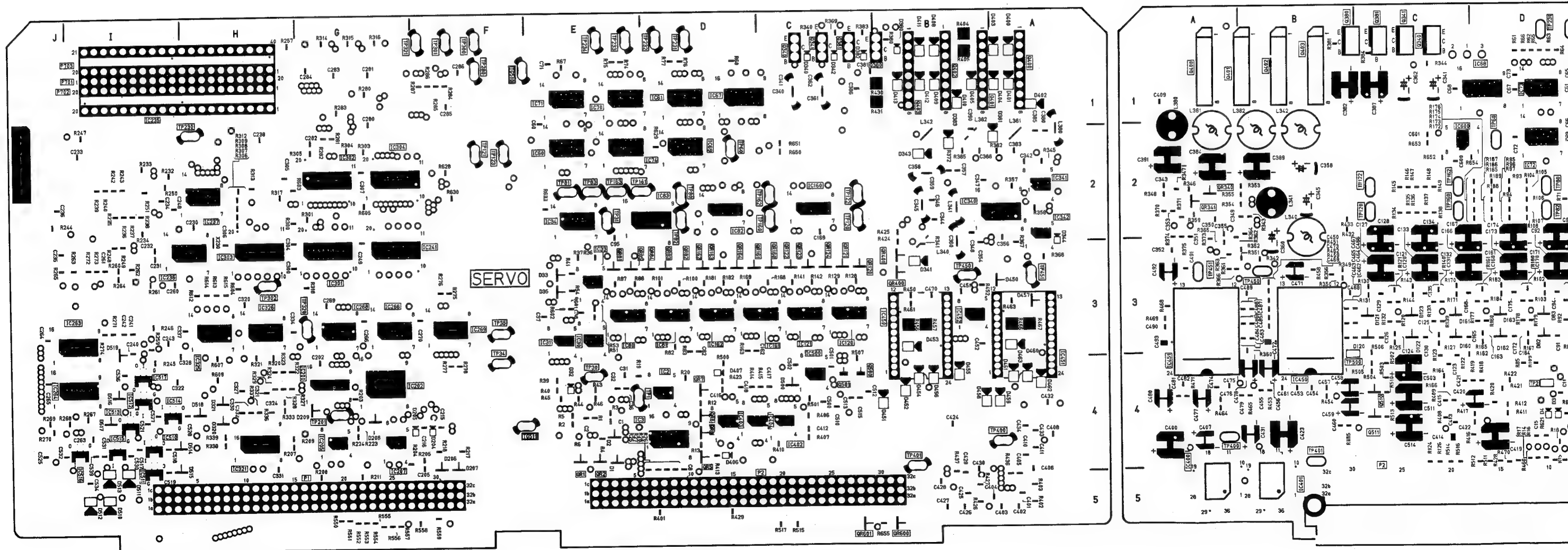


F1 SERVO										
Transistors			IC64		E-1		IC401		B-5	
Q1	E-4	Ⓢ	IC65		E-1	Ⓢ	IC402		C-4	Ⓢ
Q2	E-4	Ⓢ	IC66		E-2	Ⓢ	IC403		D-4	Ⓢ
Q3	E-4	Ⓢ	IC67		D-1	Ⓢ	IC404		C-4	Ⓢ
Q4	E-4	Ⓢ	IC68		D-1	Ⓢ	IC450		B-3	
Q5	E-4	Ⓢ	IC69		D-2	Ⓢ	IC451		A-4	
Q6	D-4	Ⓢ	IC70		E-1	Ⓢ	IC452		B-3	Ⓢ
Q340	C-1		IC71		E-1	Ⓢ	IC500		C-3	Ⓢ
Q341	C-1		IC72		D-2	Ⓢ	IC510		I-4	Ⓢ
Q380	B-1		IC73		D-1	Ⓢ	IC511		I-4	Ⓢ
Q381	C-1		IC74		D-2	Ⓢ	IC512		I-4	Ⓢ
Q400	A-1		IC80		E-3	Ⓢ	IC513		I-4	Ⓢ
Q401	A-1		IC81		D-3	Ⓢ	IC514		I-4	Ⓢ
Q402	B-1		IC82		D-2	Ⓢ	IC515		I-4	Ⓢ
Q403	B-1		IC83		D-2	Ⓢ	IC516		I-4	Ⓢ
Q500	C-4	Ⓢ	IC120		C-3	Ⓢ	IC517		I-4	Ⓢ
Q501	C-4	Ⓢ	IC121		C-3	Ⓢ	IC600		C-2	Ⓢ
Q510	C-4	Ⓢ	IC160		C-2	Ⓢ	Test Points			
Q511	C-4	Ⓢ	IC161		C-3	Ⓢ				
Transistor-Resistors			IC162		D-3	Ⓢ	TP1		E-4	
QR1	E-4	Ⓢ	IC200		G-4	Ⓢ	TP2		D-4	Ⓢ
QR2	E-4	Ⓢ	IC201		G-4	Ⓢ	TP30		E-4	
QR3	E-4	Ⓢ	IC202		G-4	Ⓢ	TP31		E-2	
QR4	D-4	Ⓢ	IC203		F-4	Ⓢ	TP32		E-3	Ⓢ
QR5	D-4	Ⓢ	IC204		G-2	Ⓢ	TP33		E-3	Ⓢ
QR6	D-4	Ⓢ	IC205		G-4	Ⓢ	TP34		F-3	
QR7	D-4	Ⓢ	IC207		G-4	Ⓢ	TP35		F-3	
QR8	D-4	Ⓢ	IC230		I-1	Ⓢ	TP60		D-2	
QR81	E-3	Ⓢ	IC231		I-3	Ⓢ	TP80		D-2	
QR82	E-3	Ⓢ	IC235		I-1		TP81		E-2	
QR83	D-3	Ⓢ	IC236		I-3	Ⓢ	TP82		D-2	
QR84	D-3	Ⓢ	IC237		H-2	Ⓢ	TP83		E-2	
QR85	E-3	Ⓢ	IC238		I-2	Ⓢ	TP120		C-2	
QR120	C-3	Ⓢ	IC239		I-2	Ⓢ	TP121		F-2	
QR121	C-3	Ⓢ	IC240		H-2	Ⓢ	TP122		C-2	
QR122	C-3	Ⓢ	IC241		F-3	Ⓢ	TP123		F-2	
QR123	C-3	Ⓢ	IC260		H-3	Ⓢ	TP160		C-2	
QR124	C-3	Ⓢ	IC261		J-3	Ⓢ	TP161		D-2	
QR160	C-3	Ⓢ	IC262		I-3	Ⓢ	TP162		C-2	
QR161	C-3	Ⓢ	IC263		I-3	Ⓢ	TP163		E-2	
QR162	D-3	Ⓢ	IC264		J-4	Ⓢ	TP200		G-4	Ⓢ
QR163	D-3	Ⓢ	IC265		F-3	Ⓢ	TP201		G-4	
QR164	D-3	Ⓢ	IC266		G-3	Ⓢ	TP202		G-4	Ⓢ
QR340	A-2	Ⓢ	IC267		G-3	Ⓢ	TP230		H-1	
QR341	A-2	Ⓢ	IC268		G-3	Ⓢ	TP231		D-1	
QR400	B-2	Ⓢ	IC269		F-3	Ⓢ	TP232		D-1	
QR401	B-3	Ⓢ	IC280		F-1	Ⓢ	TP233		E-1	
QR600	B-5	Ⓢ	IC281		F-1	Ⓢ	TP234		E-1	
QR801	C-5	Ⓢ	IC282		G-2	Ⓢ	TP280		F-1	
Integrated Circuits			IC300		H-2	Ⓢ	TP300		F-1	
IC1	E-4	Ⓢ	IC301		G-3	Ⓢ	TP301		F-1	
IC2	D-4	Ⓢ	IC302		G-2	Ⓢ	TP302		H-3	
IC3	E-4	Ⓢ	IC303		H-3	Ⓢ	TP320		G-3	
IC30	E-3	Ⓢ	IC304		G-2	Ⓢ	TP321		F-1	
IC31	E-3	Ⓢ	IC305		G-2	Ⓢ	TP400		A-4	
IC32	E-4	Ⓢ	IC320		H-4	Ⓢ	TP401		B-4	
IC33	E-3	Ⓢ	IC321		H-4	Ⓢ	TP450		B-3	
IC34	E-2	Ⓢ	IC322		H-3	Ⓢ	TP451		A-3	
IC35	E-3	Ⓢ	IC323		H-4	Ⓢ	TP500		B-4	Ⓢ
IC60	E-2	Ⓢ	IC324		H-3	Ⓢ	TG510		F-1	
IC81	D-1	Ⓢ	IC325		H-3	Ⓢ	TG511		F-4	
IC83	E-2	Ⓢ	IC326		H-3	Ⓢ	Connectors			
			IC340		B-2	Ⓢ				
			IC341		A-2	Ⓢ	P1		G-5	
			IC342		A-2	Ⓢ	P2		C-5	
			IC400		A-4	Ⓢ				

ADDRESS INFORMATION
 Ⓢ ... COMPONENT SIDE
 Ⓢ ... FOIL SIDE

F1 SERVO P.C. BOARD (VEP82105B)

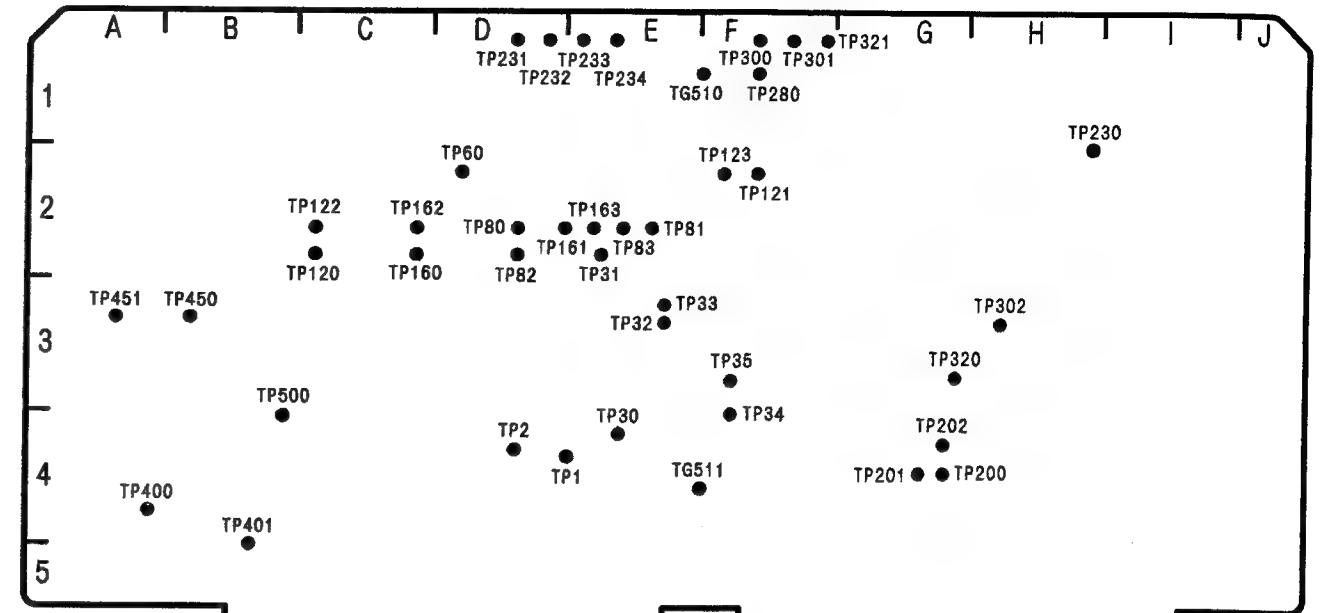
F1
1
2
3
4
5



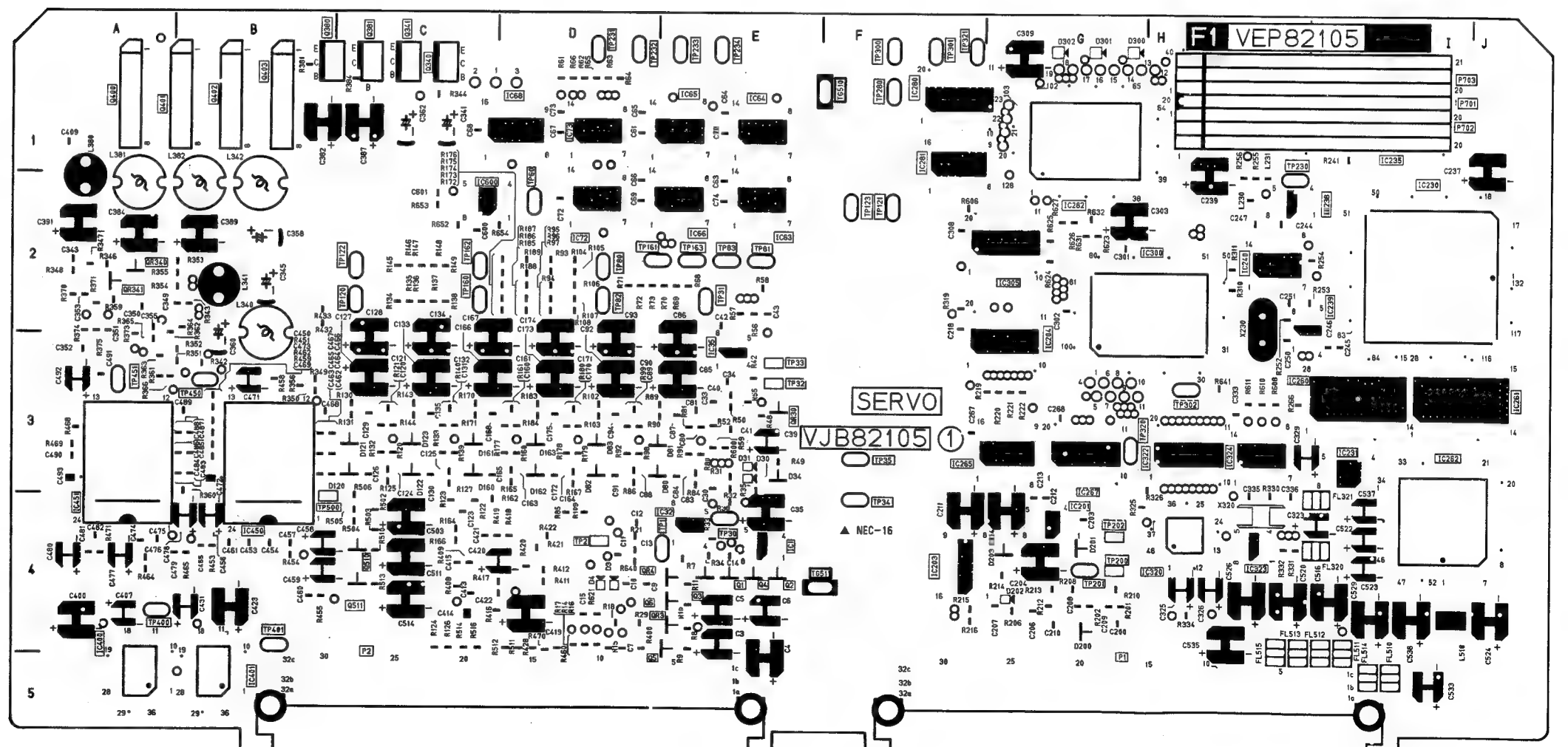
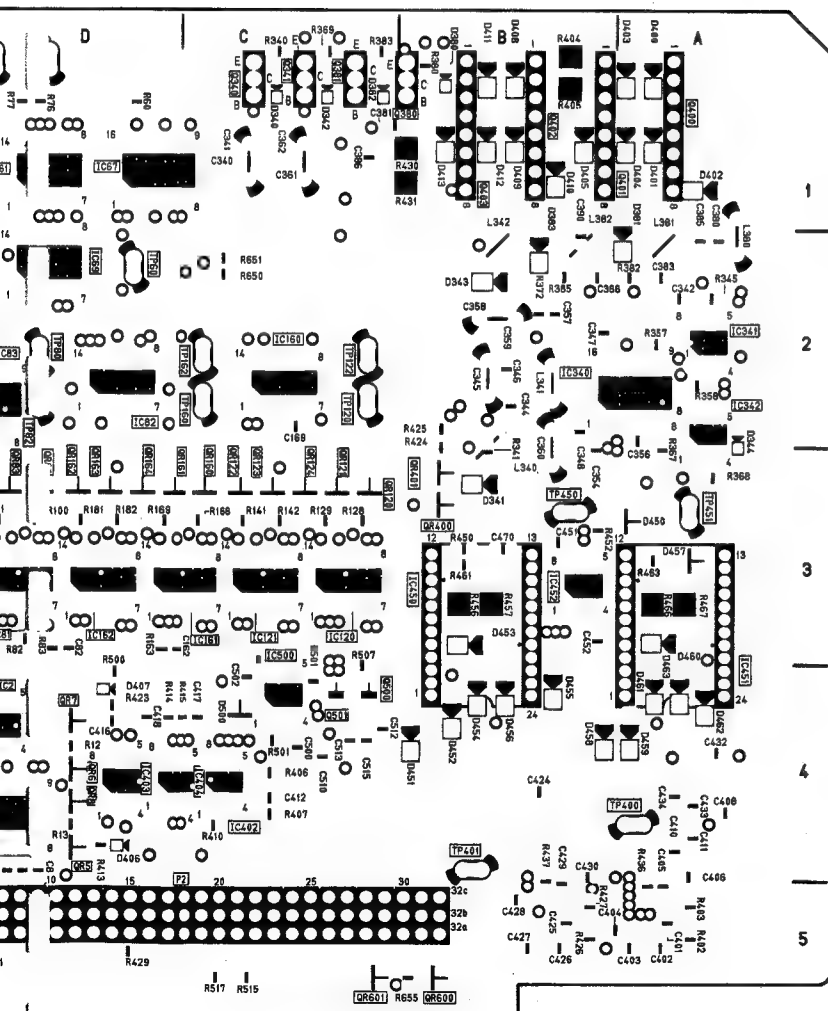
DIP →

VJB8

F1 SERVO P. C. BOARD



(COMPONENT SIDE)



VJB82105-1

DIP

F2 SYSCON P.C. BOARD (VEP86146B)

F2 SYS

A

1

2

3

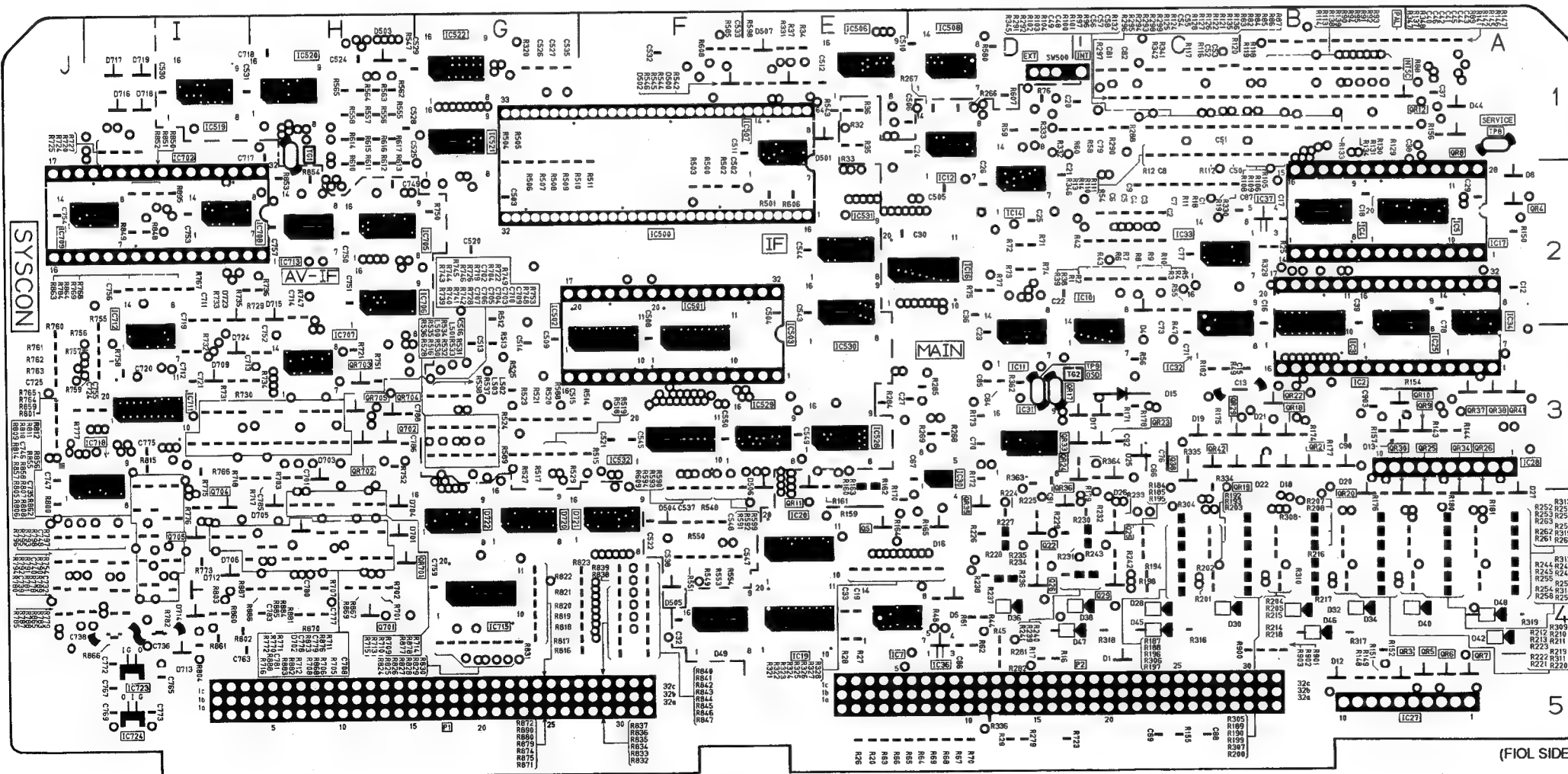
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5

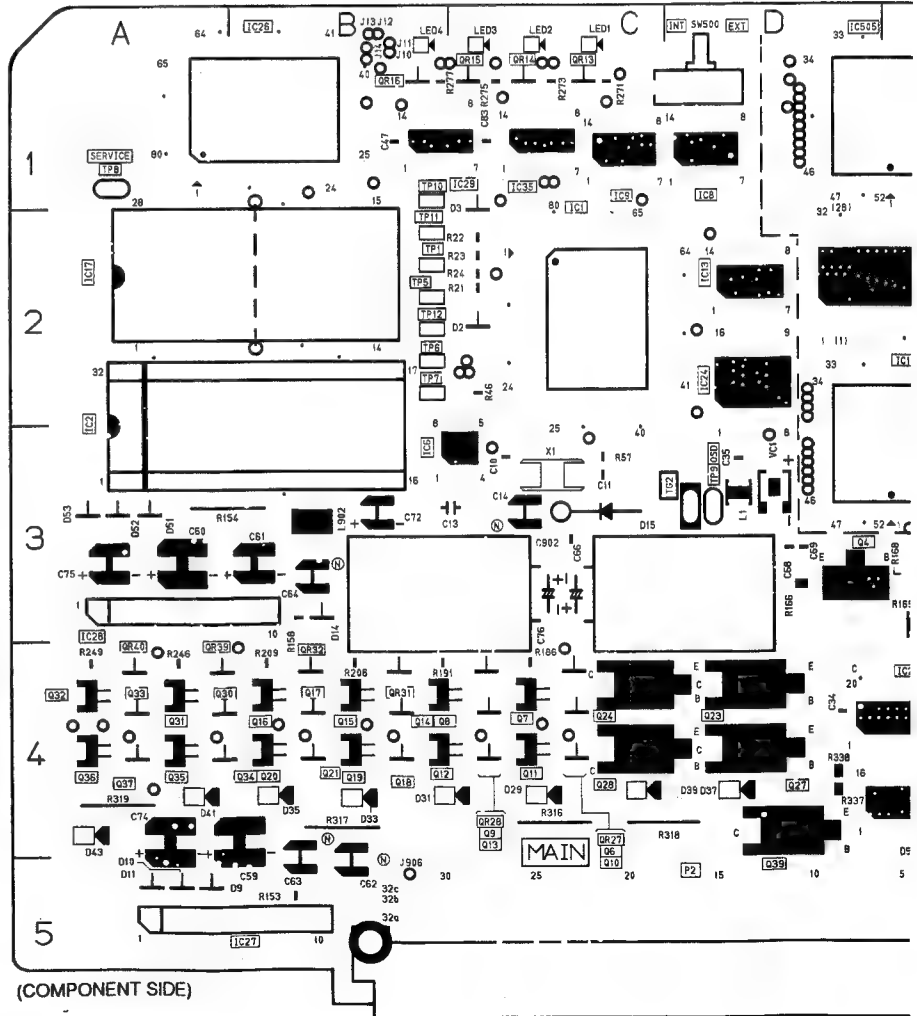
● TP8
SERV

F2 SYSCON																		
Transistors		Q26	D-4	QR7	A-4	QR32	B-4	IC9	C-1	IC37	B-2	IC525	G-1	IC720	J-4	TP504	F-2	
Q3	E-3	Q27	D-4	QR8	A-1	QR33	D-3	IC10	C-2	IC500	F-2	IC527	F-3	IC721	I-3	TP505	F-1	
Q4	D-3	Q28	C-4	QR9	A-3	QR34	A-3	IC11	D-3	IC501	F-2	IC528	E-3	IC722	I-3	TP506	F-1	
Q5	E-4	Q29	C-4	QR10	A-3	QR35	D-4	IC12	D-2	IC502	G-2	IC529	E-3	IC723	I-5	TP701	J-5	
Q6	C-4	Q30	A-4	QR11	E-4	QR36	D-3	IC13	D-2	IC504	E-2	IC530	E-3	IC724	I-5	TP702	J-5	
Q7	C-4	Q31	A-4	QR12	A-1	QR37	A-3	IC14	D-2	IC505	D-1	IC531	E-2	IC725	H-4	TG1	H-1	
Q8	B-4	Q32	A-4	QR13	C-1	QR38	A-3	IC15	E-2	IC506	E-1	IC532	F-3	IC726	H-4	TG2	D-3	
Q9	C-4	Q33	A-4	QR14	C-1	QR39	A-4	IC16	D-2	IC507	E-1	IC701	H-3	Test Points	B-2	Adjustments		
Q10	C-5	Q34	B-4	QR15	C-1	QR40	A-4	IC17	A-2	IC508	D-1	IC703	I-1			TP1	E-4	VC1
Q11	C-4	Q35	A-4	QR16	B-1	QR41	A-3	IC19	E-4	IC509	G-2	IC704	H-2	TP2	E-5	Switches		
Q12	B-4	Q36	A-4	QR17	D-3	QR42	C-3	IC20	E-4	IC510	G-3	IC705	G-2	TP3	E-4	SW500	D-1	
Q13	C-4	Q37	A-4	QR18	B-3	QR701	G-4	IC23	E-4	IC511	F-3	IC706	G-2	TP4	E-4			SW501
Q14	B-4	Q38	C-3	QR19	C-3	QR702	H-3	IC24	D-2	IC512	F-4	IC707	H-3	TP5	B-2	Connectors		
Q15	B-4	Q39	D-5	QR20	B-4	QR703	H-3	IC25	A-3	IC513	G-3	IC708	H-2	TP6	B-2	P1	G-5	
Q16	B-4	Q701	H-4	QR21	B-3	QR704	H-3	IC26	B-1	IC514	G-3	IC709	J-2	TP7	B-2			P2
Q17	B-4	Q702	H-3	QR22	B-3	QR705	H-3	IC27	B-5	IC515	G-4	IC710	I-2	TP8	A-1	P701	I-1	
Q18	B-4	Q703	H-3	QR23	C-3	Integrated Circuits	IC1	IC28	A-3	IC516	G-4	IC711	I-2	TP9	D-3			
Q19	B-4	Q704	H-3	QR24	D-3			IC3	C-1	IC29	C-1	IC517	F-1	IC712	I-3	TP10	B-1	
Q20	B-4	Q705	H-4	QR25	A-3	IC4	B-3	IC30	D-3	IC518	H-2	IC713	H-2	TP11	B-2			
Q21	B-4	Transistor-Resistors	QR3	A-4	C-4	IC5	A-2	IC31	D-3	IC519	I-1	IC714	G-4	TP12	B-2			
Q22	D-4				QR26	C-4	IC6	B-2	IC32	H-1	IC520	C-3	IC521	F-1	IC715	F-4	TP500	F-2
Q23	D-4				QR27	C-4	IC7	B-3	IC33	G-1	IC522	C-2	IC523	G-1	IC716	G-4	TP501	F-2
Q24	C-4				QR28	A-2	IC8	E-4	IC34	D-1	IC35	A-2	IC524	F-1	IC717	I-3	TP502	G-2
Q25	C-4	QR29	A-4	IC9	D-1	IC35		IC36	C-1		E-1	IC718	J-4	TP503	G-2			

ADDRESS INFORMATION
⊙ ... COMPONENT SIDE
⊙ ... FOIL SIDE



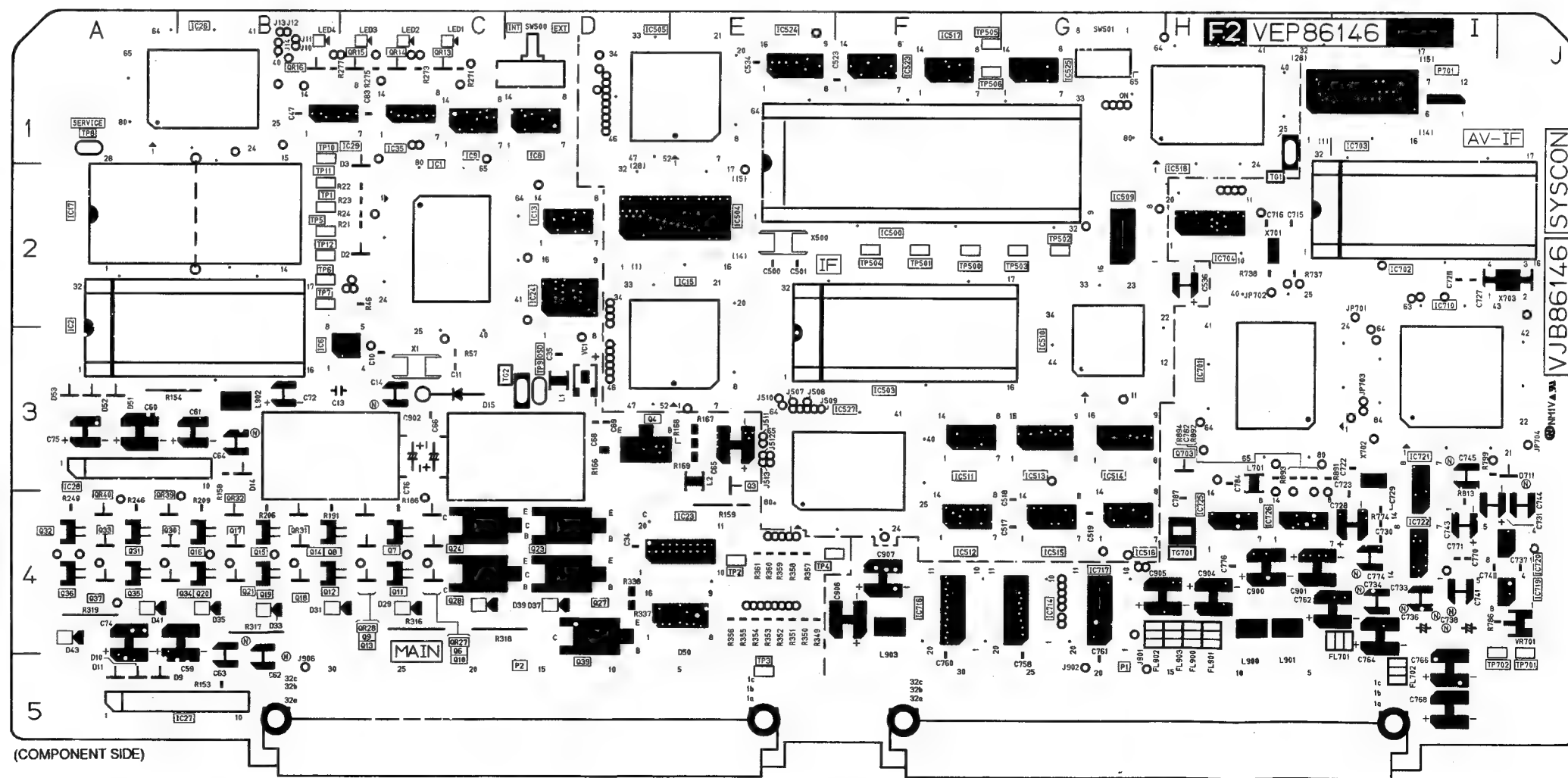
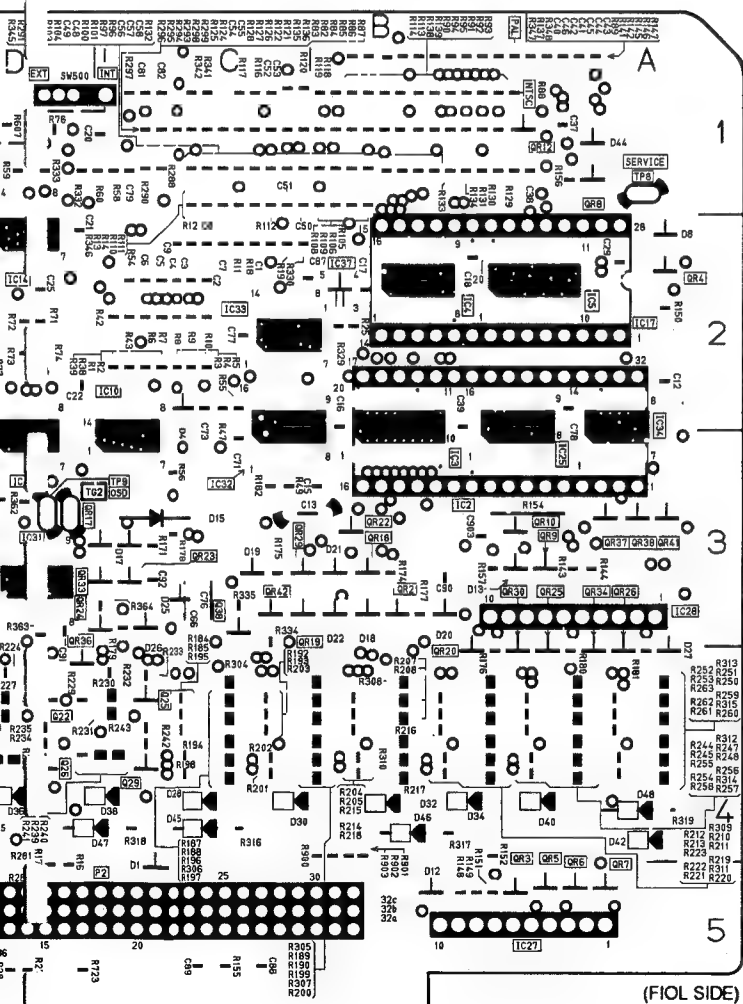
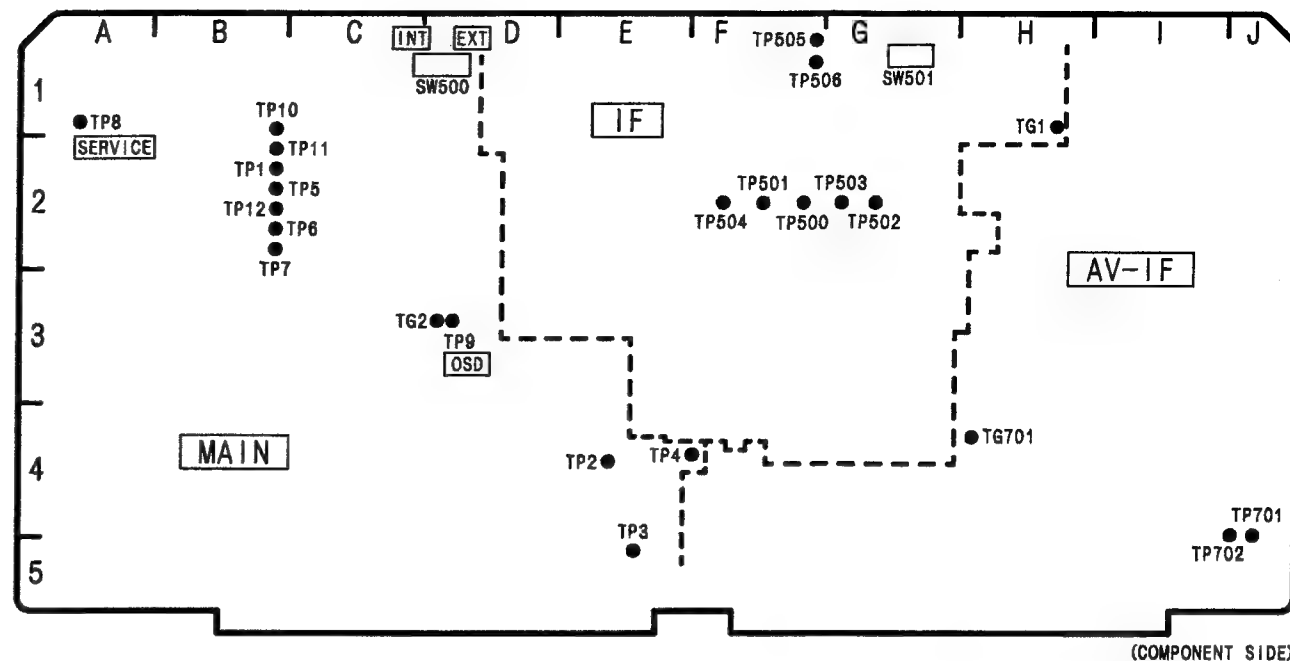
(FOIL SIDE)



(COMPONENT SIDE)

F2 SYSCON											
B-4	IC9	C-1	IC37	B-2	IC525	G-1	IC720	J-4	TP504	F-2	
D-3	IC10	C-2	IC500	F-2	IC527	F-3	IC721	I-3	TP505	F-1	
A-3	IC11	D-3	IC501	F-2	IC528	E-3	IC722	I-3	TP506	F-1	
D-4	IC12	D-2	IC502	G-2	IC529	E-3	IC723	I-5	TP701	J-5	
D-3	IC13	D-2	IC504	E-2	IC530	E-3	IC724	I-5	TP702	J-5	
A-3	IC14	D-2	IC505	D-1	IC531	E-2	IC725	H-4	TG1	H-1	
A-3	IC15	E-2	IC506	E-1	IC532	F-3	IC726	H-4	TG2	D-3	
A-4	IC16	D-2	IC507	E-1	IC701	H-3			TG701	H-4	
A-4	IC17	A-2	IC508	D-1	IC703	I-1					
A-3	IC19	E-4	IC509	G-2	IC704	H-2					
C-3	IC20	E-4	IC510	G-3	IC705	G-2					
G-4	IC23	E-4	IC511	F-3	IC706	G-2					
H-3	IC24	D-2	IC512	F-4	IC707	H-3					
H-3	IC25	A-3	IC513	G-3	IC708	H-2					
H-3	IC26	B-1	IC514	G-3	IC709	J-2					
H-3	IC27	B-5	IC515	G-4	IC710	I-2					
	IC28	A-3	IC516	G-4	IC711	I-2					
	IC29	C-1	IC517	F-1	IC712	I-3					
	IC30	D-3	IC518	H-2	IC713	H-2					
	IC31	D-3	IC519	I-1	IC714	G-4					
	IC32	C-3	IC520	H-1	IC715	G-4					
	IC33	C-2	IC521	G-1	IC716	F-4					
	IC34	A-2	IC522	G-1	IC717	G-4					
	IC35	C-1	IC523	F-1	IC718	I-3					
	IC36	D-4	IC524	E-1	IC719	J-4					

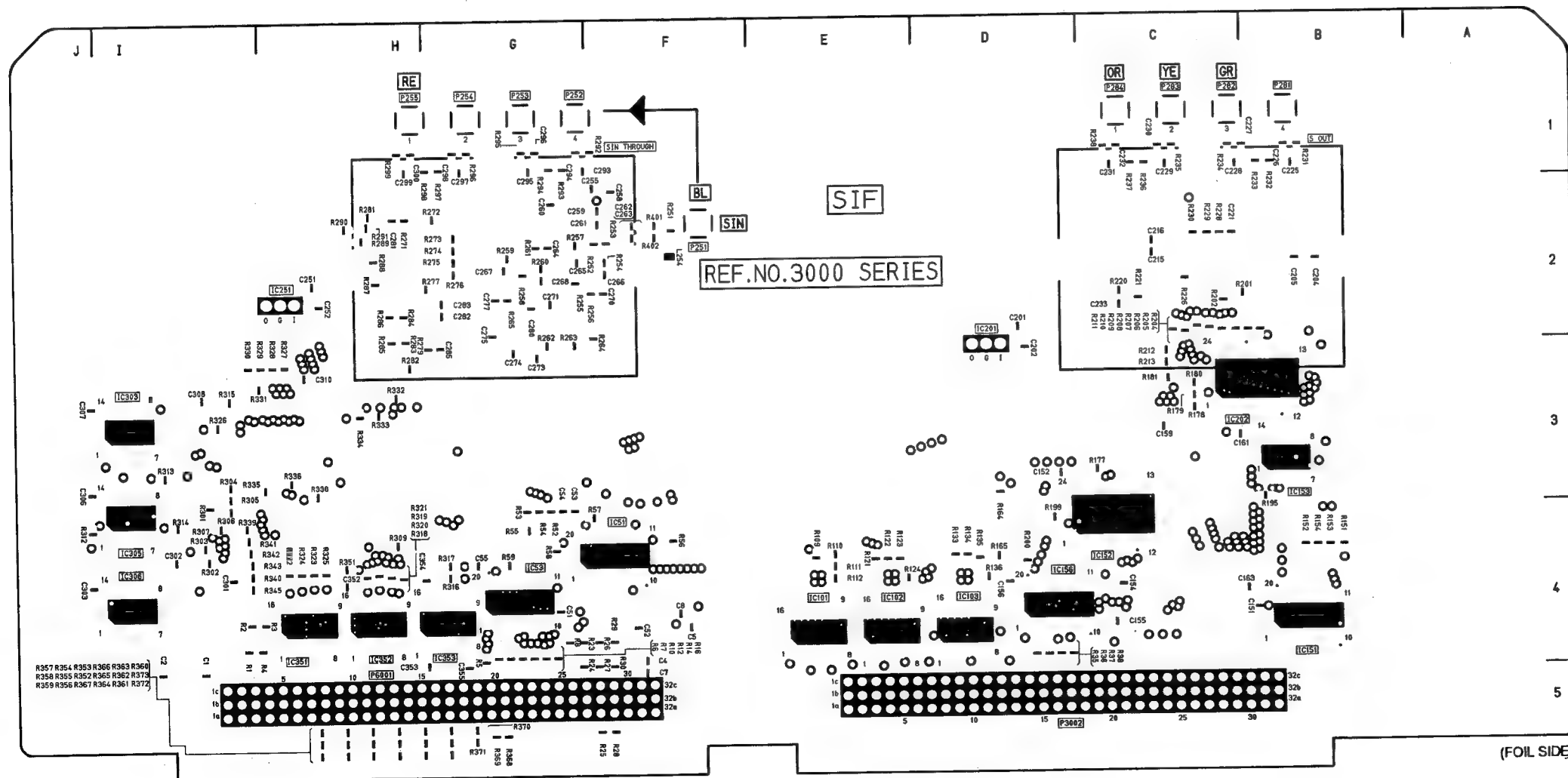
F2 SYSCON P. C. BOARD



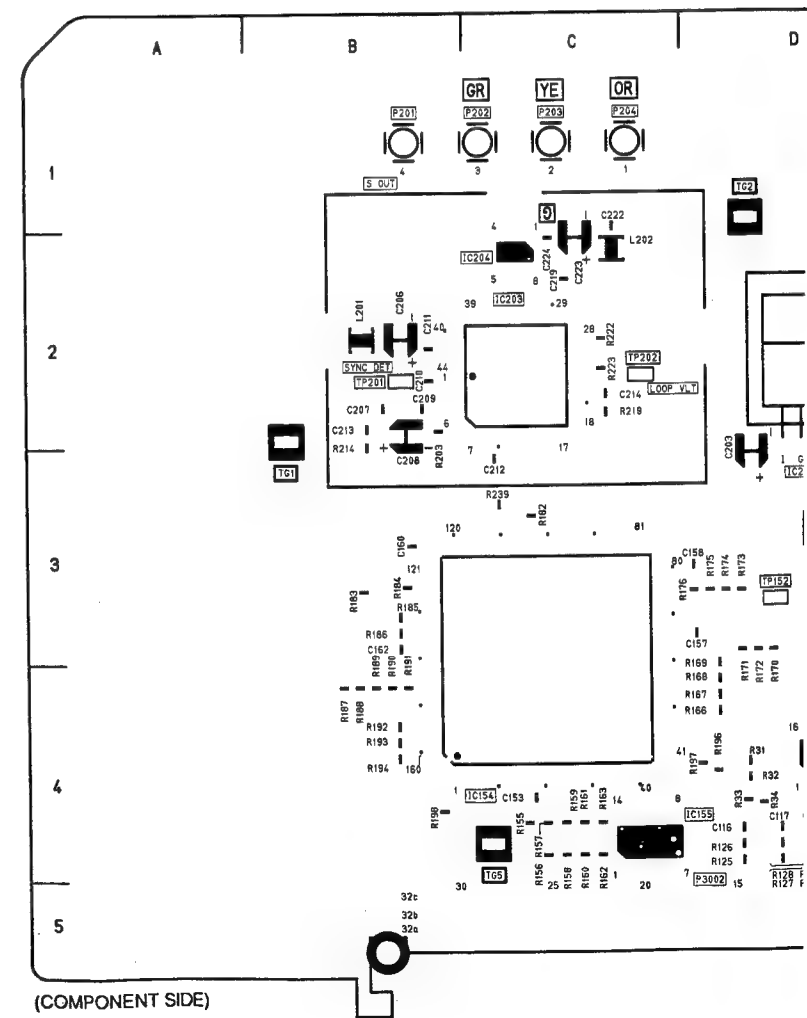
[AJ-YA750] F3 SIF P.C. BOARD (VEP83220A)

F3 SIF									
Transistors		IC151	B-4	⊙	IC352	H-4	⊙	TP311	J-3
Q251		IC152	C-4	⊙	IC353	G-4	⊙	TP312	J-3
Transistor-Resistors		IC153	B-3	⊙	IC354	G-4	⊙	TG1	B-3
QR51		IC154	C-4	⊙	IC355	H-4	⊙	TG2	D-1
Integrated Circuits		IC155	D-4	⊙	IC356	H-4	⊙	TG3	F-2
IC51		IC201	D-4	⊙	Test Points		TG4	H-1	⊙
IC52		IC202	D-3	⊙	TP151		TG5	C-4	⊙
IC53		IC203	C-2	⊙	TP152		TG6	D-3	⊙
IC54		IC204	C-2	⊙	TP201		TG7	F-4	⊙
IC55		IC251	H-2	⊙	TP202		TG8	J-3	⊙
IC56		IC252	F-2	⊙	TP251		Connectors		
IC57		IC253	G-3	⊙	TP301		P202	C-1	
IC58		IC254	H-2	⊙	TP302		P203	C-1	
IC101		IC255	G-2	⊙	TP303		P204	C-1	
IC102		IC301	I-3	⊙	TP304		P251	F-2	
IC103		IC302	H-3	⊙	TP305		P255	H-1	
IC104		IC303	I-3	⊙	TP306		P3001	G-5	
IC105		IC304	G-3	⊙	TP307		P3002	D-5	
IC106		IC305	I-4	⊙	TP308				
		IC306	I-4	⊙	TP309				
		IC351	H-4	⊙	TP310				

ADDRESS INFORMATION
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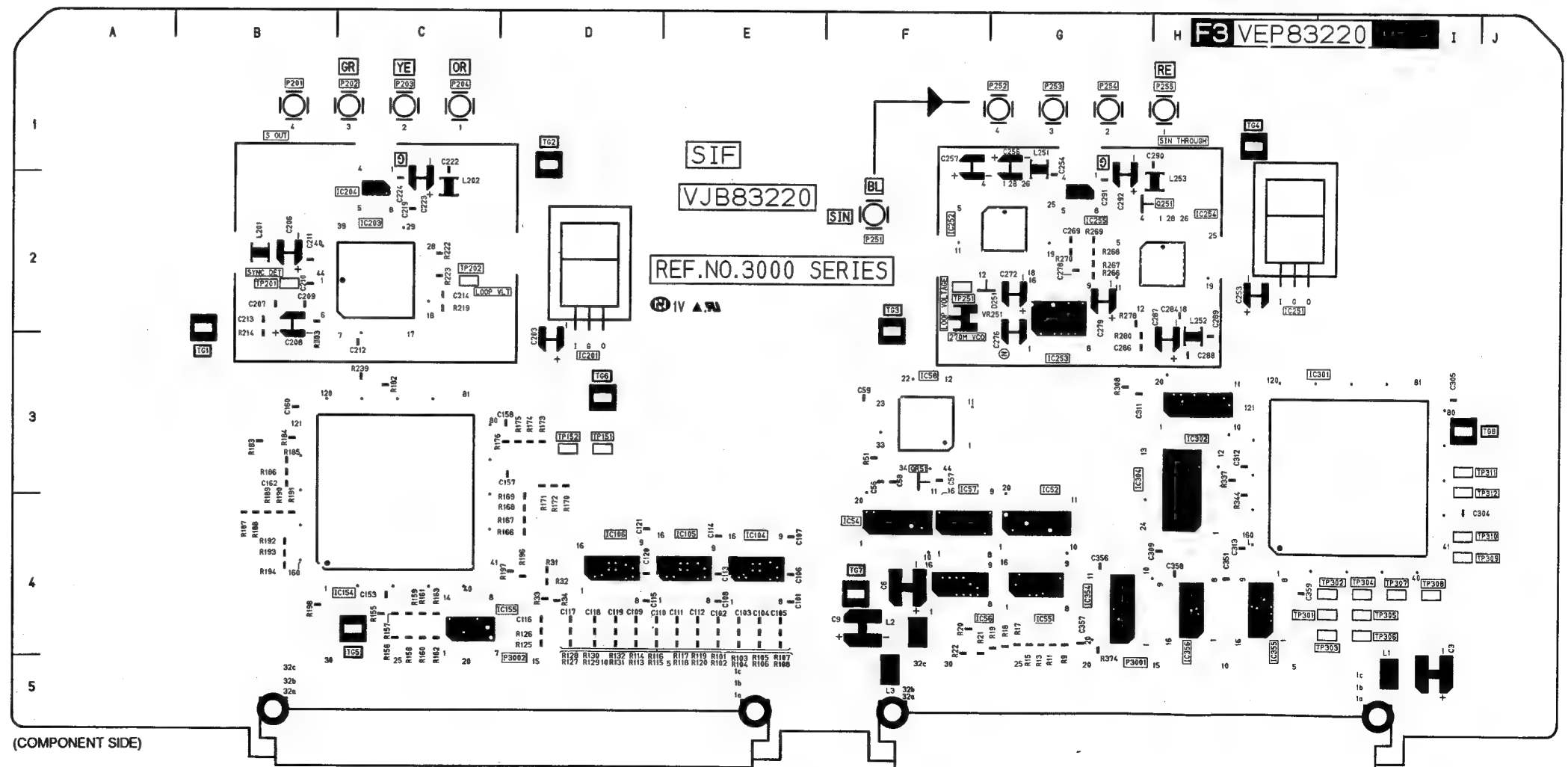
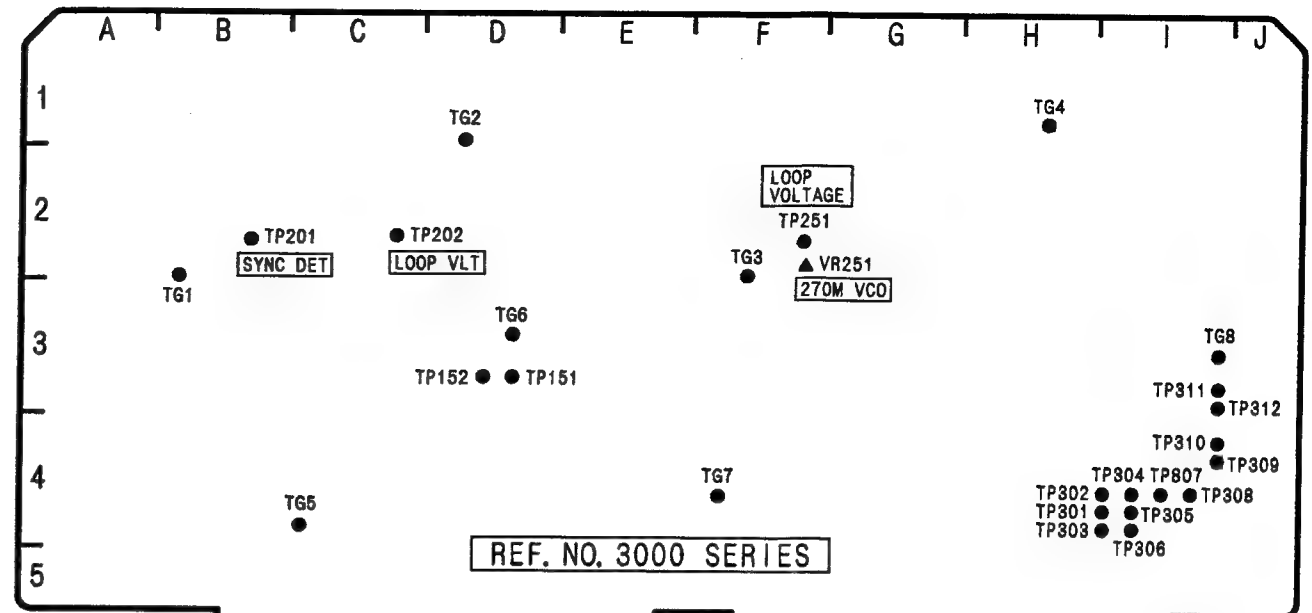


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ADDRESS INFORMATION
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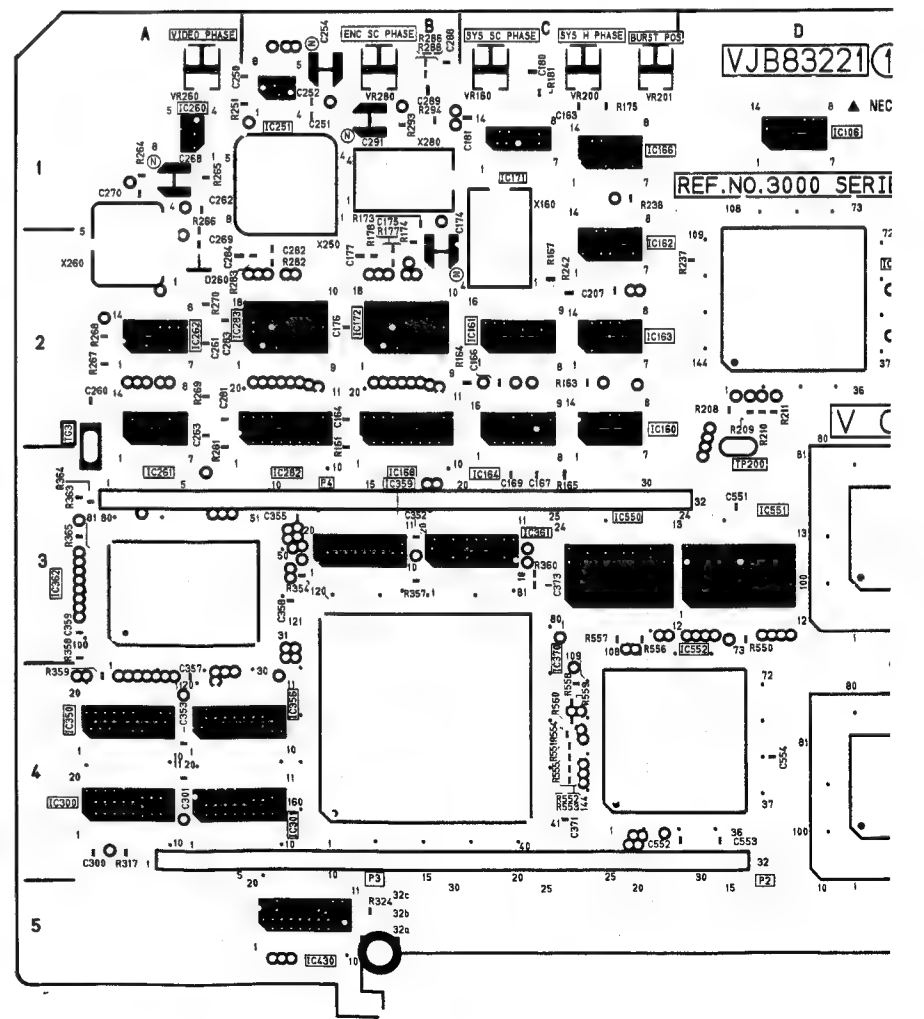
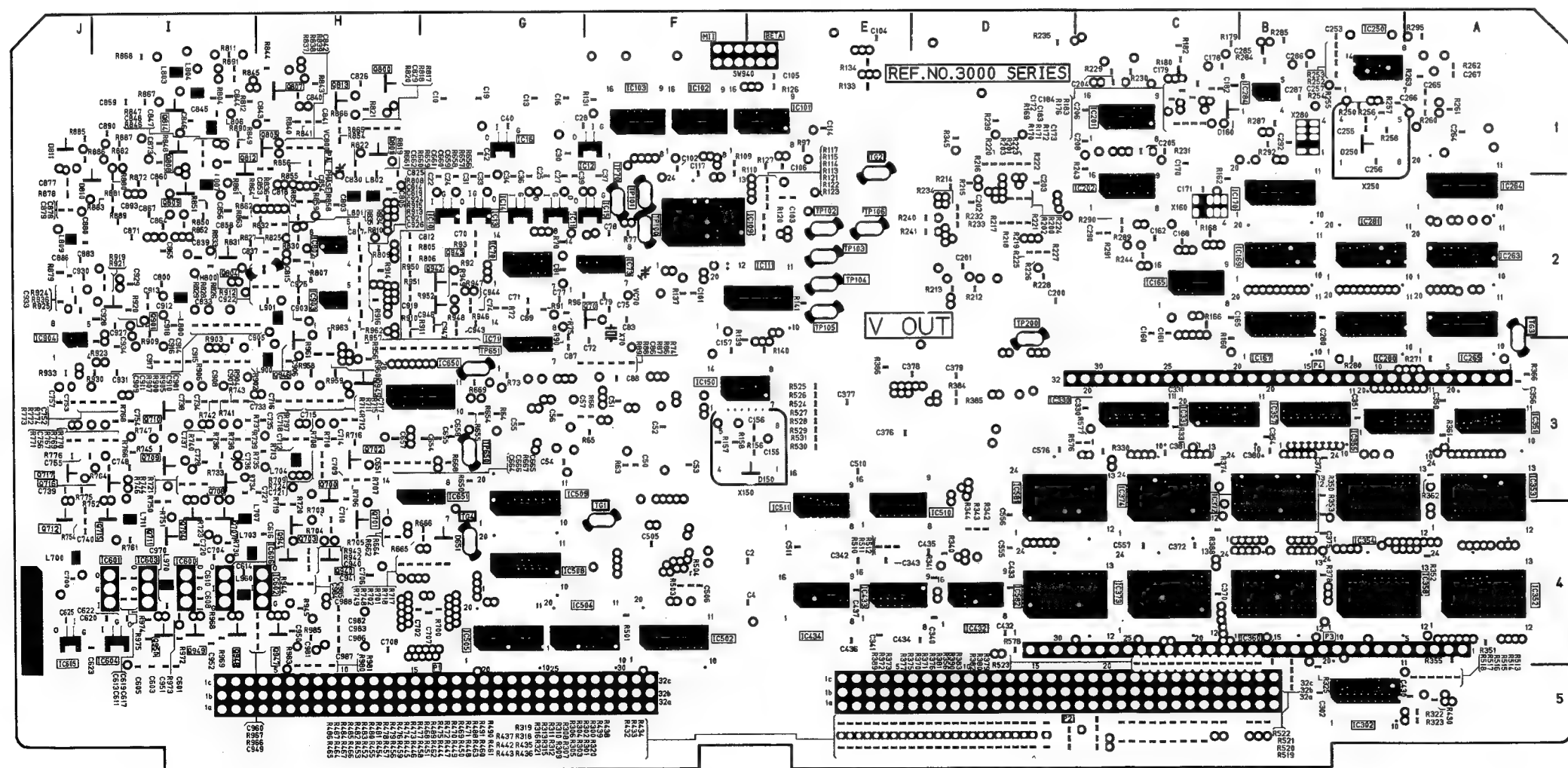
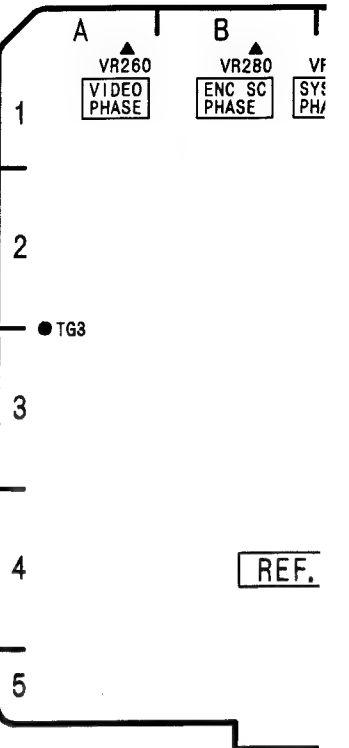


F4 V OUT P.C. BOARD (VEP83221B)

F4 V. OUT P. C. BOARD

F4 V OUT														
Transistors			Integrated Circuits			IC8151			IC8265			IC8370		
Q8070	F-2	Q8806	IC8010	G-2	IC8111	E-3	IC8280	A-3	IC8371	E-3	IC8582	D-4	Test Points	VR8200
Q8071	F-3	Q8807	IC8011	G-2	IC8112	E-2	IC8281	B-3	IC8372	E-3	IC8600	I-4	TP70	VR8201
Q8072	G-3	Q8808	IC8012	F-1	IC8113	C-2	IC8282	B-3	IC8373	C-3	IC8601	I-4	TP100	VR8260
Q8700	H-3	Q8809	IC8013	G-2	IC8114	C-2	IC8283	B-2	IC8374	C-4	IC8602	H-4	TP101	VR8280
Q8701	H-4	Q8810	IC8014	G-2	IC8115	C-2	IC8284	B-1	IC8430	B-5	IC8603	I-4	TP102	VR8700
Q8702	H-3	Q8811	IC8015	F-2	IC8116	C-3	IC8300	A-4	IC8432	D-4	IC8604	J-4	TP103	VR8701
Q8703	H-4	Q8812	IC8016	G-1	IC8117	C-2	IC8301	B-4	IC8433	E-4	IC8605	H-4	TP104	VR8702
Q8704	I-4	Q8813	IC8017	F-3	IC8118	C-1	IC8302	B-5	IC8434	F-4	IC8606	G-3	TP105	VR8703
Q8707	I-4	Q8814	IC8018	G-3	IC8119	B-3	IC8303	D-3	IC8500	F-4	IC8650	G-3	TP106	VR8704
Q8708	I-3	Q8815	IC8019	G-2	IC8120	B-2	IC8304	C-3	IC8501	G-4	IC8700	H-4	TP200	VR8705
Q8709	I-3	Q8816	IC8020	G-2	IC8121	B-2	IC8305	E-4	IC8502	F-4	IC8701	H-4	TP650	VR8706
Q8710	I-3	Q8817	IC8021	G-2	IC8122	C-1	IC8306	A-4	IC8503	F-4	IC8702	H-3	TP651	VR8801
Q8711	I-4	Q8818	IC8022	F-2	IC8123	B-2	IC8307	A-3	IC8504	G-4	IC8703	I-3	TG8001	VR8802
Q8712	J-4	Q8819	IC8023	G-2	IC8124	D-2	IC8308	A-3	IC8505	G-4	IC8704	J-3	TG8002	VR8803
Q8715	I-4	Q8820	IC8024	E-2	IC8125	C-1	IC8309	B-4	IC8506	F-4	IC8801	H-2	TG8003	VR8804
Q8716	J-3	Q8821	IC8025	E-1	IC8126	C-2	IC8310	B-3	IC8507	G-3	IC8802	H-2	TG8004	VR8805
Q8717	J-3	Q8822	IC8026	F-1	IC8127	B-1	IC8311	B-4	IC8508	D-4	IC8803	I-2		VR8806
Q8800	H-1	Q8823	IC8027	F-1	IC8128	B-1	IC8312	B-3	IC8509	E-4	IC8804	I-2		VR8807
Q8801	H-1	Q8824	IC8028	E-1	IC8129	A-1	IC8313	B-3	IC8510	C-3	IC8805	I-2		VR8900
Q8802	H-2	Q8825	IC8029	D-1	IC8130	A-3	IC8314	B-3	IC8511	D-3	IC8806	H-2		VR8901
Q8803	H-2	Q8826	IC8030	E-2	IC8131	A-2	IC8315	B-4	IC8512	D-3	IC8807	J-2		VR8902
Q8804	I-2	Q8827	IC8031	F-2	IC8132	A-2	IC8316	C-3	IC8513	D-3	IC8808	G-2		VR8903
Q8805	H-1	Q8828	IC8032	F-3	IC8133	A-2	IC8317	A-3	IC8514	D-3	IC8809			VR8904

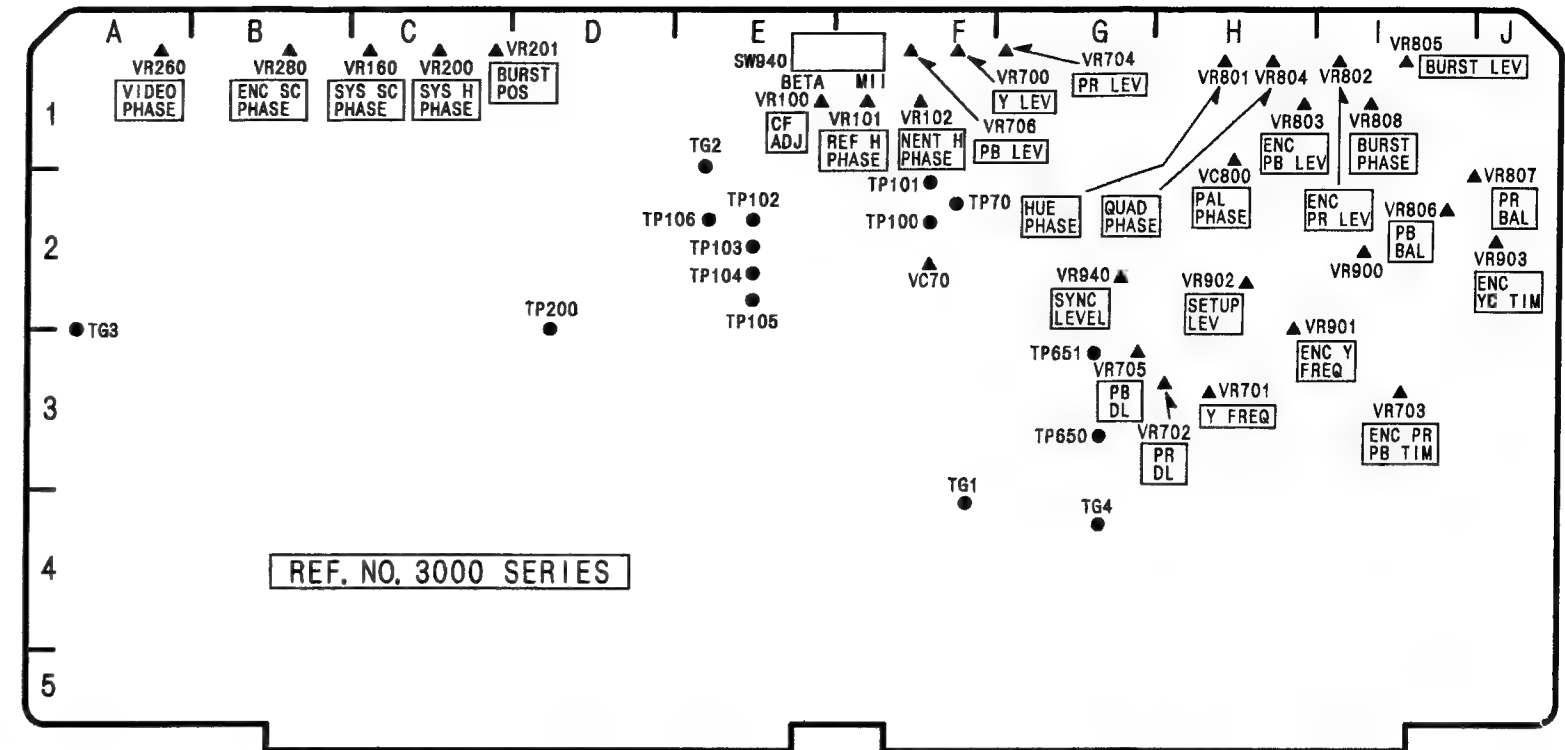
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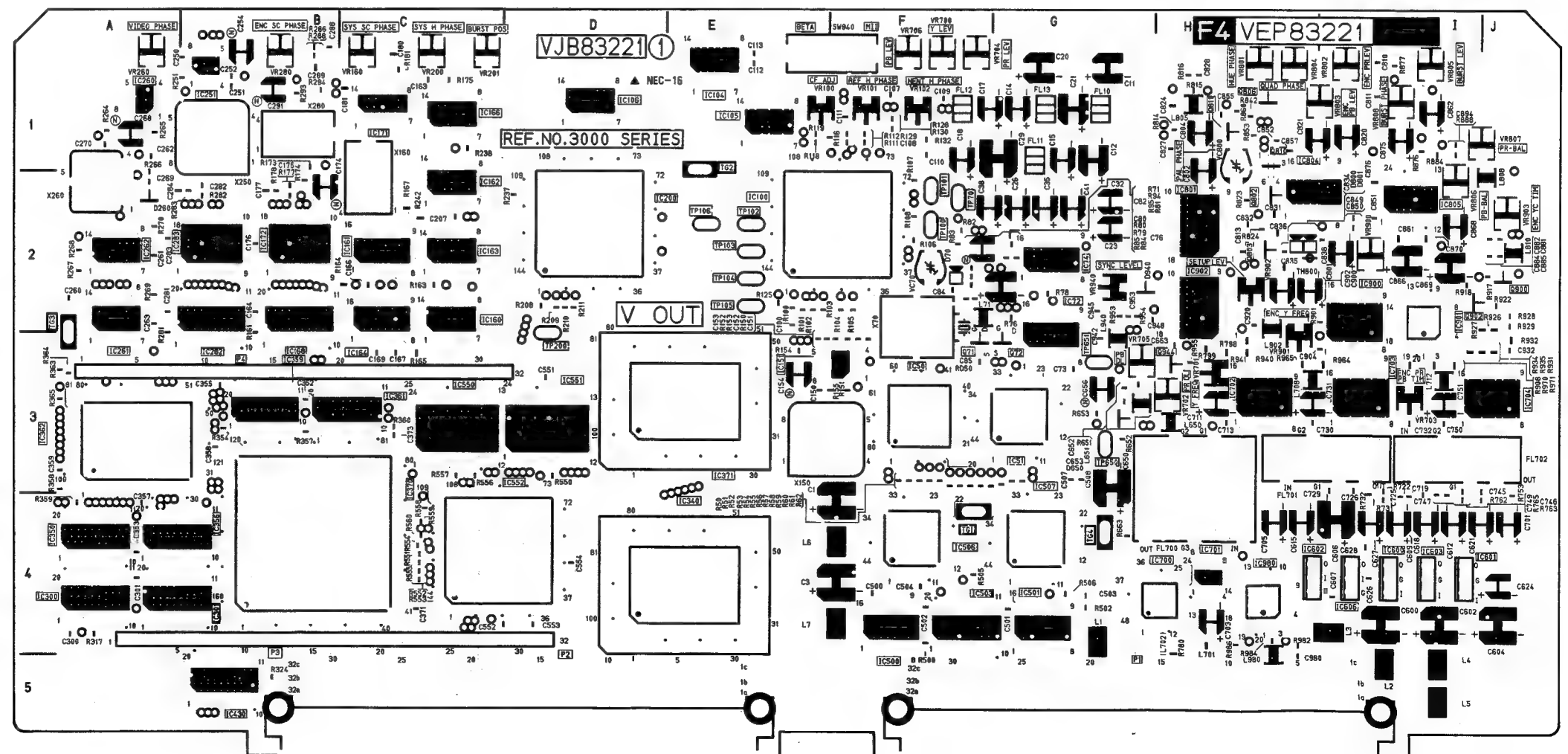
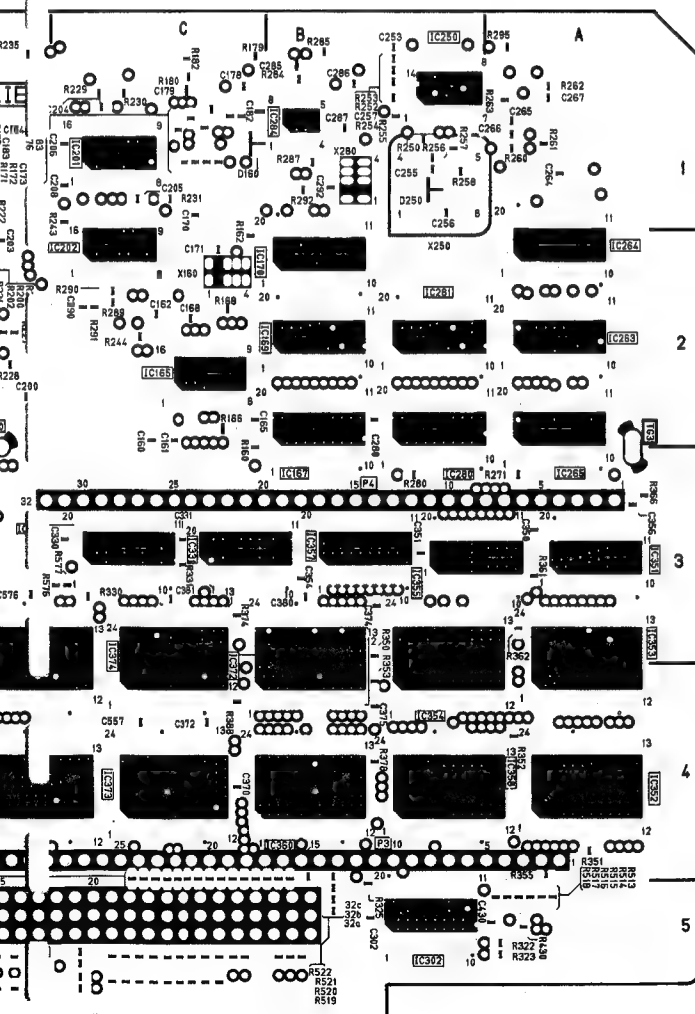
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F4 V. OUT P. C. BOARD

Test Points				Switch			
C-3	⊙	IC8582	D-4	⊙	VR8200	C-1	⊙
E-3	⊙	IC8600	I-4	⊙	VR8201	C-1	⊙
C-3	⊙	IC8601	I-4	⊙	VR8260	A-1	⊙
C-4	⊙	IC8602	H-4	⊙	VR8280	B-1	⊙
C-3	⊙	IC8603	I-4	⊙	VR8700	F-1	⊙
B-5	⊙	IC8604	I-4	⊙	VR8701	H-3	⊙
D-4	⊙	IC8605	J-4	⊙	VR8702	H-3	⊙
E-4	⊙	IC8606	H-4	⊙	VR8703	I-3	⊙
E-4	⊙	IC8650	G-3	⊙	VR8704	G-1	⊙
F-4	⊙	IC8651	G-3	⊙	VR8705	G-3	⊙
G-4	⊙	IC8700	H-4	⊙	VR8706	F-1	⊙
F-4	⊙	IC8701	H-4	⊙	VR8801	H-1	⊙
F-4	⊙	IC8702	H-3	⊙	VR8802	I-1	⊙
G-4	⊙	IC8703	I-3	⊙	VR8803	I-1	⊙
G-4	⊙	IC8704	J-3	⊙	VR8804	H-1	⊙
F-4	⊙	IC8801	H-2	⊙	VR8805	I-1	⊙
G-3	⊙	IC8802	H-2	⊙	VR8806	I-2	⊙
G-4	⊙	IC8804	H-1	⊙	VR8807	J-1	⊙
G-3	⊙	IC8805	I-2	⊙	VR8808	I-1	⊙
D-4	⊙	IC8900	I-2	⊙	VR8900	I-2	⊙
E-4	⊙	IC8901	I-2	⊙	VR8901	H-3	⊙
C-3	⊙	IC8902	H-2	⊙	VR8902	H-2	⊙
D-3	⊙	IC8903	H-2	⊙	VR8903	J-2	⊙
D-3	⊙	IC8904	J-3	⊙	VR8940	G-2	⊙
D-3	⊙	IC8980	H-4	⊙			



(COMPONENT SIDE)



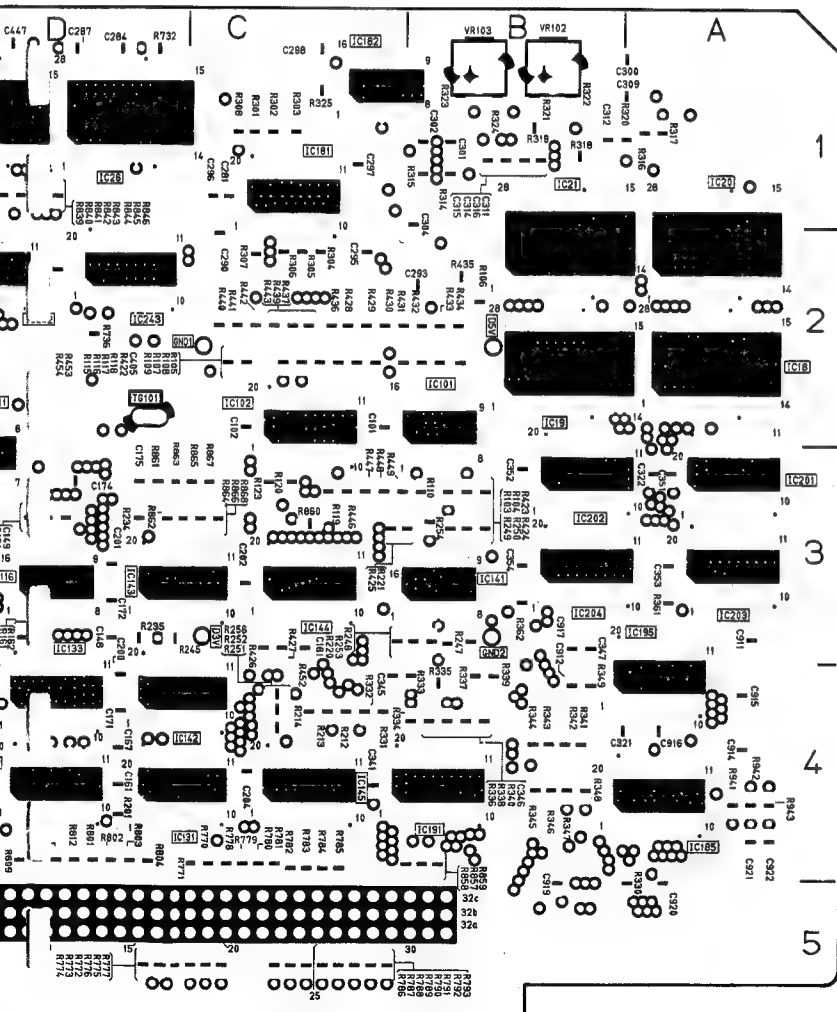
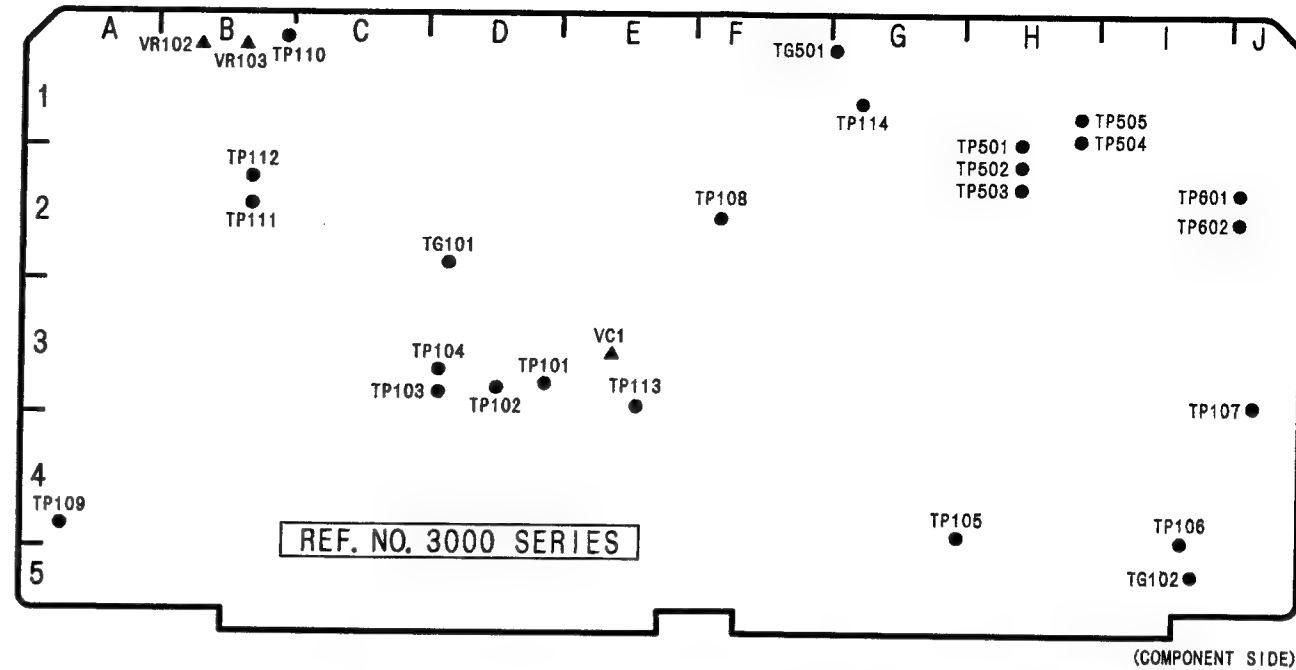
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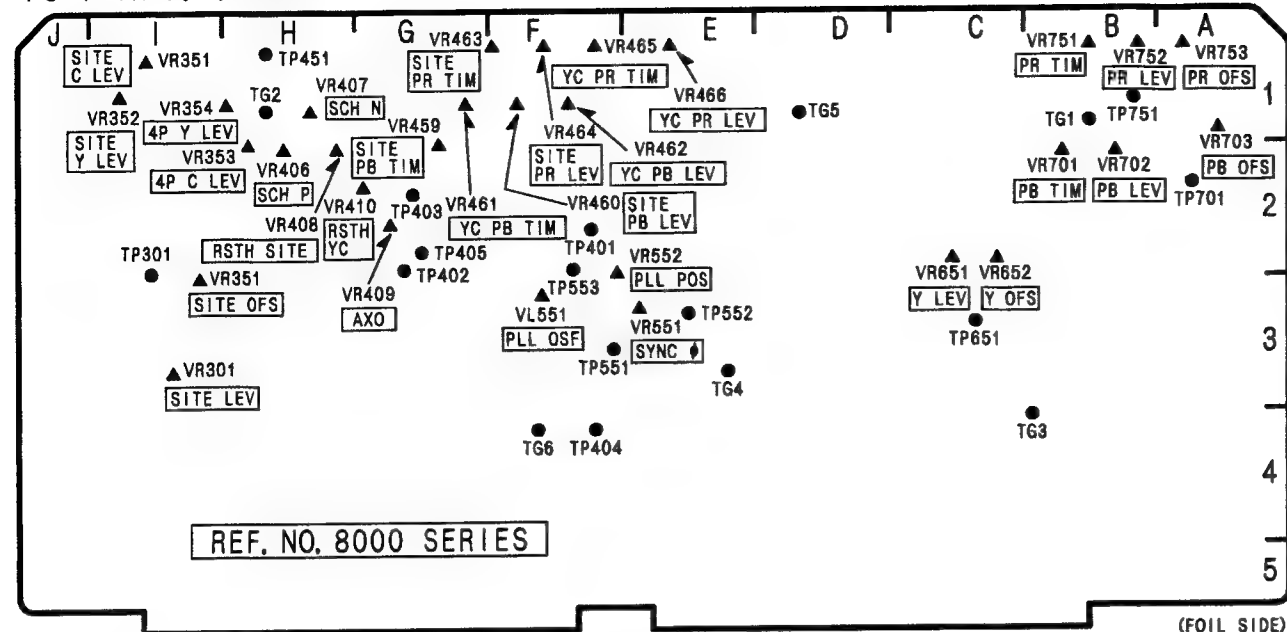
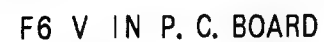
F5 REC PB											
Transistors		IC19	B-2	IC116	D-3	IC202	B-3	IC254	F-4	TP109	A-4
Q1	E-3	IC20	A-1	IC117	F-3	IC203	A-3	IC255	E-4	TP110	C-1
Q501	H-1	IC21	B-1	IC118	F-2	IC204	B-3	IC256	E-4	TP111	B-2
Transistor-Resistor		IC22	H-3	IC119	G-3	IC213	H-4	IC257	E-4	TP112	B-2
QR501	H-1	IC23	I-3	IC120	G-2	IC214	I-3	IC258	E-4	TP113	F-3
Integrated Circuits		IC24	C-2	IC121	E-3	IC215	H-2	IC501	I-1	TP114	G-1
IC1	E-2	IC25	G-3	IC131	D-4	IC221	G-4	IC502	J-2	TP105	G-4
IC2	E-1	IC26	D-1	IC132	D-4	IC222	G-4	IC503	H-2	TP501	H-1
IC3	D-4	IC27	E-1	IC133	D-3	IC223	G-4	IC504	J-2	TP502	H-1
IC4	D-3	IC28	E-1	IC141	B-3	IC224	G-3	IC505	J-2	TP503	H-2
IC5	D-2	IC30	G-4	IC142	C-4	IC225	F-4	IC507	H-1	TP504	H-1
IC6	C-4	IC31	B-4	IC143	D-3	IC226	H-3	IC508	H-1	TP505	H-1
IC7	G-1	IC32	J-3	IC144	C-3	IC227	G-2	IC601	I-2	TP601	J-2
IC8	G-1	IC33	I-4	IC145	C-4	IC228	G-2	IC603	I-2	TP602	J-2
IC9	H-4	IC34	H-3	IC146	G-2	IC231	G-2	IC901	J-4	TG101	D-2
IC10	I-4	IC35	A-4	IC151	G-2	IC232	H-3	IC903	I-4	TG102	I-5
IC11	F-2	IC36	B-5	IC161	H-4	IC233	I-3	IC905	I-4	TG501	G-1
IC12	F-1	IC37	A-5	IC162	H-4	IC234	F-2	Test Points		Adjustments	
IC13	D-1	IC101	B-2	IC171	F-1	IC235	F-2				
IC14	C-2	IC102	C-2	IC175	F-2	IC236	I-2	TP101	D-3	VC1	E-3
IC15	B-1	IC103	E-3	IC177	H-2	IC237	H-2	TP102	D-3	VR102	B-1
IC16	A-3	IC104	F-4	IC181	C-1	IC241	E-2	TP103	D-3	VR103	B-1
IC17	B-2	IC111	D-2	IC182	C-1	IC242	D-2	TP104	D-3	Connectors	
IC18	A-2	IC112	E-4	IC185	A-4	IC243	D-2	TP105	G-4		
		IC113	F-3	IC191	B-4	IC251	F-4	TP106	I-4	P1	G-5
		IC114	E-2	IC195	A-3	IC252	F-4	TP107	J-3	P2	D-5
		IC115	F-2	IC201	A-3	IC253	F-4	TP108	F-2	P3	C-1

ADDRESS INFORMATION
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F5 REC PB P. C. BOARD



F6 V IN P.C. BOARD (VEP83341A)

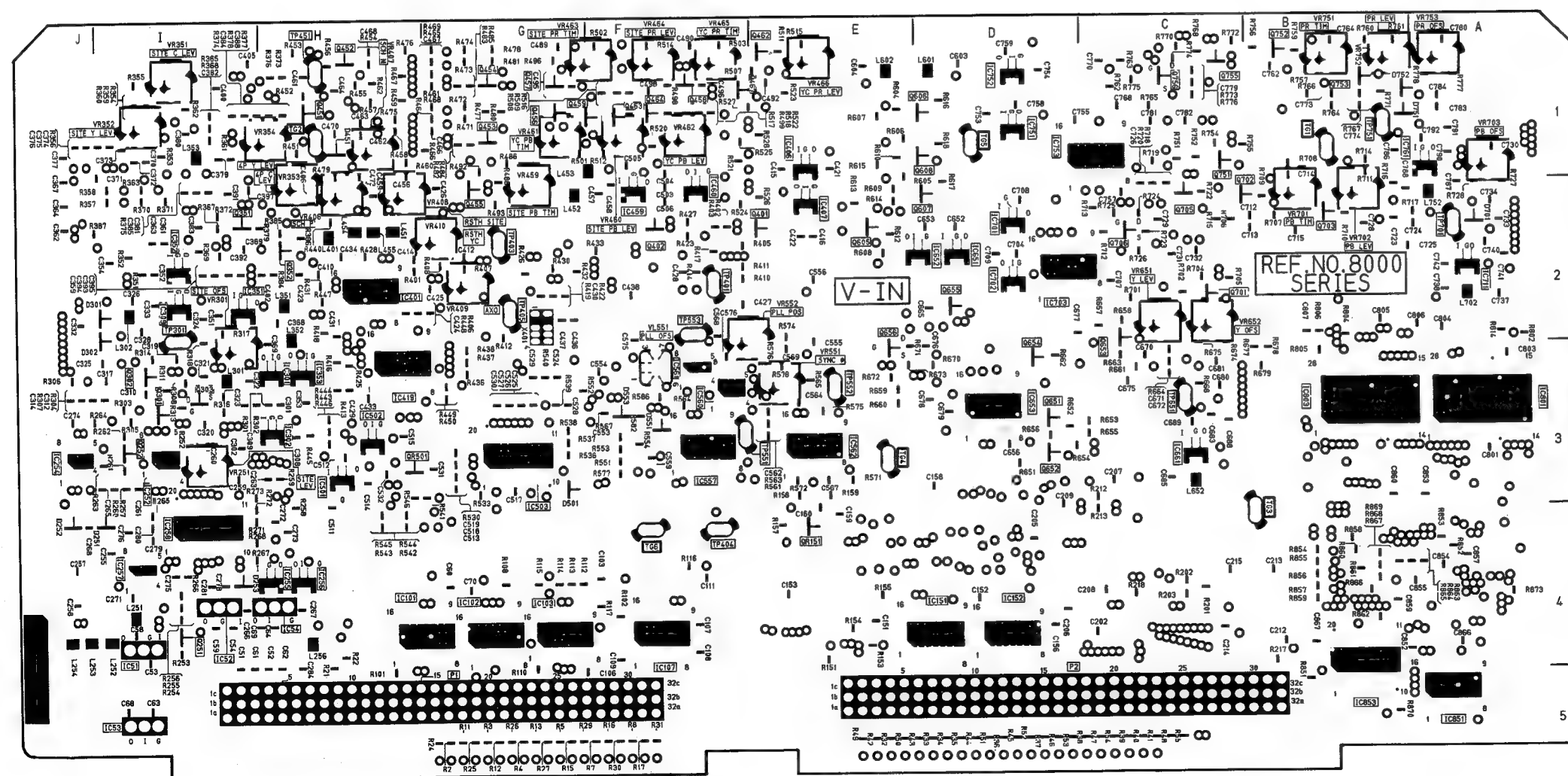


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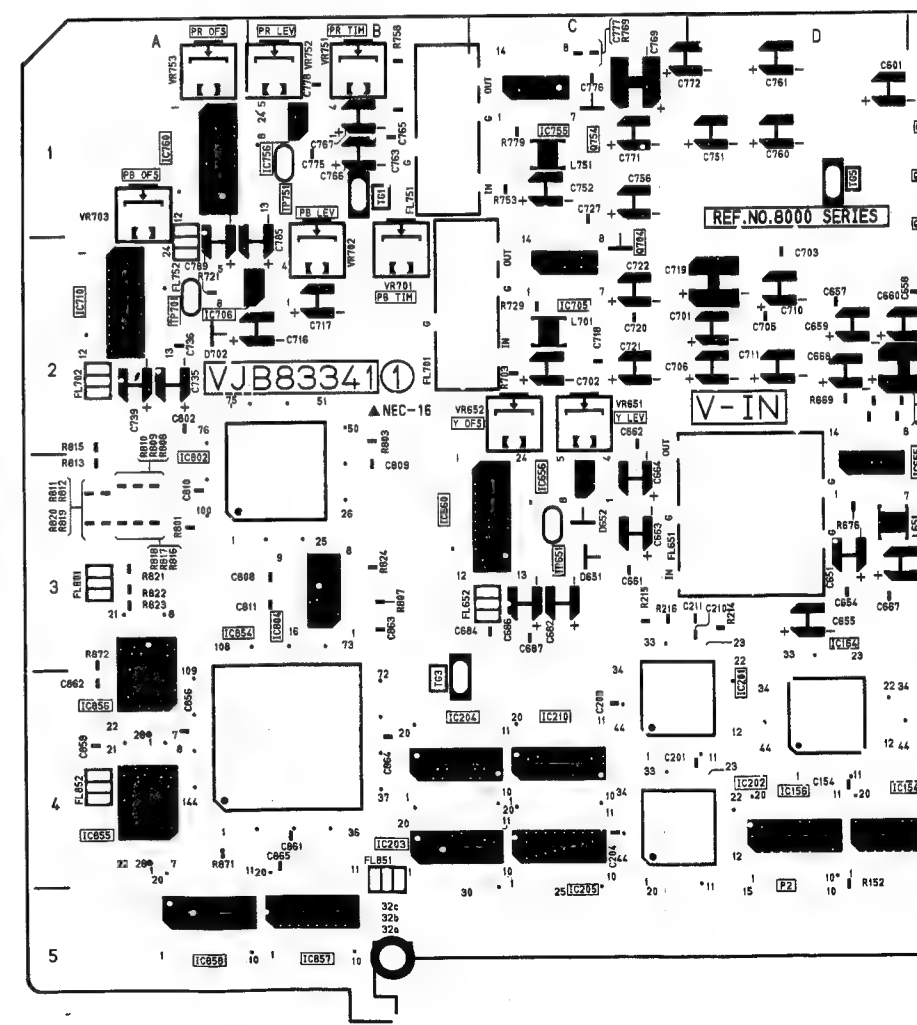
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F6 V IN												
Transistors			Q466	E-1	Q754	C-2	IC153	E-4	IC303	I-3	IC456	
Q251	I-4	Q551	F-3	Q755	C-1	IC154	D-4	IC304	J-3	IC456		
Q252	I-3	Q552	F-3	Q756	C-1	IC155	E-4	IC308	J-2	IC456		
Q301	I-3	Q553	F-3	Transistors-Resistors			D-4	IC351	I-2	IC461		
Q302	I-3	Q554	F-3	QR151 QR201 QR501 QR551			E-3	IC352	I-2	IC500		
Q303	I-3	Q601	E-1				E-4	IC164	D-3	IC353	H-3	IC500
Q351	I-2	Q602	E-1				D-4	IC165	E-3	IC354	J-2	IC500
Q352	H-3	Q603	E-1				H-3	IC201	D-4	IC355	I-1	IC500
Q401	E-2	Q604	E-2	F-3	IC202	D-4	IC356	I-2	IC500			
Q402	F-2	Q605	E-2	Integrated Circuits			IC203	IC357	I-1	IC55		
Q451	H-1	Q606	D-1	IC51 IC52 IC53 IC54			B-4	IC358	H-1	IC55		
Q452	H-1	Q607	D-2				I-4	IC204	C-4	IC359	I-1	IC55
Q453	G-1	Q608	D-1				I-4	IC205	C-3	IC401	H-2	IC55
Q454	G-1	Q651	D-3				I-5	IC210	H-3	IC402	H-2	IC56
Q455	G-2	Q652	D-3	IC101	H-4	IC252	I-3	IC403	G-3	IC56		
Q456	G-1	Q653	C-3	IC102	G-4	IC253	C-4	IC404	G-3	IC56		
Q457	G-1	Q654	D-3	IC103	G-4	IC254	J-3	IC407	E-2	IC56		
Q458	F-1	Q655	D-2	IC107	F-4	IC255	H-4	IC408	E-1	IC85		
Q459	G-1	Q656	E-2	IC109	F-4	IC256	H-4	IC418	F-2	IC85		
Q462	E-1	Q701	B-2	IC110	G-4	IC257	I-4	IC419	H-3	IC85		
Q463	F-1	Q704	C-2	IC111	F-4	IC258	I-4	IC423	G-2	IC85		
Q464	F-1	Q705	C-2	IC151	D-4	IC259	H-4	IC428	H-3	IC85		
Q465	F-1	Q706	B-3	IC152	D-4	IC301	H-3	IC452	H-1	IC86		
		Q751	B-2			IC302	H-3	IC453	G-1	IC86		

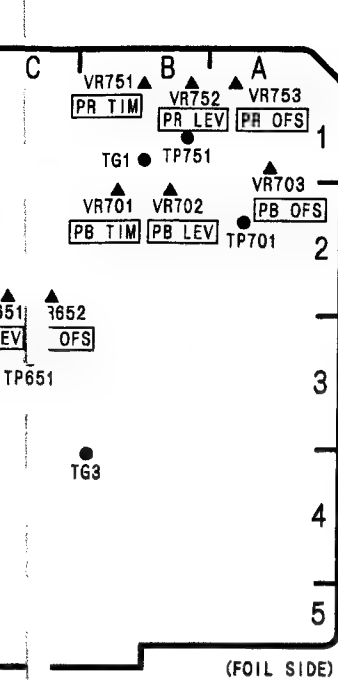
ADDRESS INFORMATION
 (C) ... COMPONENT SIDE
 (F) ... FOIL SIDE



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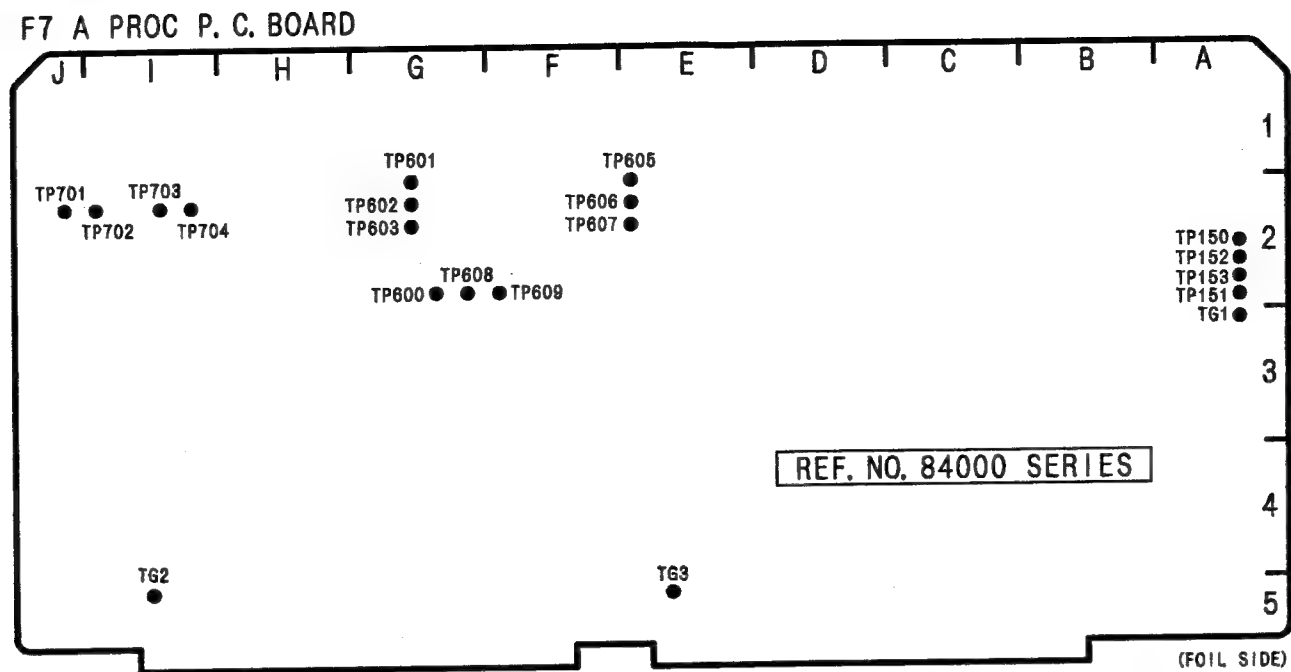


VJB833



F6 VIN																													
Transistors			Q466	E-1	Q754	C-2	IC153	E-4	IC303	I-3	IC455	E-1	IC701	D-2	IC858	A-5	TG1	C-2	VR463	F-1									
Q251	I-4	Q551	F-3	Q755	C-1	IC154	D-4	IC304	J-3	IC456	E-1	IC702	D-2	Test Points	I-2	TG2	H-1	VR464	F-1										
Q252	I-3	Q552	F-3	Q756	C-1	IC155	E-4	IC308	J-2	IC459	F-2	IC703	D-2			TG3	B-4	VR465	F-1										
Q301	I-3	Q553	F-3	Transistors-Resistors			E-4	IC351	I-2	IC460	F-2	IC705	B-2			TG4	G-3	VR466	E-1										
Q302	I-3	Q554	F-3	Q601	E-1	QR151	E-4	IC161	E-3	IC352	I-2	IC501	H-3	A-2	I-2	TG5	D-1	VR551	E-3										
Q303	I-3	Q602	E-1	Q603	E-1	QR201	D-4	IC164	D-3	IC353	H-3	IC502	H-3	A-2		TP301	F-2	VR552	E-2										
Q351	I-2	Q604	E-2	Q605	E-2	QR501	H-3	IC165	E-3	IC354	J-2	IC503	G-3	A-2		TP401	G-2	VR651	C-2										
Q352	H-3	Q606	D-1	Q607	D-2	QR551	F-3	IC201	D-4	IC355	I-1	IC504	G-3	D-1	TP402	G-2	Adjustments	VR652	C-2										
Q401	E-2	Q608	D-1	Q609	D-2	Integrated Circuits			IC202	D-4	IC356	I-2	IC507	D-1	TP403	G-2		VL551	F-2										
Q402	F-2	Q610	D-1	Q611	D-2	IC51	I-4	IC203	B-4	IC357	I-1	IC551	F-3	D-1	TP404	F-4		VR251	J-3										
Q451	H-1	Q612	D-1	Q613	D-2	IC52	I-4	IC204	B-4	IC358	H-1	IC552	G-3	A-1	TP405	G-2	VR301	I-2	VR701	B-2									
Q452	H-1	Q614	D-1	Q615	D-2	IC53	I-5	IC205	C-4	IC359	I-1	IC553	E-3	B-2	TP451	H-1	VR351	I-1	VR702	B-2									
Q453	G-1	Q616	D-1	Q617	D-2	IC54	I-5	IC210	C-3	IC401	H-2	IC554	F-3	A-1	TP501	E-2	VR352	I-1	VR703	A-1									
Q454	G-1	Q618	D-1	Q619	D-2	IC55	I-5	IC211	H-3	IC402	H-2	IC560	F-3	B-1	TP502	E-2	VR353	H-1	VR751	B-1									
Q455	G-2	Q620	D-1	Q621	D-2	IC56	I-5	IC212	I-3	IC403	G-3	IC561	F-3	A-3	TP503	G-1	VR354	H-1	VR752	B-1									
Q456	G-1	Q622	D-1	Q623	D-2	IC101	H-4	IC213	C-4	IC404	G-3	IC562	E-3	A-3	TP551	F-3	VR355	H-1	VR753	A-1									
Q457	G-1	Q624	D-1	Q625	D-2	IC102	G-4	IC214	J-3	IC407	E-2	IC567	F-3	C-2	TP552	E-3	Connectors												
Q458	F-1	Q626	D-1	Q627	D-2	IC103	G-4	IC215	H-4	IC408	E-1	IC651	D-2	B-3	TP553	F-2	P1	G-4											
Q459	G-1	Q628	D-1	Q629	E-2	IC107	F-4	IC216	H-4	IC418	F-2	IC652	D-2	A-5	TP601	D-3	P2	D-4											
Q462	E-1	Q701	B-2	Q704	C-2	IC109	F-4	IC217	I-4	IC419	H-3	IC653	D-3	B-5	TP602	D-3													
Q463	F-1	Q705	C-2	Q706	B-3	IC110	G-4	IC218	I-4	IC423	G-2	IC655	E-3	A-3	TP603	D-3													
Q464	F-1	Q706	B-3	Q751	B-2	IC111	F-4	IC219	H-4	IC428	H-3	IC656	C-3	A-4	TP651	C-3													
Q465	F-1					IC151	D-4	IC301	H-3	IC452	H-1	IC660	B-3	A-4	TP701	A-3													
						IC152	D-4	IC302	H-3	IC453	G-1	IC661	C-3	B-5	TP751	A-2													
															TP801	B-2													
																	VR461	G-1											
																	VR462	F-1											

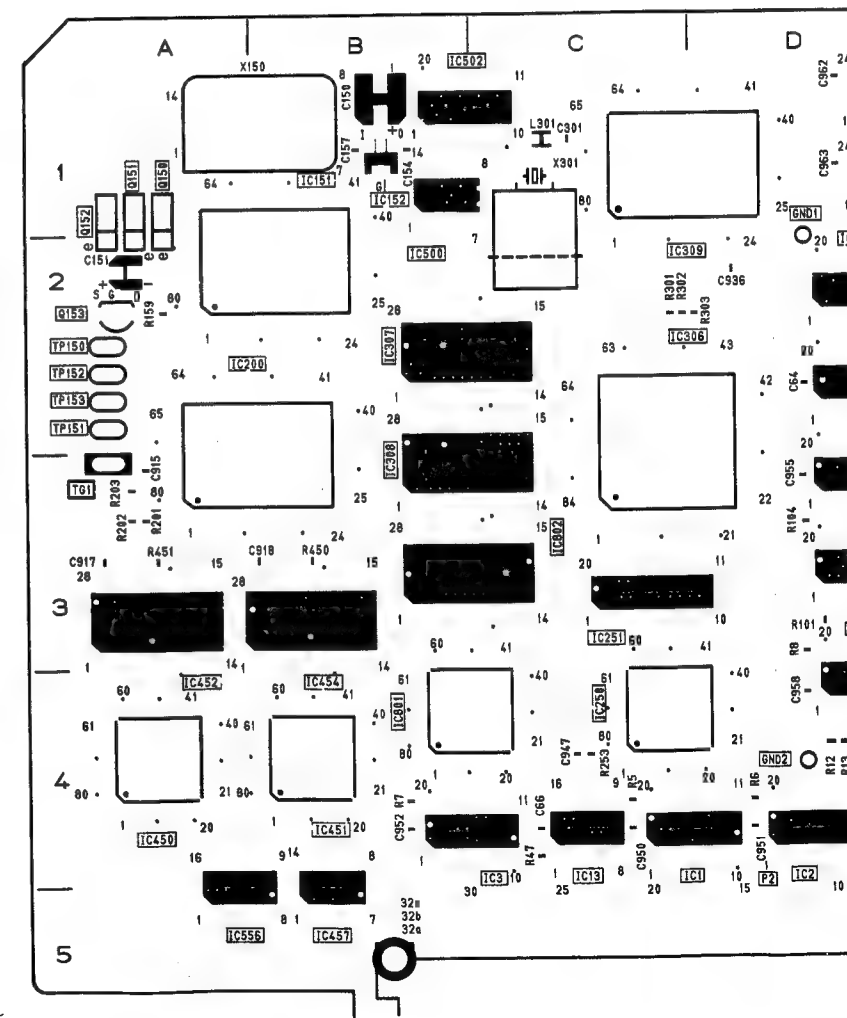
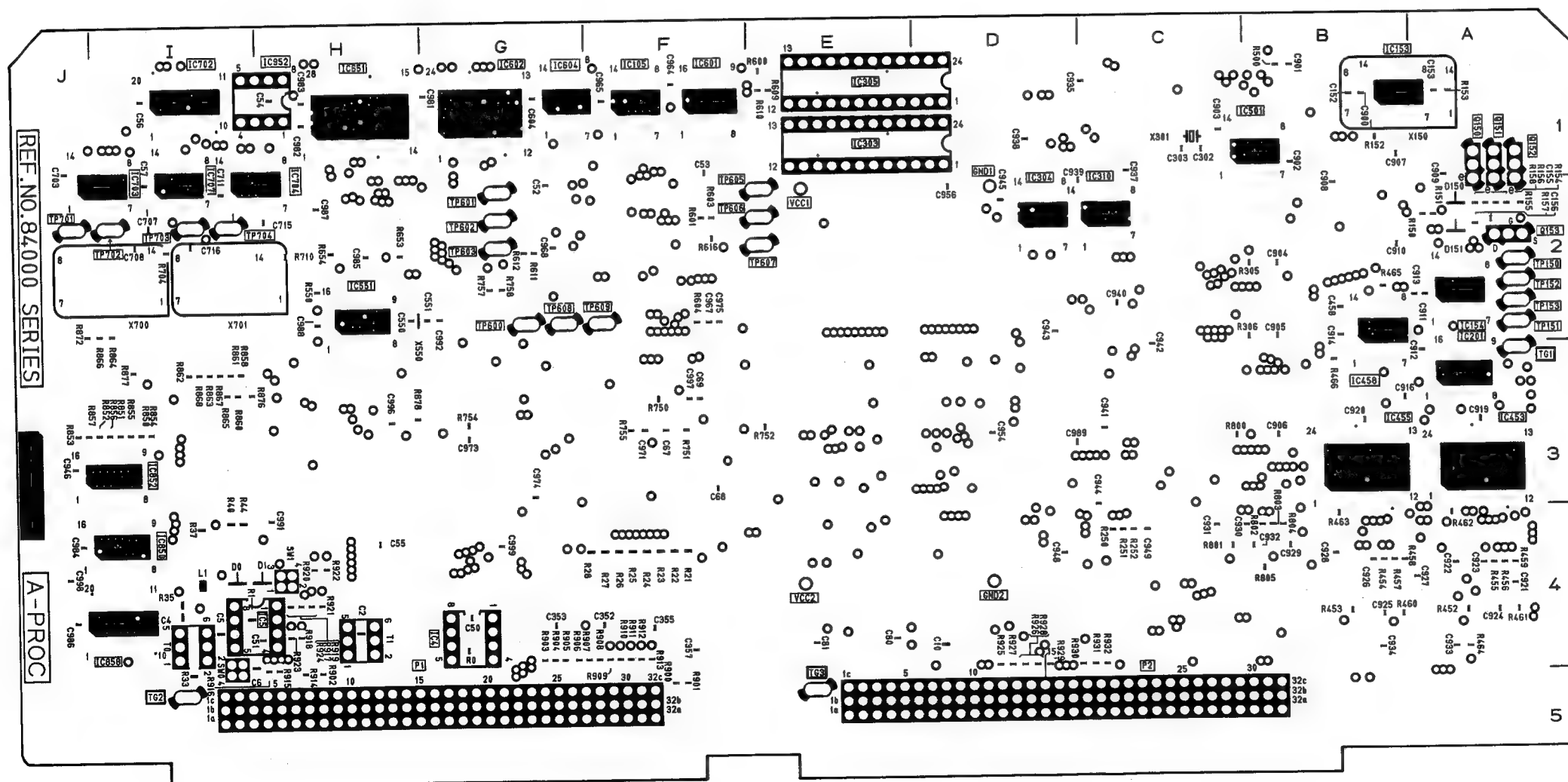
F7 A PROC P.C. BOARD (VEP84179B)



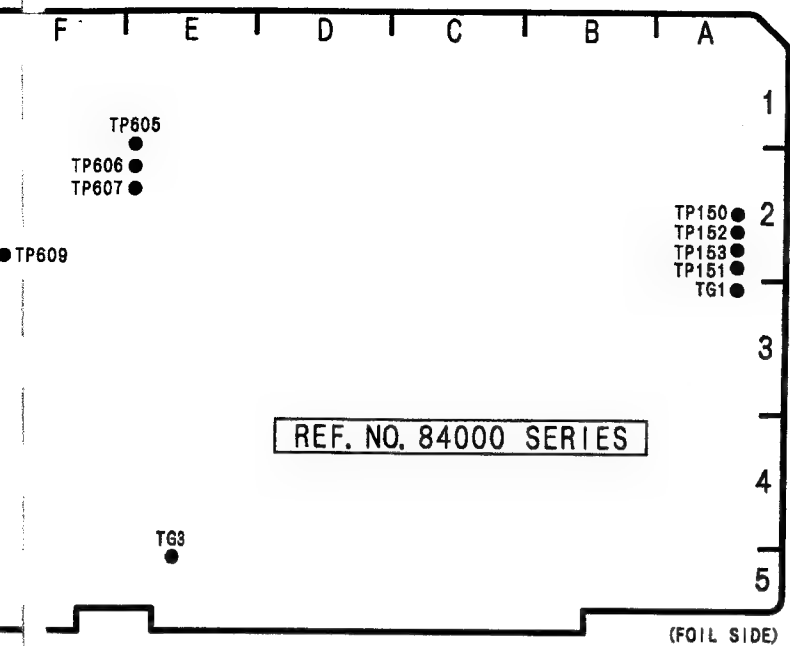
Transistors		
QB4150	A-1	
QB4151	A-1	
QB4152	A-1	
QB4153	A-2	

Integrated Circuits		
IC84001	C-4	Ⓢ
IC84002	D-4	Ⓢ
IC84003	C-4	Ⓢ
IC84004	G-4	
IC84005	I-4	
IC84006	D-3	Ⓢ
IC84007	F-3	Ⓢ
IC84008	F-3	Ⓢ
IC84010	E-4	Ⓢ
IC84011	E-4	Ⓢ
IC84012	I-3	Ⓢ
IC84013	C-4	Ⓢ
IC84100	E-3	Ⓢ

ADDRESS INFORMATION
 © ... COMPONENT SIDE
 Ⓢ ... FOIL SIDE

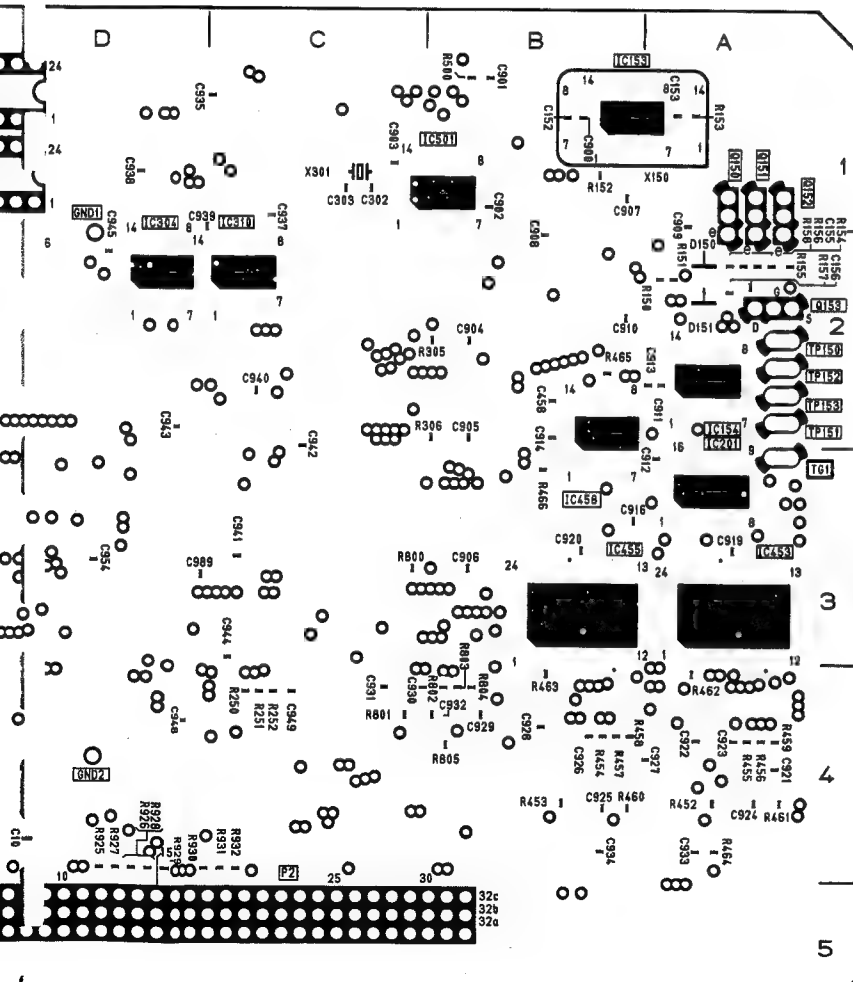


VJB



F7 A PROC																
Transistors			IC84101	E-3	⊙	IC84309	C-2	⊙	IC84603	F-2	⊙	IC84859	J-3	⊙	TP84609	F-2
Q84150	A-1		IC84102	E-3	⊙	IC84310	C-1	⊙	IC84604	G-1	⊙	IC84860	I-2	⊙	TP84701	J-2
Q84151	A-1		IC84103	E-3	⊙	IC84311	E-2	⊙	IC84650	H-2	⊙	IC84861	I-3	⊙	TP84702	I-2
Q84152	A-1		IC84104	E-3	⊙	IC84312	E-2	⊙	IC84651	H-1	⊙	IC84862	G-3	⊙	TP84703	I-2
Q84153	A-2		IC84105	F-1	⊙	IC84450	A-4	⊙	IC84702	I-1	⊙	IC84863	H-3	⊙	TP84704	I-2
			IC84151	B-1	⊙	IC84451	B-4	⊙	IC84703	I-1	⊙	IC84864	I-4	⊙	TG84001	A-3
			IC84152	B-1	⊙	IC84452	A-4	⊙	IC84704	H-1	⊙	IC84865	H-3	⊙	TG84002	I-5
			IC84153	B-1	⊙	IC84453	A-3	⊙	IC84705	I-1	⊙				TG84003	E-5
			IC84154	A-2	⊙	IC84454	B-4	⊙	IC84706	H-1	⊙	Test Points			Connectors	
			IC84200	B-2	⊙	IC84455	B-3	⊙	IC84707	I-1	⊙	TP84150	A-2			
			IC84201	A-2	⊙	IC84457	B-5	⊙	IC84750	F-3	⊙	TP84151	A-2			
			IC84250	C-4	⊙	IC84458	B-3	⊙	IC84751	G-3	⊙	TP84152	A-2			
			IC84251	C-3	⊙	IC84500	B-2	⊙	IC84752	G-4	⊙	TP84153	A-2			
			IC84301	E-2	⊙	IC84501	B-1	⊙	IC84801	B-4	⊙	TP84600	G-2			
			IC84302	D-2	⊙	IC84502	B-1	⊙	IC84802	C-3	⊙	TP84601	G-2			
			IC84303	E-1	⊙	IC84550	H-2	⊙	IC84850	I-4	⊙	TP84602	G-2			
			IC84304	D-1	⊙	IC84551	H-2	⊙	IC84852	I-3	⊙	TP84603	G-2			
			IC84305	E-1	⊙	IC84556	A-5	⊙	IC84855	J-3	⊙	TP84605	F-1			
			IC84306	C-2	⊙	IC84600	F-1	⊙	IC84856	I-3	⊙	TP84606	F-2			
			IC84307	B-2	⊙	IC84601	F-1	⊙	IC84857	J-2	⊙	TP84607	E-2			
			IC84308	B-3	⊙	IC84602	G-1	⊙	IC84858	I-4	⊙	TP84608	G-2			

ADDRESS INFORMATION
 ⊙ ... COMPONENT SIDE
 ⊙ ... FOIL SIDE

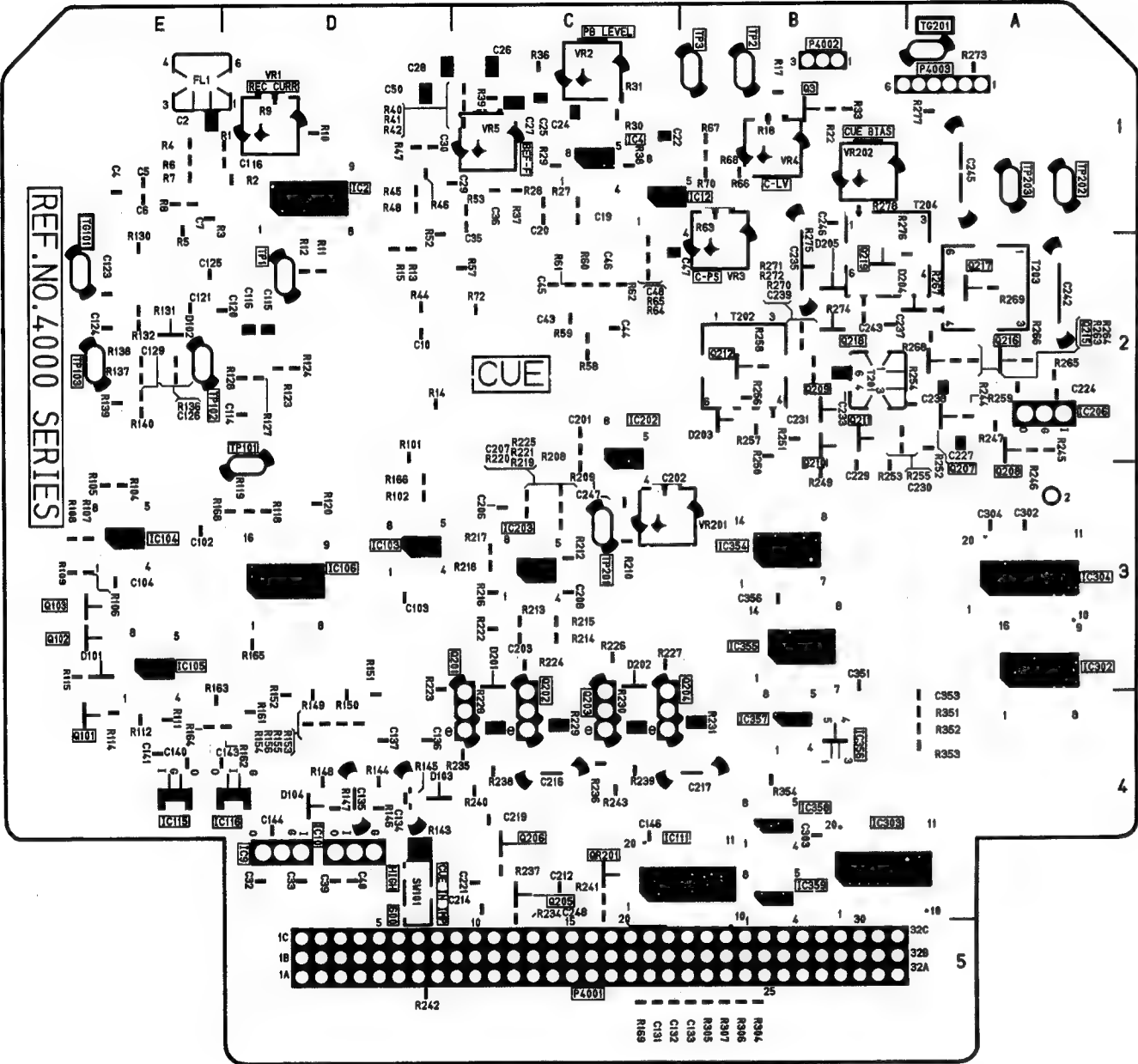


F8 ADDA																													
Transistors			Q4343	A-2	Ⓢ	QR4041	G-3	Ⓢ	IC4007	I-3	Ⓢ	IC4163	I-4	Ⓢ	IC4291	C-1	Ⓢ	IC4505	E-4	Ⓢ	TG4122	D-1							
Q4003	I-2	Ⓢ	Q4344	C-4	Ⓢ	QR4042	G-3	Ⓢ	IC4008	I-3	Ⓢ	IC4164	F-2	Ⓢ	IC4341	D-2	Ⓢ	IC4506	F-4	Ⓢ	Adjustments								
Q4041	H-2	Ⓢ	Q4345	D-3		QR4121	F-1	Ⓢ	IC4041	H-3	Ⓢ	IC4165	F-2	Ⓢ	IC4342	C-2	Ⓢ	Test Points			VR4002	I-3							
Q4161	F-1	Ⓢ	Q4346	D-3		QR4161	F-2	Ⓢ	IC4042	G-3	Ⓢ	IC4166	F-2	Ⓢ	IC4343	D-2	Ⓢ	TP83	H-2		VR4042	G-3							
Q4162	G-2	Ⓢ	Q4347	D-3		QR4162	F-2	Ⓢ	IC4043	H-4	Ⓢ	IC4167	F-3	Ⓢ	IC4344	C-2	Ⓢ	TP84	I-2		VR4161	G-2							
Q4163	G-3		Q4348	D-3		QR4221	D-2	Ⓢ	IC4044	H-4	Ⓢ	IC4168	F-3	Ⓢ	IC4345	D-2	Ⓢ	TP90	H-1		VR4221	E-2							
Q4164	F-2		Q4349	C-4	Ⓢ	QR4222	E-1	Ⓢ	IC4045	H-3	Ⓢ	IC4221	E-2	Ⓢ	IC4346	C-2	Ⓢ	TP121	F-1		VR4281	B-1							
Q4165	F-3		Q4350	C-4	Ⓢ	QR4281	C-1	Ⓢ	IC4046	H-3	Ⓢ	IC4222	D-2	Ⓢ	IC4347	C-3	Ⓢ	TP123	F-1		VR4282	D-1							
Q4166	G-3	Ⓢ	Q4415	C-3		QR4282	B-1	Ⓢ	IC4047	H-3	Ⓢ	IC4223	E-2	Ⓢ	IC4348	D-3	Ⓢ	TP126	F-1		Switches								
Q4167	F-3	Ⓢ	Q4416	C-3		QR4283	D-1	Ⓢ	IC4048	H-2	Ⓢ	IC4224	E-2	Ⓢ	IC4411	C-2	Ⓢ	TP161	F-2		SW4001	I-4							
Q4221	E-1	Ⓢ	Q4417	B-3		QR4284	B-1	Ⓢ	IC4081	H-1	Ⓢ	IC4225	E-3	Ⓢ	IC4412	B-2	Ⓢ	TP217	E-1		SW4041	H-4							
Q4222	F-2		Q4418	B-3		QR4285	D-1	Ⓢ	IC4082	G-1	Ⓢ	IC4226	E-3	Ⓢ	IC4413	B-2	Ⓢ	TP221	E-2		Connectors								
Q4223	F-3		Q4419	B-4	Ⓢ	QR4341	A-2	Ⓢ	IC4083	I-2	Ⓢ	IC4281	D-1	Ⓢ	IC4414	B-2	Ⓢ	TP281	C-1		P4001	G-4							
Q4224	E-2		Q4420	B-4	Ⓢ	QR4342	B-4	Ⓢ	IC4084	H-1	Ⓢ	IC4282	C-1	Ⓢ	IC4415	C-2	Ⓢ	TP283	C-1		P4002	D-4							
Q4225	E-3		Q4481	A-3	Ⓢ	Integrated Circuits			IC4085	H-1	Ⓢ	IC4283	D-1	Ⓢ	IC4416	B-2	Ⓢ	TP285	B-1										
Q4226	E-3	Ⓢ	Q4482	A-3	Ⓢ	IC4001	I-3	Ⓢ	IC4121	E-1	Ⓢ	IC4284	A-1	Ⓢ	IC4417	B-3	Ⓢ	TP286	D-1										
Q4227	E-3	Ⓢ	Q4483	A-3	Ⓢ	IC4002	I-3	Ⓢ	IC4122	F-1	Ⓢ	IC4285	A-1	Ⓢ	IC4418	C-3	Ⓢ	TP288	C-1										
Q4281	B-1	Ⓢ	Q4484	A-3	Ⓢ	IC4003	I-4	Ⓢ	IC4123	G-1	Ⓢ	IC4286	D-1	Ⓢ	IC4481	A-3	Ⓢ	TP289	B-1										
Q4282	D-1	Ⓢ	Transistor-Resistors			IC4004	I-4	Ⓢ	IC4124	E-1	Ⓢ	IC4287	A-1	Ⓢ	IC4501	F-4	Ⓢ	TG4001	G-2										
Q4341	A-2	Ⓢ	QR4001	I-3	Ⓢ	IC4005	I-3	Ⓢ	IC4125	F-1	Ⓢ	IC4288	A-1	Ⓢ	IC4502	E-4	Ⓢ	TG4002	I-2										
Q4342	A-2	Ⓢ	QR4002	I-3	Ⓢ	IC4006	I-2	Ⓢ	IC4161	G-2	Ⓢ	IC4289	E-1	Ⓢ	IC4503	D-4	Ⓢ	TG4121	F-1										
									IC4162	H-4	Ⓢ	IC4290	E-1	Ⓢ	IC4504	F-4	Ⓢ												

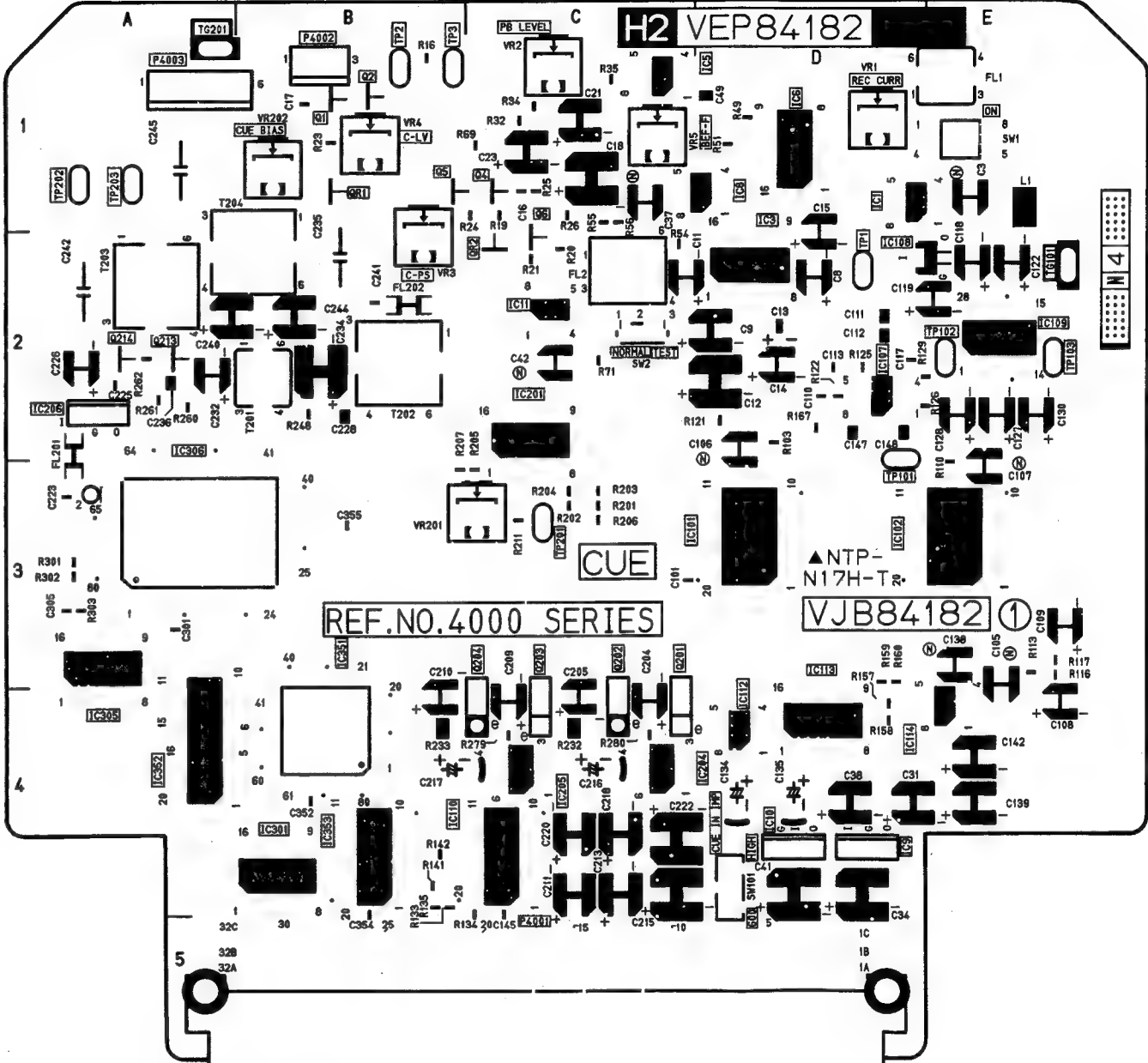
F8 ADDA P. C. BOARD



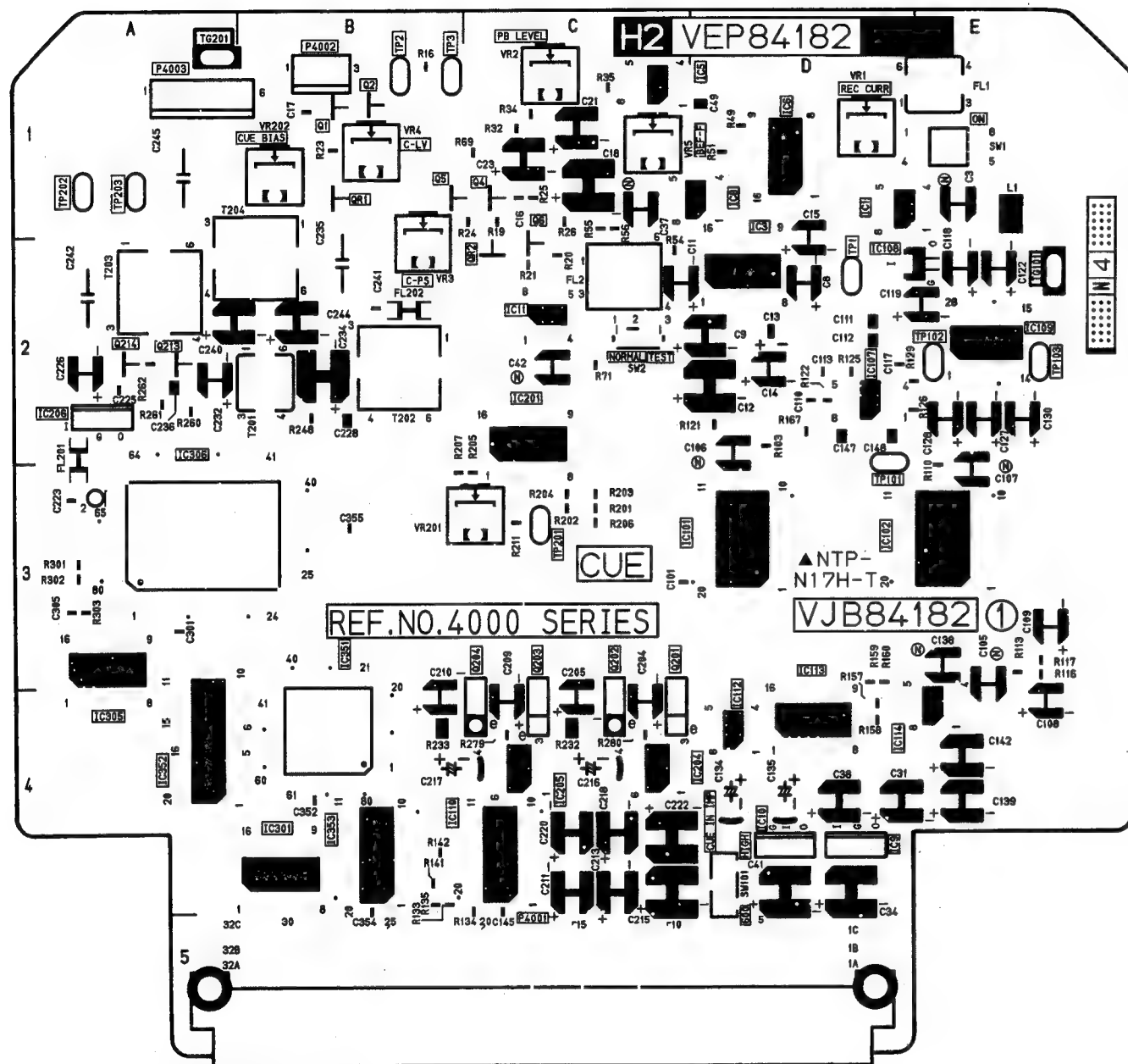
H2 CUE P.C. BOARD (VEP84182A)



(FOIL SIDE)



(COMPONENT SIDE)

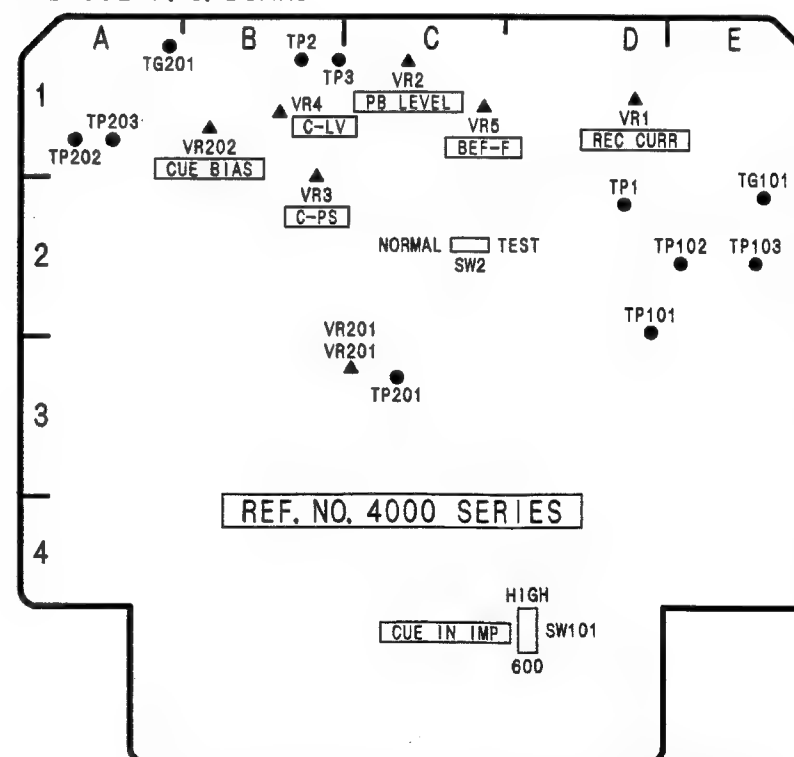


(COMPONENT SIDE)

H2 CUE											
Transistors			Transistor-Resistors			Integrated Circuits			Test Points		
Q4001	B-1	⊙	QR4001	B-1	⊙	IC4001	D-1	⊙	TP1	D-2	
Q4002	B-1	⊙	QR4002	C-2	⊙	IC4002	D-1	⊙	TP2	B-1	
Q4003	B-1	⊙	QR4201	C-4	⊙	IC4003	D-1	⊙	TP3	B-1	
Q4004	C-1	⊙				IC4004	C-1	⊙			
Q4005	B-1	⊙				IC4005	D-1	⊙			
Q4006	C-1	⊙				IC4006	D-1	⊙			
Q4101	E-4	⊙				IC4008	D-1	⊙			
Q4102	E-3	⊙				IC4009	D-4	⊙			
Q4103	E-3	⊙				IC4010	D-4	⊙			
Q4201	C-3	⊙				IC4011	C-2	⊙			
Q4202	C-3	⊙				IC4012	B-1	⊙			
Q4203	C-3	⊙				IC4101	C-3	⊙			
Q4204	C-3	⊙				IC4102	D-3	⊙			
Q4205	C-4	⊙				IC4103	D-3	⊙			
Q4206	C-4	⊙				IC4104	E-3	⊙			
Q4207	A-3	⊙				IC4105	E-3	⊙			
Q4208	A-3	⊙				IC4106	D-3	⊙			
Q4209	B-2	⊙				IC4107	D-2	⊙			
Q4210	B-2	⊙				IC4108	E-2	⊙			
Q4211	B-2	⊙				IC4109	E-2	⊙			
Q4212	B-2	⊙				IC4110	B-4	⊙			
Q4213	A-2	⊙				IC4111	C-4	⊙			
Q4214	A-2	⊙				IC4112	D-4	⊙			
Q4215	A-2	⊙									
Q4216	A-2	⊙									
Q4217	A-2	⊙									
Q4218	B-2	⊙									
Q4219	B-2	⊙									

ADDRESS INFORMATION
 ⊙ ... COMPONENT SIDE
 ⊙ ... FOIL SIDE

H2 CUE P. C. BOARD

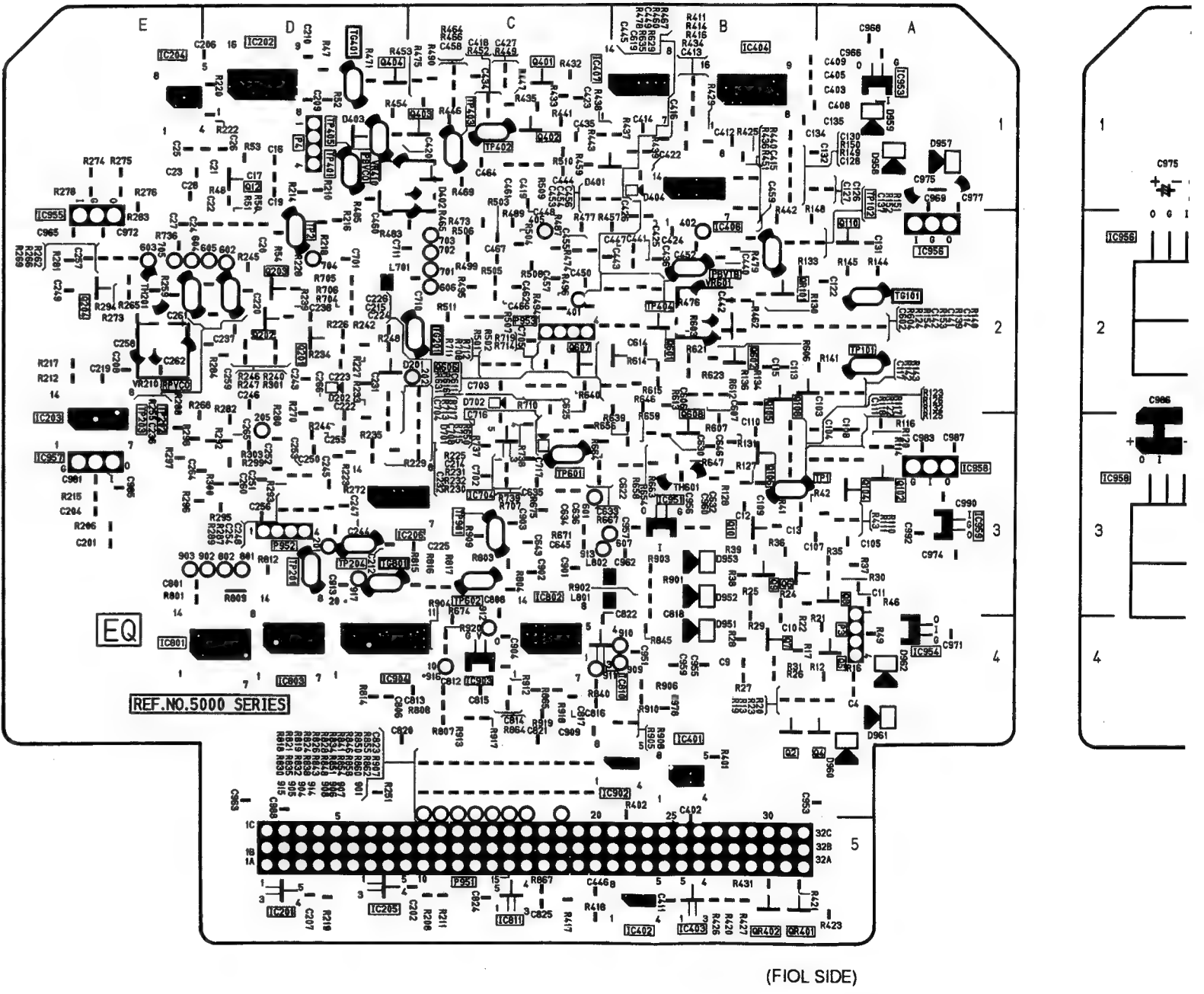
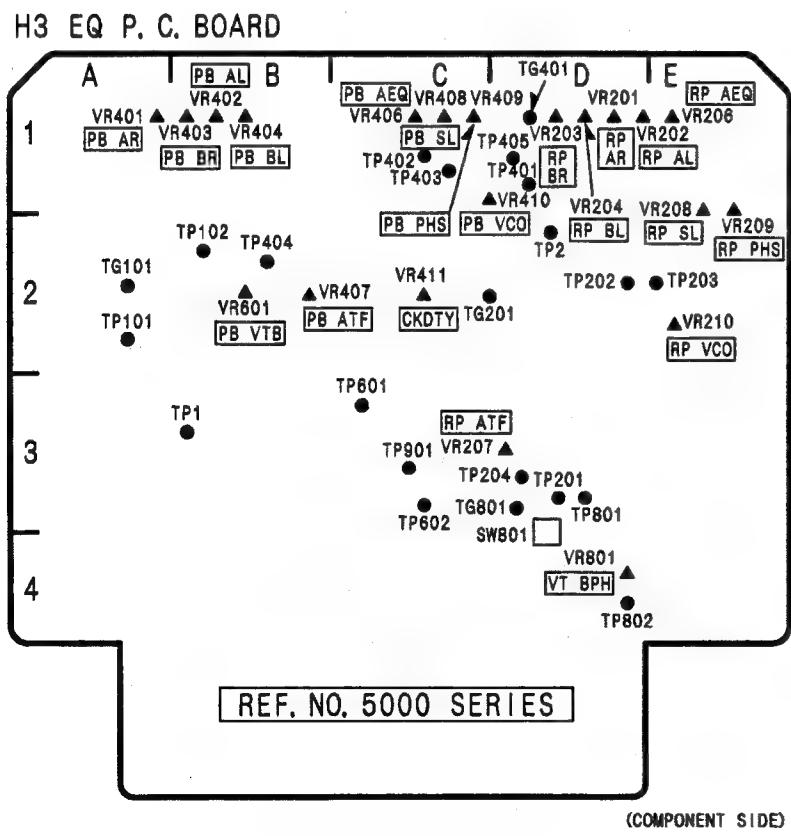


(COMPONENT SIDE)

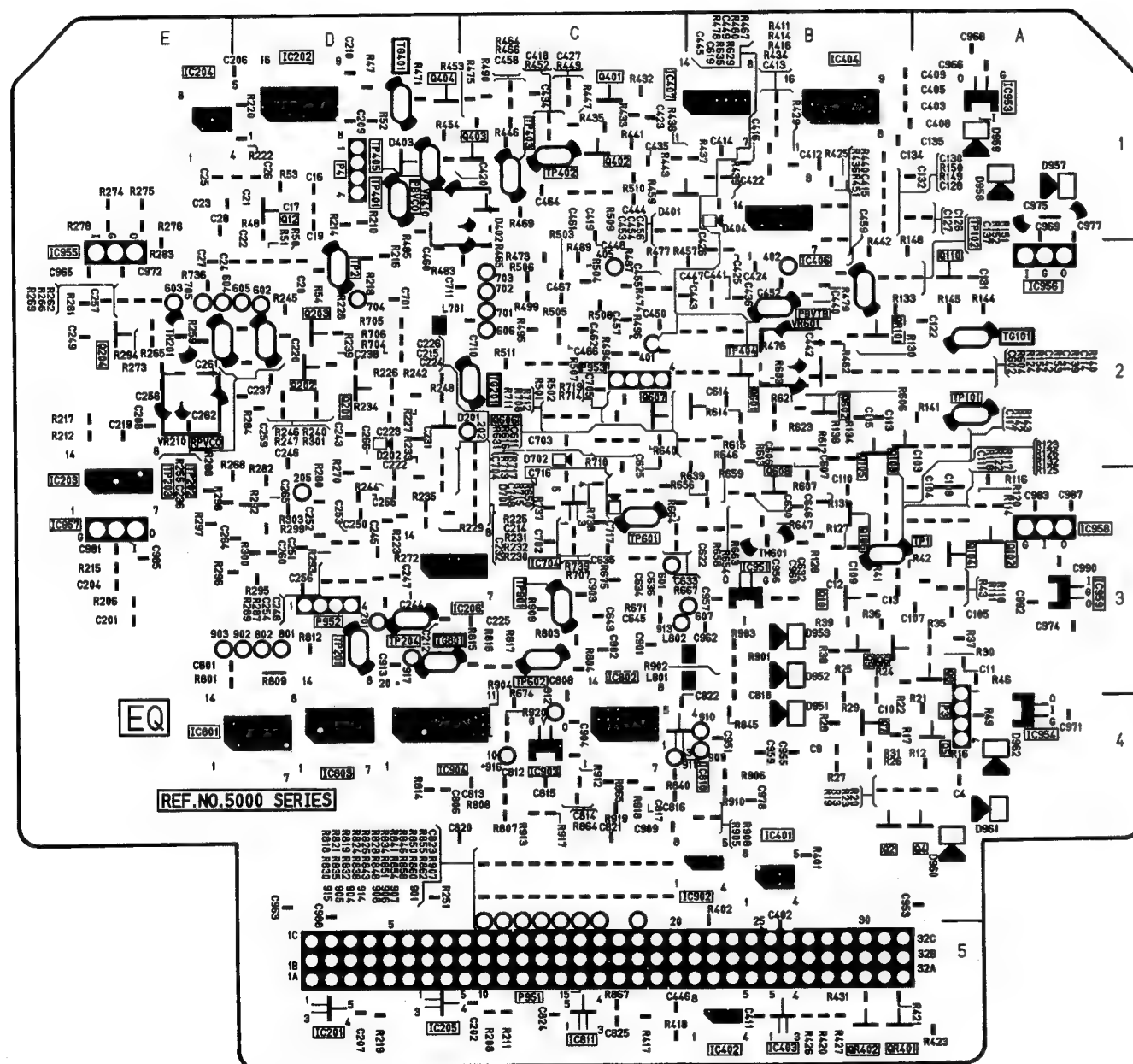
H3 EQ P.C. BOARD (VEP85048A)

H3 EQ									
Transistors		Q5603	B-2	IC5411	C-2	Test Points		VR5210	E-2
Q5001	A-4	Q5606	C-2	IC5601	B-2	TP1	B-3	VR5401	A-1
Q5002	B-4	Q5607	C-2	IC5602	B-3	TP2	D-2	VR5402	B-1
Q5003	B-4	Q5608	B-3	IC5603	C-3	TP101	A-2	VR5403	B-1
Q5004	A-4	Transistor-Resistors		IC5701	D-2	TP102	B-2	VR5404	B-1
Q5005	A-4	QR5101	B-2	IC5702	C-2	TP201	D-3	VR5406	C-1
Q5006	B-3	QR5401	B-5	IC5703	C-3	TP202	D-2	VR5407	B-2
Q5007	B-4	QR5402	B-5	IC5704	C-3	TP203	E-2	VR5408	C-1
Q5008	A-3	Integrated Circuits		IC5801	E-4	TP204	D-3	VR5409	C-1
Q5009	B-3	IC5001	E-1	IC5802	C-3	TP401	D-1	VR5410	D-1
Q5010	B-3	IC5101	B-2	IC5803	D-4	TP402	C-1	VR5411	C-2
Q5011	A-3	IC5102	B-1	IC5805	D-4	TP403	C-1	VR5801	B-2
Q5012	D-1	IC5201	D-5	IC5806	D-4	TP404	B-2	VR5801	D-4
Q5101	A-3	IC5202	D-1	IC5807	C-4	TP405	D-1	Switch	
Q5102	A-3	IC5203	E-3	IC5808	C-4	TP601	C-3	SW5801	D-3
Q5103	B-3	IC5204	E-1	IC5809	C-4	TP602	C-3	Connectors	
Q5104	A-3	IC5205	D-5	IC5811	C-3	TP801	D-3	P5003	A-4
Q5105	B-2	IC5206	C-3	IC5901	C-3	TP802	E-4	P5004	D-1
Q5106	B-2	IC5207	D-3	IC5902	B-4	TP901	C-3	P5951	C-5
Q5108	B-2	IC5208	D-2	IC5903	C-4	TG5101	A-2	P5952	D-3
Q5109	A-2	IC5209	D-2	IC5904	D-4	TG5201	C-2	P5953	C-2
Q5110	A-2	IC5210	E-3	IC5951	B-3	TG5401	D-1	Adjustments	
Q5201	D-2	IC5401	B-4	IC5952	B-3	VR201	D-1		
Q5203	D-2	IC5402	B-5	IC5953	A-1	VR202	E-1	Adjustments	
Q5204	E-2	IC5403	B-5	IC5954	E-2	VR203	D-1		
Q5401	C-1	IC5404	B-1	IC5955	E-3	VR204	D-1		
Q5402	C-1	IC5405	B-2	IC5956	A-2	VR206	E-1		
Q5403	C-1	IC5406	B-2	IC5957	E-3	VR207	D-3		
Q5404	D-1	IC5407	C-1	IC5958	A-3	VR208	E-1		
Q5601	B-2	IC5408	C-2	IC5959	A-3	VR209	E-1		
Q5602	B-2	IC5409	C-1						

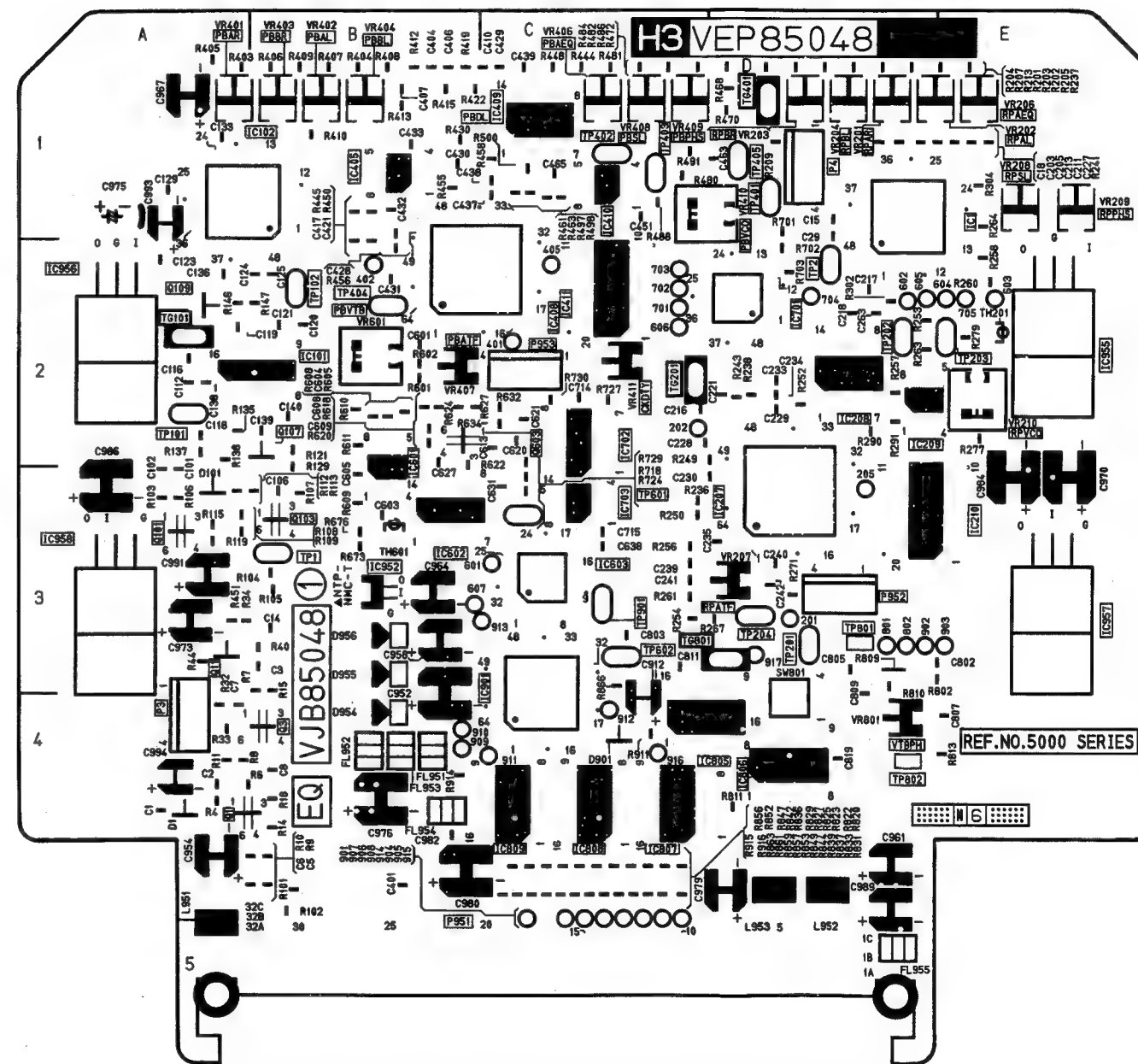
ADDRESS INFORMATION
⊙ ... COMPONENT SIDE
⊙ ... FOIL SIDE



H3 EQ P.C. BOARD (VEP85048A)

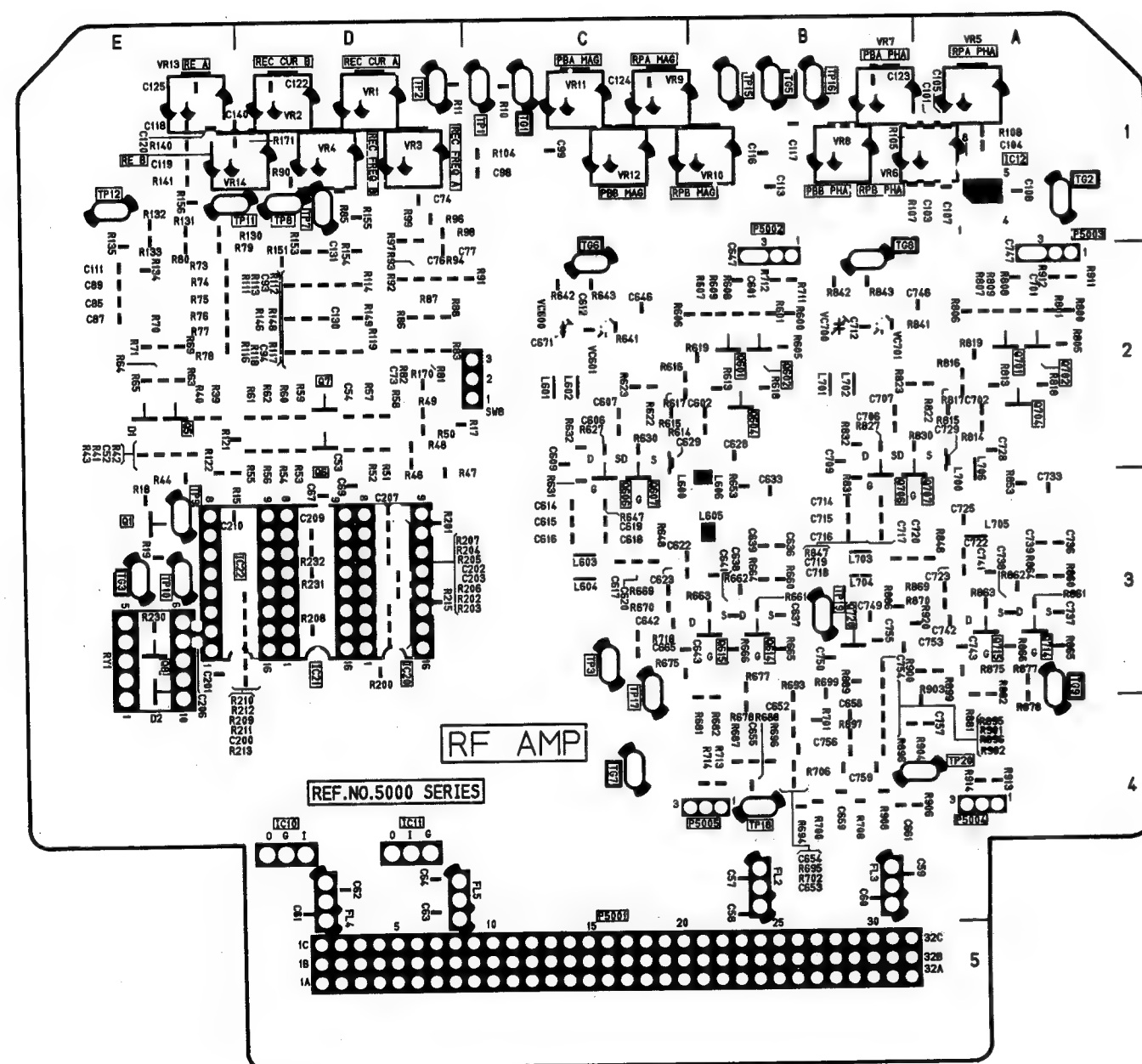


(FIOL SIDE)

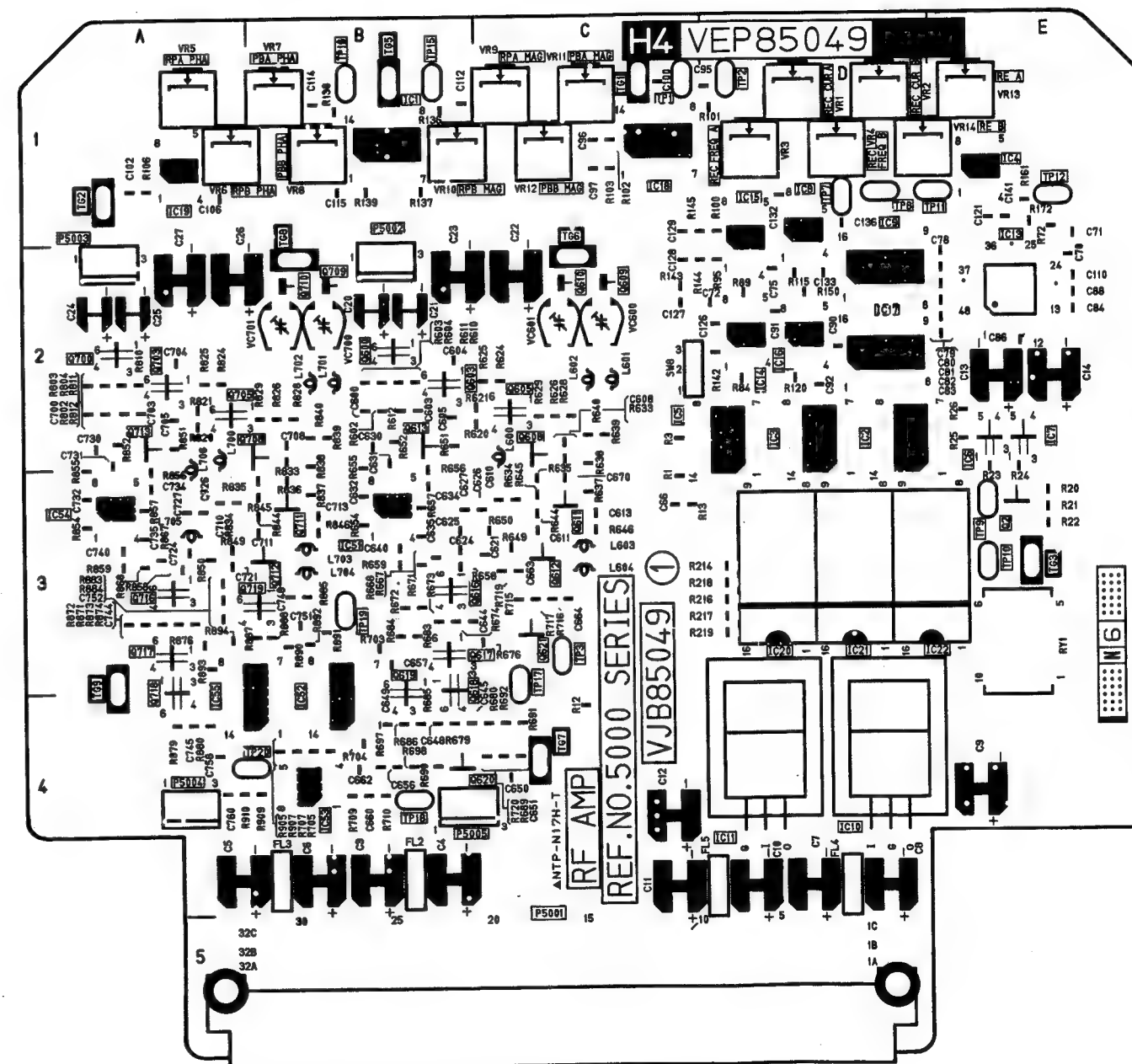


(COMPONENT SIDE)

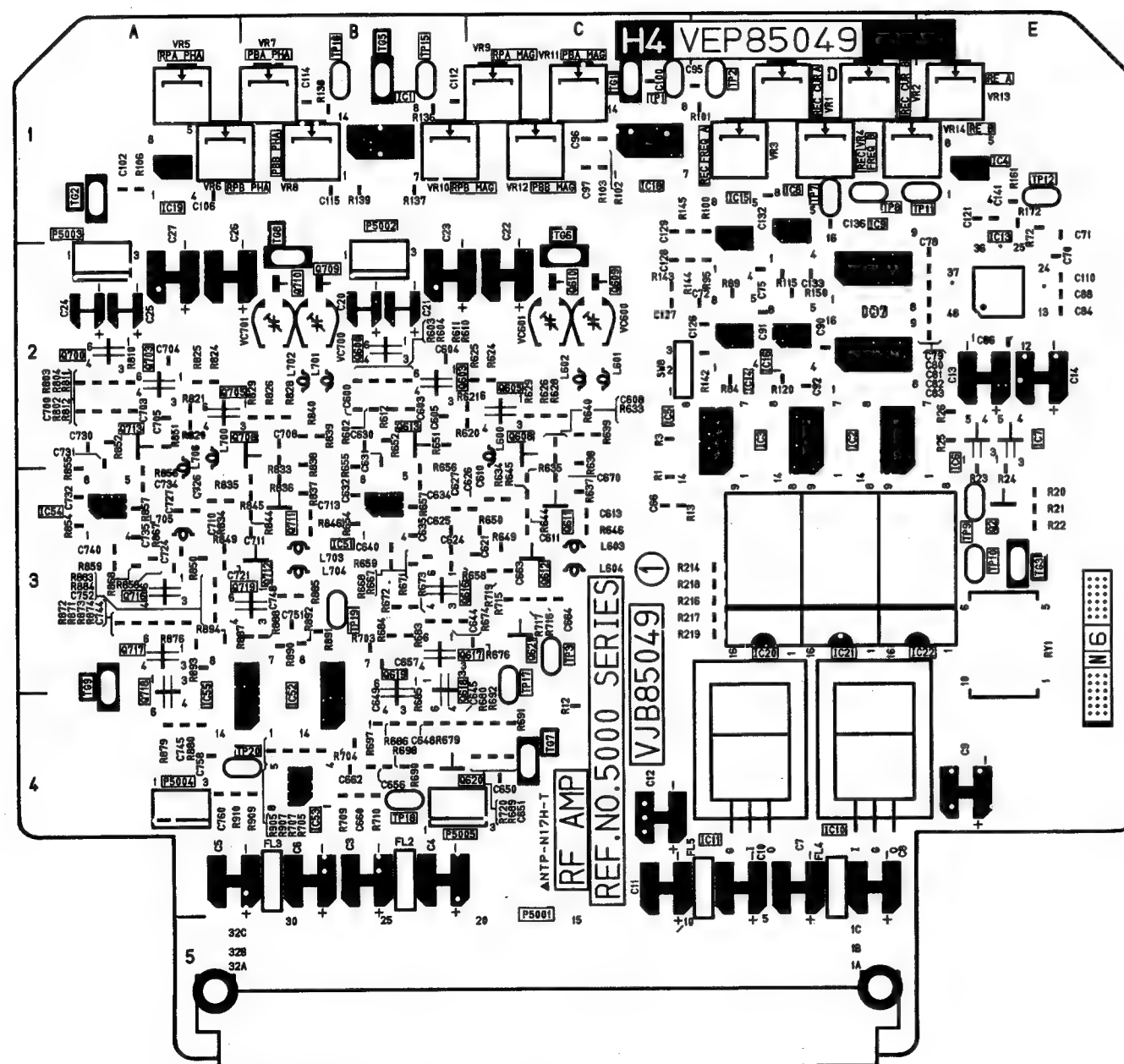
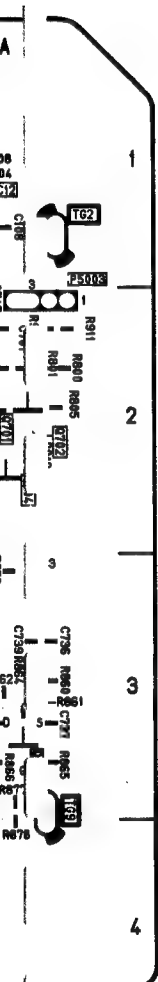
H4 RF AMP P.C. BOARD (VEP85049A)



(FOIL SIDE)



(COMPONENT SIDE)

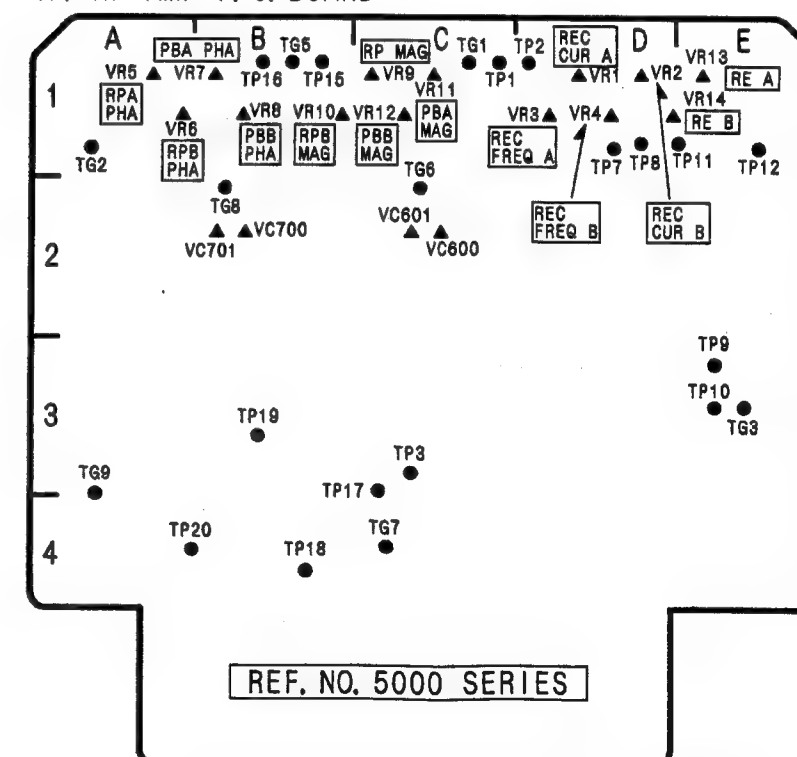


(COMPONENT SIDE)

H4 RF AMP									
Transistors		Q5704		A-2		IC5016		D-2	
Q5001	E-3	Q5705	A-2	Q5706	B-3	IC5017	D-2	TG5007	C-4
Q5002	E-3	Q5707	A-3	Q5708	B-2	IC5018	C-1	TG5008	B-2
Q5005	E-2	Q5709	B-2	Q5710	B-2	IC5019	A-1	TG5009	A-3
Q5006	D-2	Q5711	B-3	Q5712	B-3	IC5020	D-3	Adjustments	
Q5007	D-2	Q5713	A-2	Q5714	A-3	IC5021	D-3	VC5600	C-2
Q5008	E-3	Q5715	A-3	Q5716	A-3	IC5022	E-3	VC5601	C-2
Q5600	B-2	Q5717	A-3	Q5718	A-3	IC5051	B-3	VC5700	B-2
Q5601	B-2	Q5719	B-3	Q5720	B-3	IC5052	B-4	VC5701	B-2
Q5602	B-2					IC5053	B-4	VR5001	D-1
Q5603	B-2					IC5054	A-3	VR5002	D-1
Q5604	B-2					IC5055	A-4	VR5003	D-1
Q5605	C-2					Test Points		VR5004	D-1
Q5606	C-3					TP1	C-1	VR5005	A-1
Q5607	C-3					TP2	D-1	VR5006	A-1
Q5608	C-2					TP3	C-3	VR5007	B-1
Q5609	C-2					TP7	D-1	VR5008	B-1
Q5610	C-2					TP8	D-1	VR5009	C-1
Q5611	C-3					TP9	E-3	VR5010	B-1
Q5612	C-3					TP10	E-3	VR5011	C-1
Q5613	B-2					TP11	D-1	VR5012	C-1
Q5614	B-3					TP12	E-1	VR5013	E-1
Q5615	B-3					TP15	B-1	VR5014	E-1
Q5616	B-3					TP16	B-1	Switch	
Q5617	C-3					TP17	C-3	SW5008	C-2
Q5618	B-3					TP18	B-4	Connectors	
Q5619	B-3					TP19	B-3	P5001	C-4
Q5620	B-4					TP20	A-4	P5002	B-1
Q5621	C-3					TG5001	C-1	P5003	A-1
Q5700	A-2					TG5002	A-1	P5004	A-4
Q5701	A-2					TG5003	E-3	P5005	B-4
Q5702	A-2					TG5005	B-1		
Q5703	A-2					TG5006	C-1		

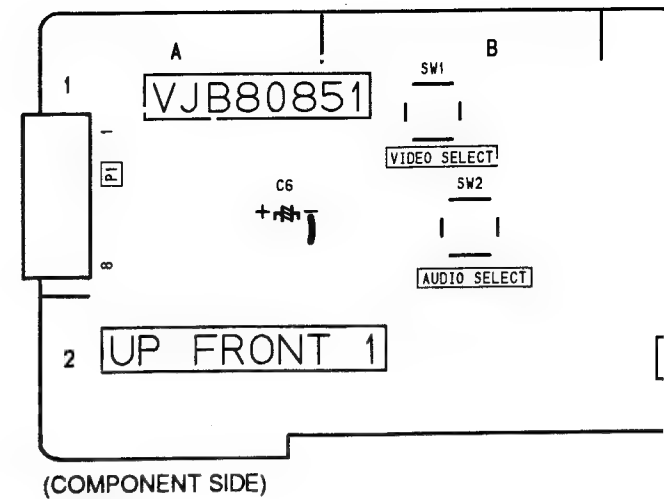
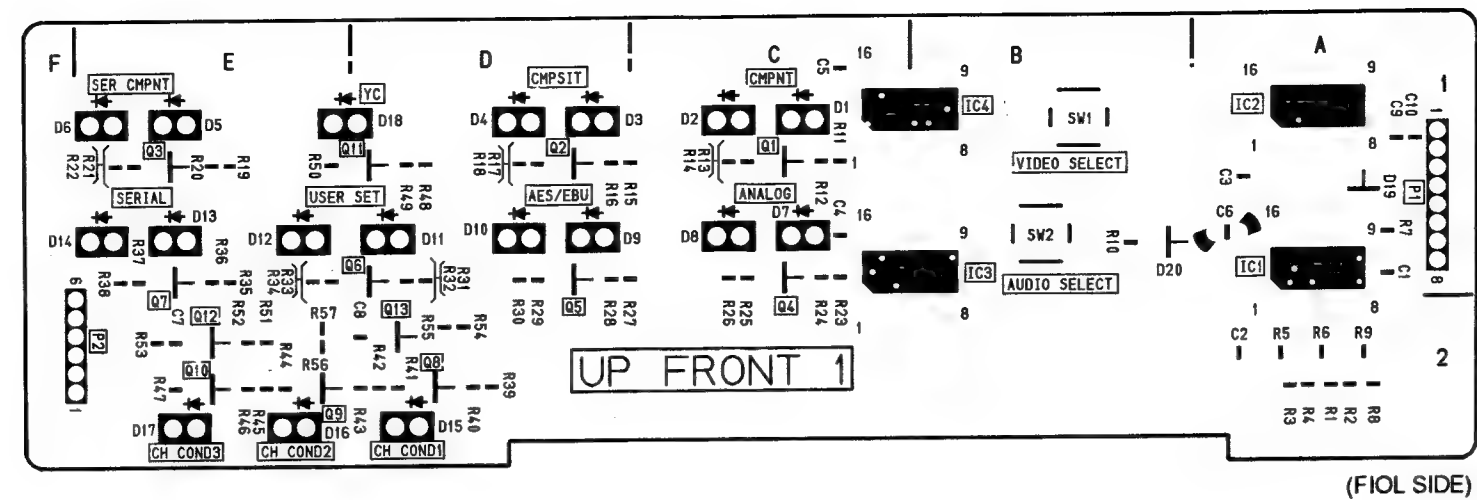
ADDRESS INFORMATION
 © ... COMPONENT SIDE
 Ⓢ ... FOIL SIDE

H4 RF AMP P. C. BOARD

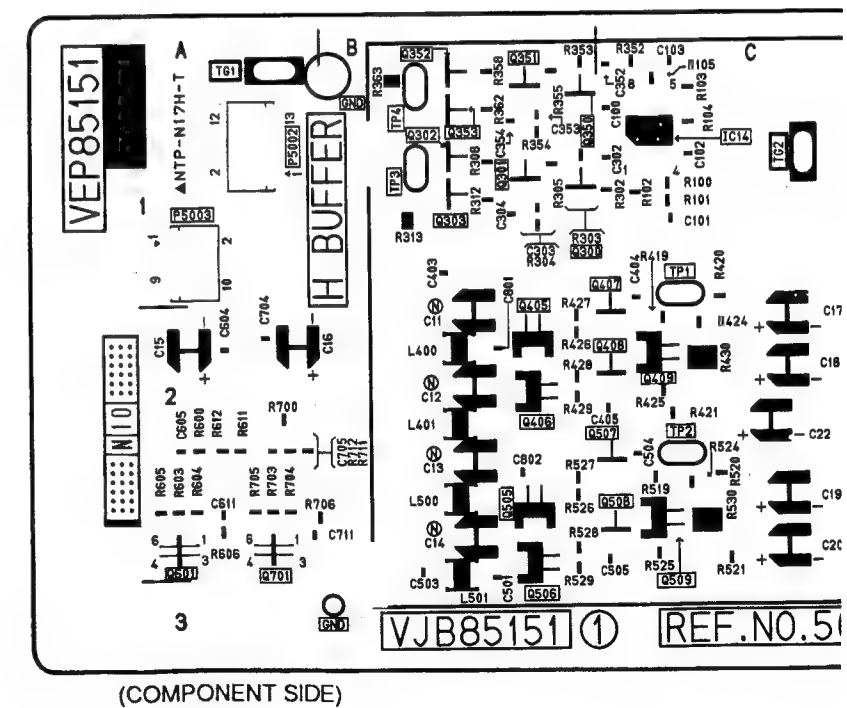
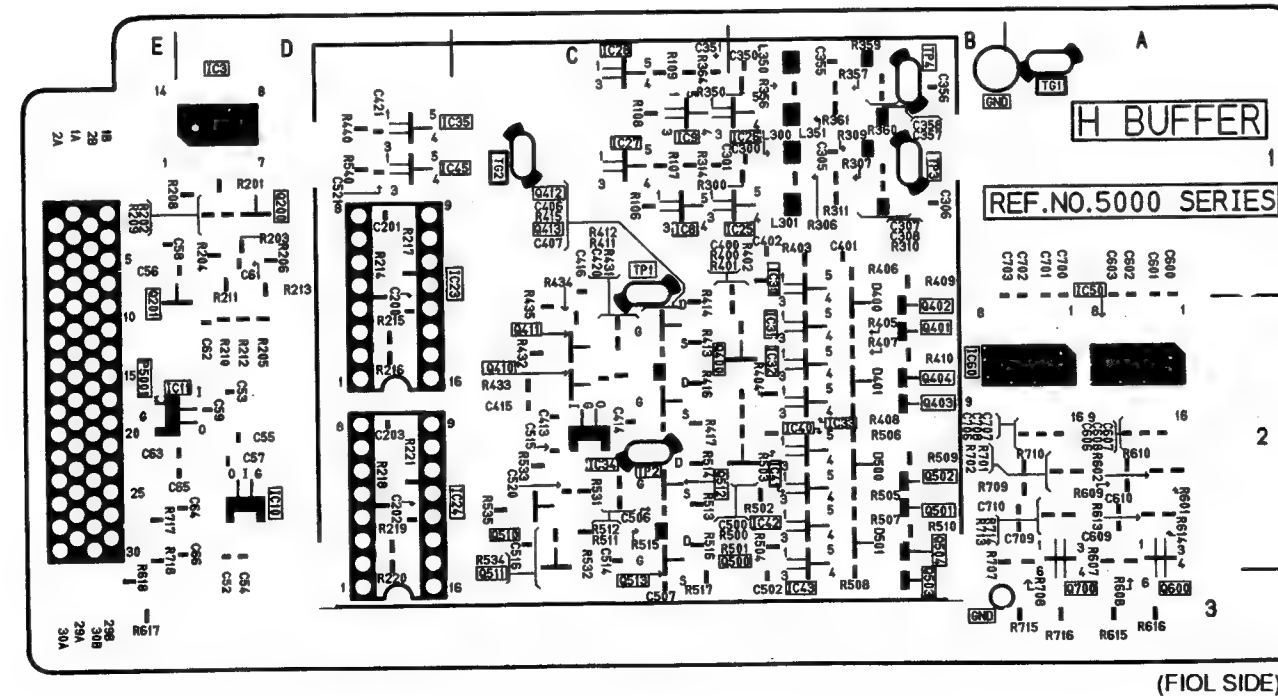
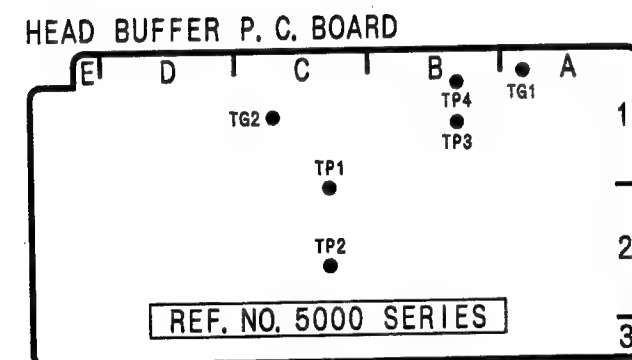


(COMPONENT SIDE)

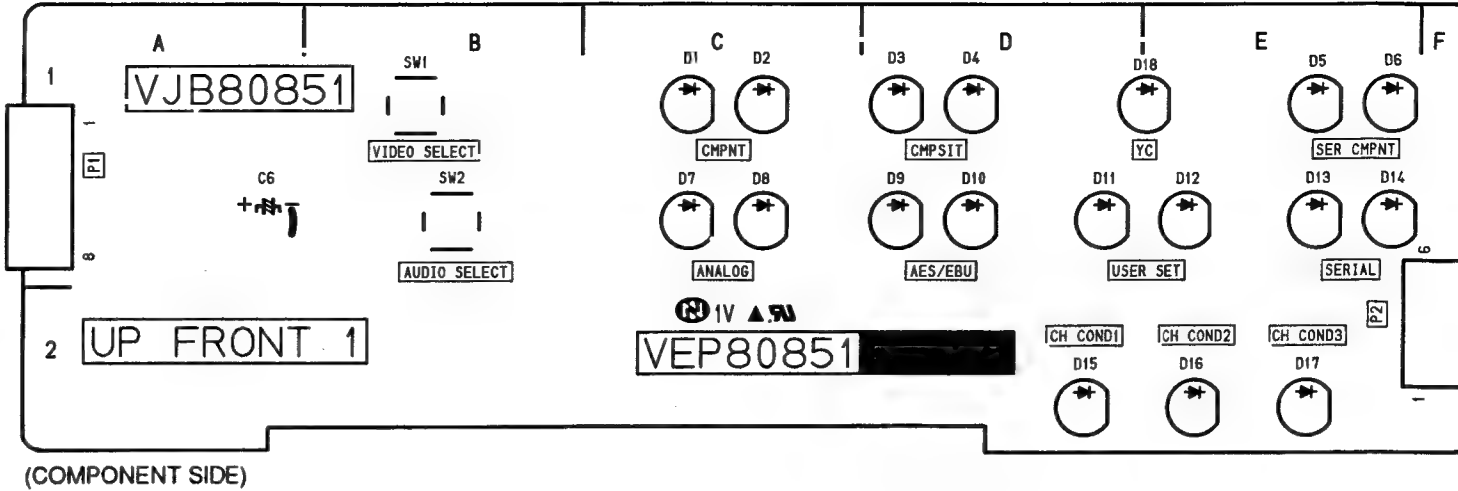
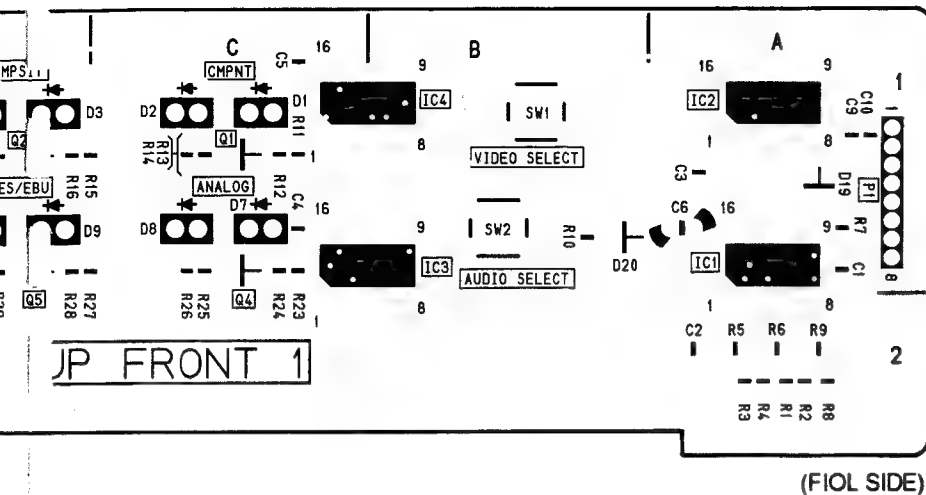
UP FRONT 1 P.C. BOARD (VEP80851A)



HEAD BUFFER P.C. BOARD (VEP85151A)



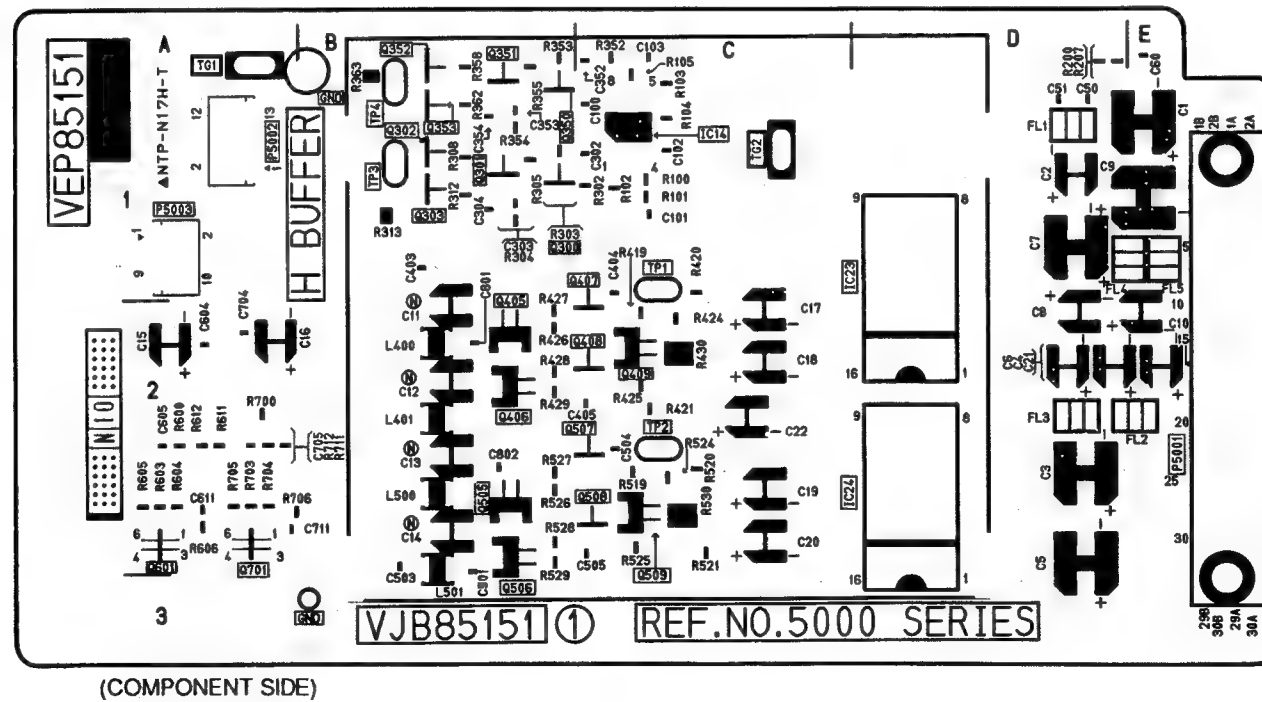
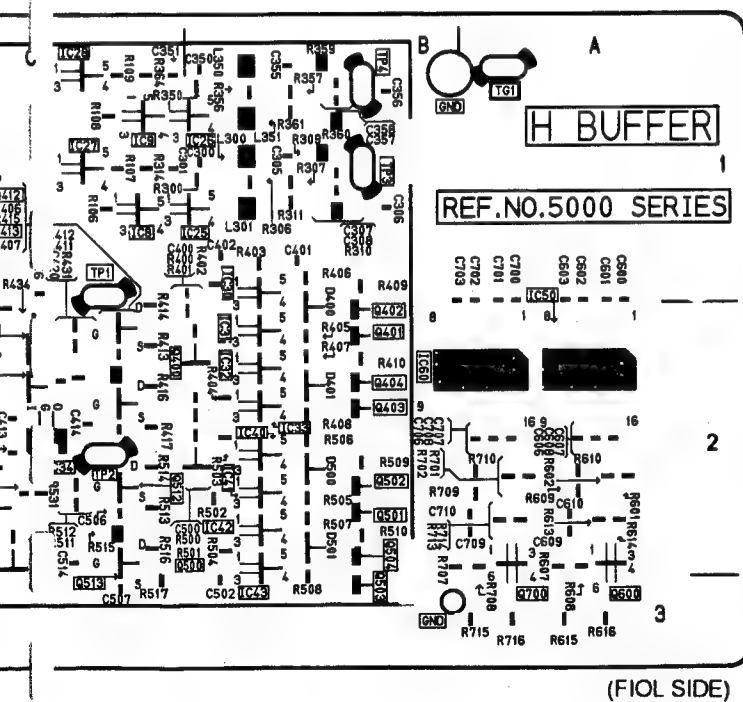
(VEP80851A)



UP FRONT 1		
Transistors		
Q1	C-1	⊙
Q2	D-1	⊙
Q3	E-1	⊙
Q4	C-2	⊙
Q5	D-2	⊙
Q6	D-1	⊙
Q7	E-1	⊙
Q8	D-2	⊙
Q9	E-2	⊙
Q10	E-2	⊙
Q11	D-1	⊙
Q12	E-2	⊙
Q13	D-2	⊙
Integrated Circuits		
IC1	A-1	⊙
IC2	A-1	⊙
IC3	B-1	⊙
IC4	B-1	⊙
Switches		
SW1	B-1	
SW2	B-1	
Connectors		
P1	A-1	
P2	E-2	

ADDRESS INFORMATION
 ⊙ ... COMPONENT SIDE
 ⊙ ... FOIL SIDE

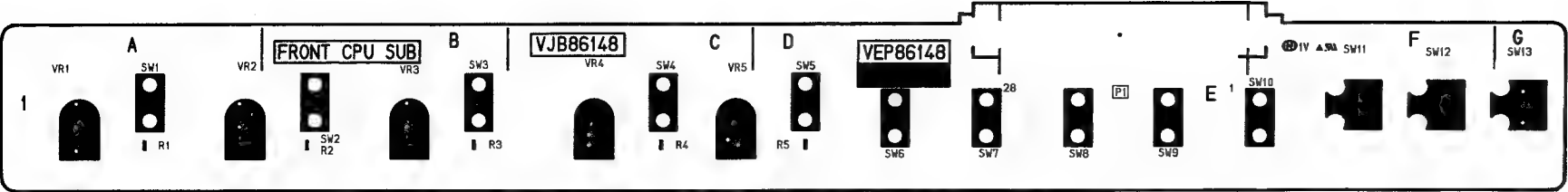
(VEP85151A)



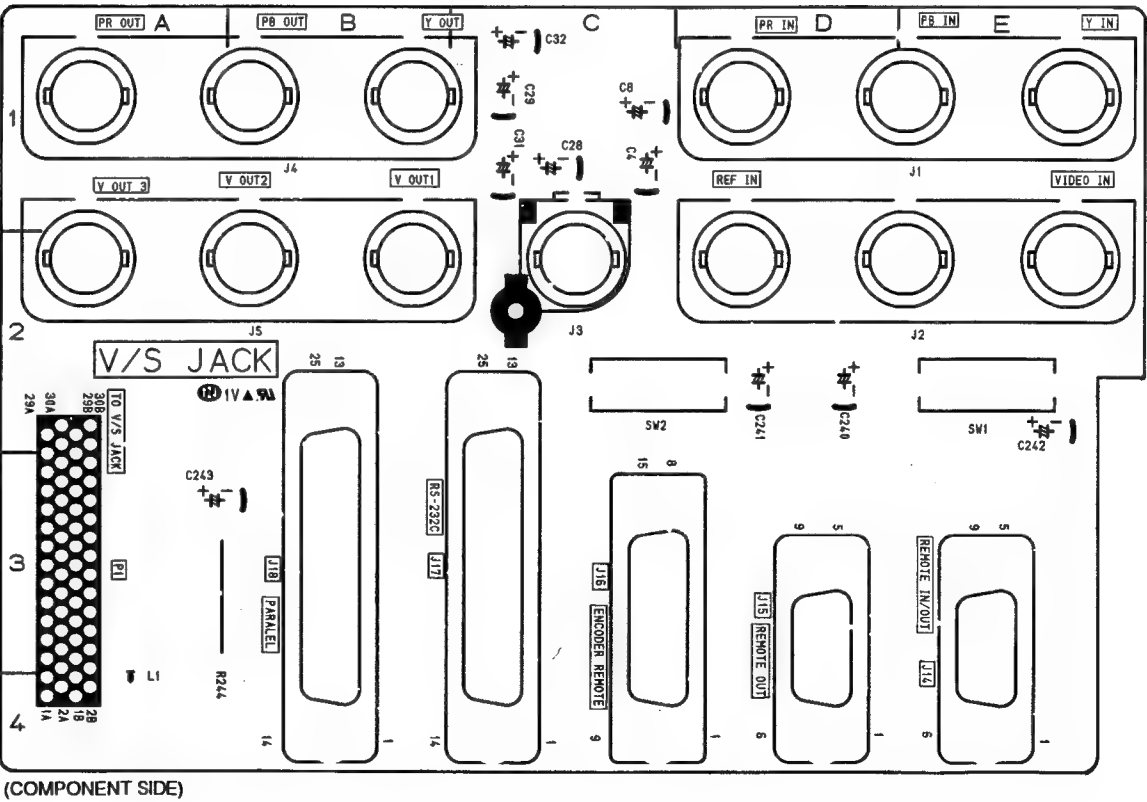
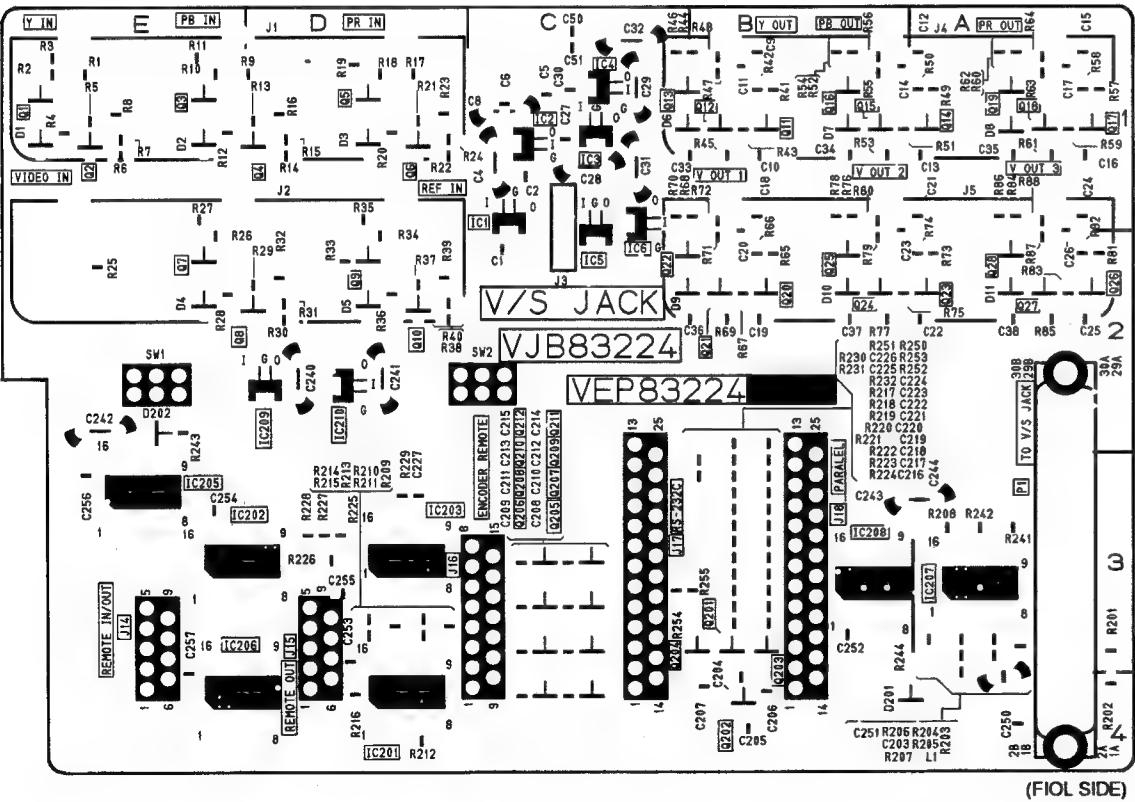
HEAD BUFFER					
Transistors		Integrated Circuits			
Q5200	D-1	⊙	IC5003	D-1	⊙
Q5201	E-1	⊙	IC5008	C-1	⊙
Q5300	B-1	⊙	IC5009	C-1	⊙
Q5301	B-1	⊙	IC5010	D-2	⊙
Q5302	B-1	⊙	IC5011	E-2	⊙
Q5303	B-1	⊙	IC5014	C-1	⊙
Q5350	B-1	⊙	IC5023	D-1	
Q5351	B-1	⊙	IC5024	D-2	
Q5352	B-1	⊙	IC5025	B-1	⊙
Q5353	B-1	⊙	IC5026	B-1	⊙
Q5400	C-2	⊙	IC5027	C-1	⊙
Q5401	B-2	⊙	IC5028	C-1	⊙
Q5402	B-2	⊙	IC5030	B-1	⊙
Q5403	B-2	⊙	IC5031	B-2	⊙
Q5404	B-2	⊙	IC5032	B-2	⊙
Q5405	B-2	⊙	IC5033	B-2	⊙
Q5406	B-2	⊙	IC5034	C-2	⊙
Q5407	C-1	⊙	IC5035	D-1	⊙
Q5408	C-2	⊙	IC5040	B-2	⊙
Q5409	C-2	⊙	IC5041	B-2	⊙
Q5410	C-2	⊙	IC5042	B-2	⊙
Q5411	C-2	⊙	IC5043	B-3	⊙
Q5412	C-1	⊙	IC5045	D-1	⊙
Q5413	C-1	⊙	IC5050	A-2	⊙
Q5500	C-2	⊙	IC5060	B-2	⊙
Q5501	B-2	⊙	Test Points		
Q5502	B-2	⊙	TP1	C-1	
Q5503	B-3	⊙	TP2	C-2	
Q5504	B-2	⊙	TP3	B-1	
Q5505	B-2	⊙	TP4	B-1	
Q5506	B-3	⊙	TG5001	A-1	
Q5507	C-2	⊙	TG5002	C-1	
Q5508	C-2	⊙	Connectors		
Q5509	C-2	⊙	P5001	E-2	
Q5510	C-2	⊙	P5002	A-1	⊙
Q5511	C-2	⊙	P5003	A-1	⊙
Q5512	C-2	⊙			
Q5513	C-3	⊙			
Q5600	A-3	⊙			
Q5601	A-2	⊙			
Q5700	A-3	⊙			
Q5701	A-2	⊙			

ADDRESS INFORMATION
 ⊙ ... COMPONENT SIDE
 ⊙ ... FOIL SIDE

FRONT CPU SUB P.C. BOARD (VEP86148A)



V/S JACK P.C. BOARD (VEP83224A)



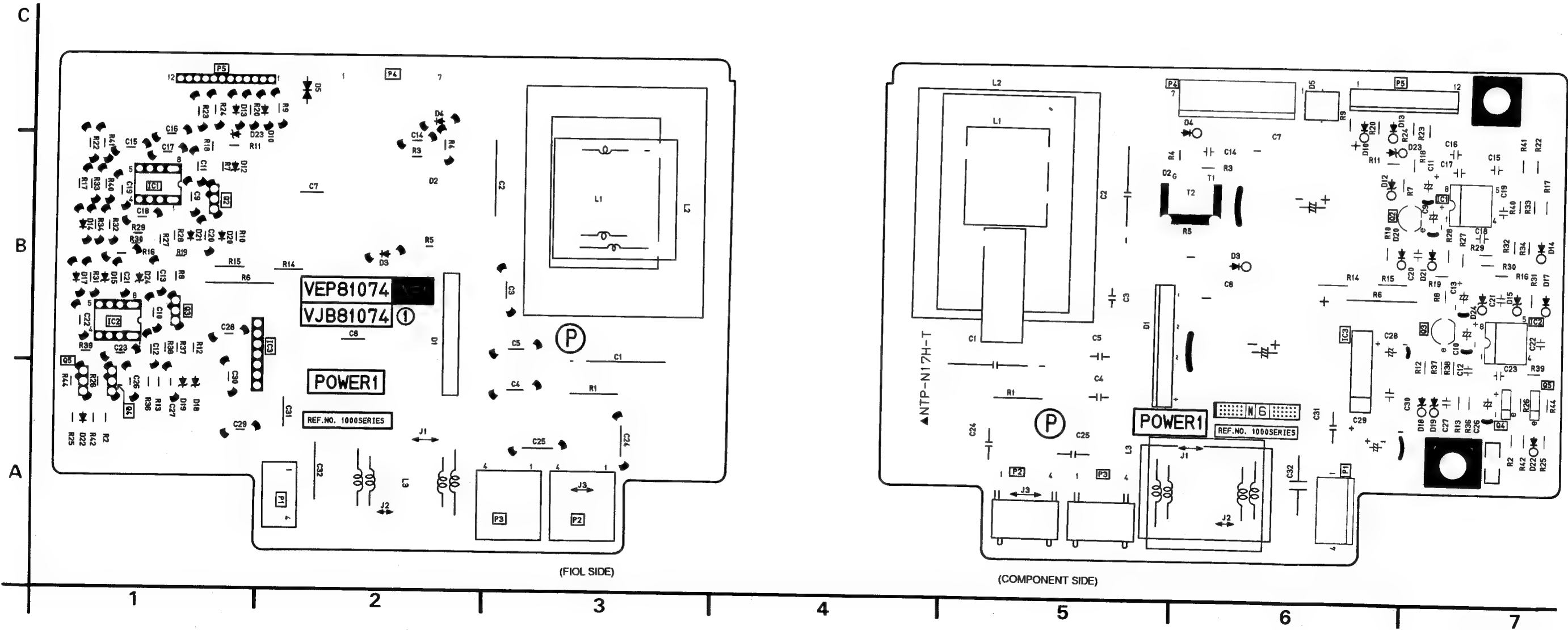
V/S JACK		
Transistors		
Q1	E-1	Ⓢ
Q2	E-1	Ⓢ
Q3	E-1	Ⓢ
Q4	D-1	Ⓢ
Q5	D-1	Ⓢ
Q6	D-1	Ⓢ
Q7	E-2	Ⓢ
Q8	E-2	Ⓢ
Q9	D-2	Ⓢ
Q10	D-2	Ⓢ
Q11	B-1	Ⓢ
Q12	B-1	Ⓢ
Q13	C-1	Ⓢ
Q14	A-1	Ⓢ
Q15	B-1	Ⓢ
Q16	B-1	Ⓢ
Q17	A-1	Ⓢ
Q18	A-1	Ⓢ
Q19	A-1	Ⓢ
Q20	B-2	Ⓢ
Q21	B-2	Ⓢ
Q22	C-2	Ⓢ
Q23	A-2	Ⓢ
Q24	B-2	Ⓢ
Q25	B-2	Ⓢ
Q26	A-2	Ⓢ
Q27	A-2	Ⓢ
Q28	A-2	Ⓢ
Q201	B-3	Ⓢ
Q202	B-4	Ⓢ
Q203	B-3	Ⓢ
Q204	C-3	Ⓢ
Q205	C-3	Ⓢ
Q206	C-3	Ⓢ
Q207	C-3	Ⓢ
Q208	C-3	Ⓢ
Q209	C-3	Ⓢ
Q210	C-3	Ⓢ
Q211	C-2	Ⓢ
Q212	C-2	Ⓢ
Integrated Circuits		
IC1	C-1	Ⓢ
IC2	C-1	Ⓢ
IC3	C-1	Ⓢ
IC4	C-1	Ⓢ
IC5	C-2	Ⓢ
IC6	C-2	Ⓢ
IC201	D-4	Ⓢ
IC202	E-3	Ⓢ
IC203	D-3	Ⓢ
IC205	E-3	Ⓢ
IC206	E-3	Ⓢ
IC207	A-3	Ⓢ
IC208	B-3	Ⓢ
IC209	D-2	Ⓢ
IC210	D-2	Ⓢ
Switches		
SW1	E-2	
SW2	C-2	
Connector		
P1	A-3	

ADDRESS INFORMATION
Ⓢ ... COMPONENT SIDE
Ⓢ ... FOIL SIDE

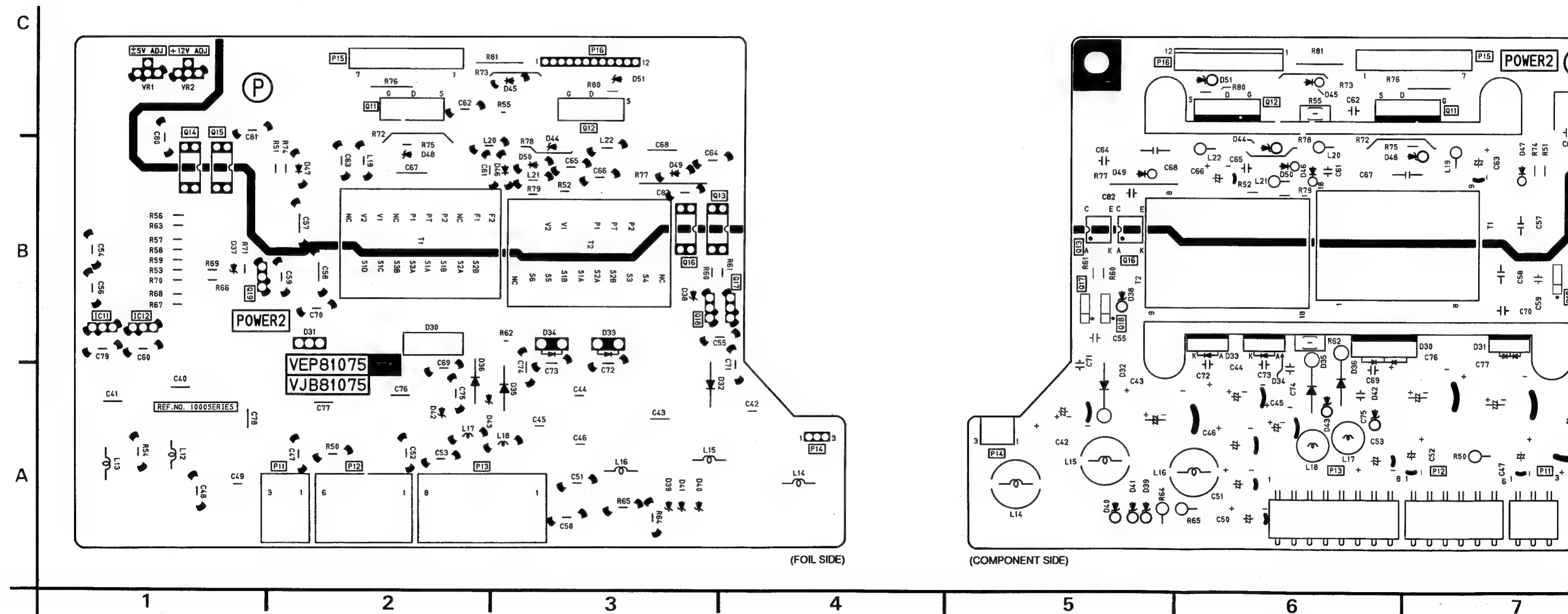
POWER 1 P.C. BOARD (VEP81074B)

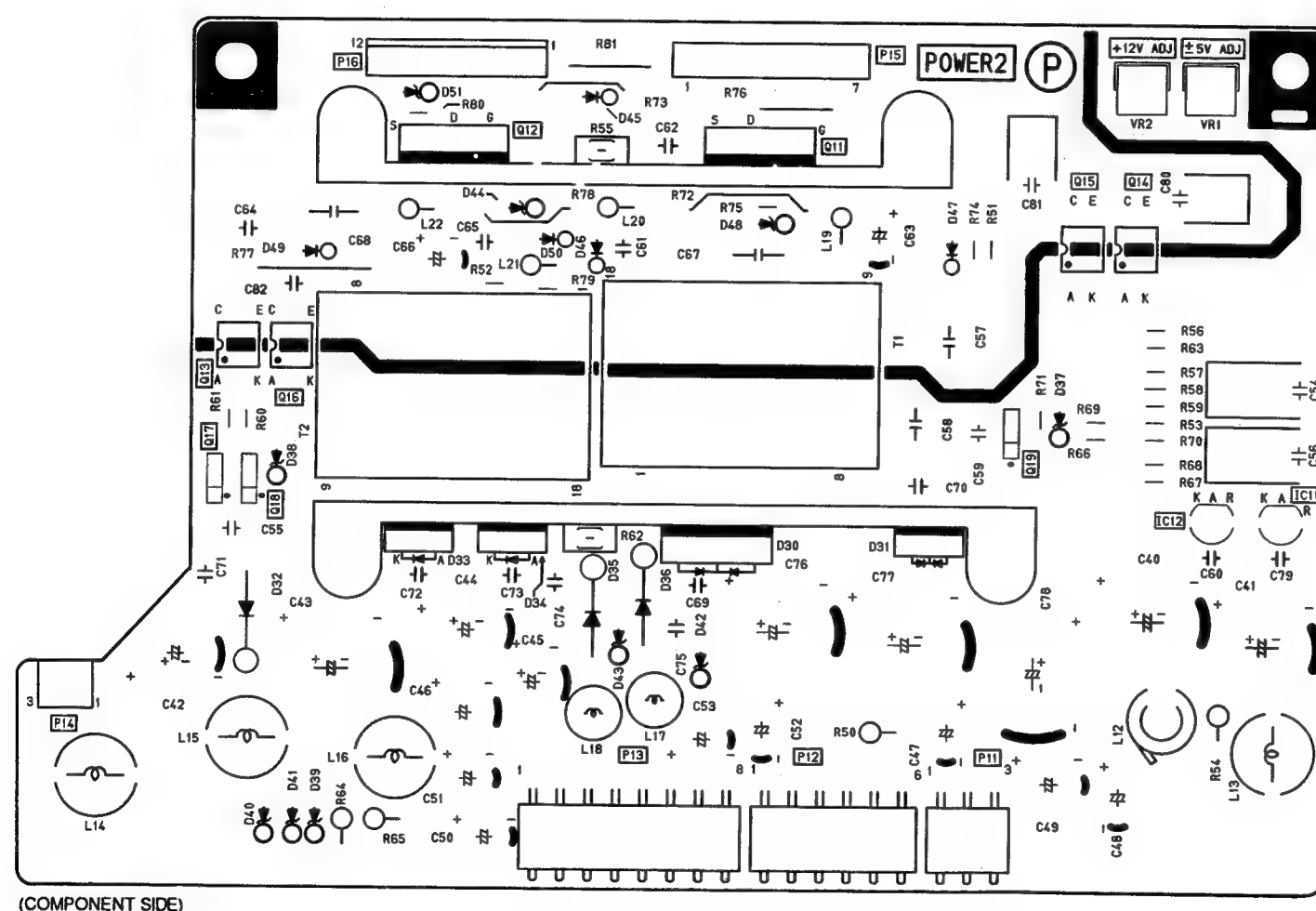
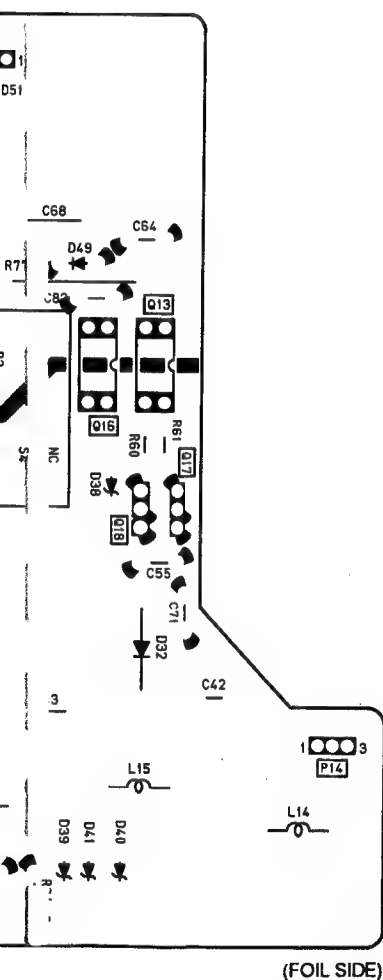
POWER 1	
Transistors	
Q2	B-6, B-1
Q3	B-7, B-1
Q4	A-7, A-1
Q5	A-7, A-1
Integrated Circuits	
IC1	B-7, B-1
IC2	B-7, B-1
IC3	B-6, B-1
Connectors	
P1	A-6, A-2
P3	A-5, A-3
P4	C-5, C-2
P5	C-6, C-1

ADDRESS INFORMATION



POWER 2 P.C. BOARD (VEP81075B)

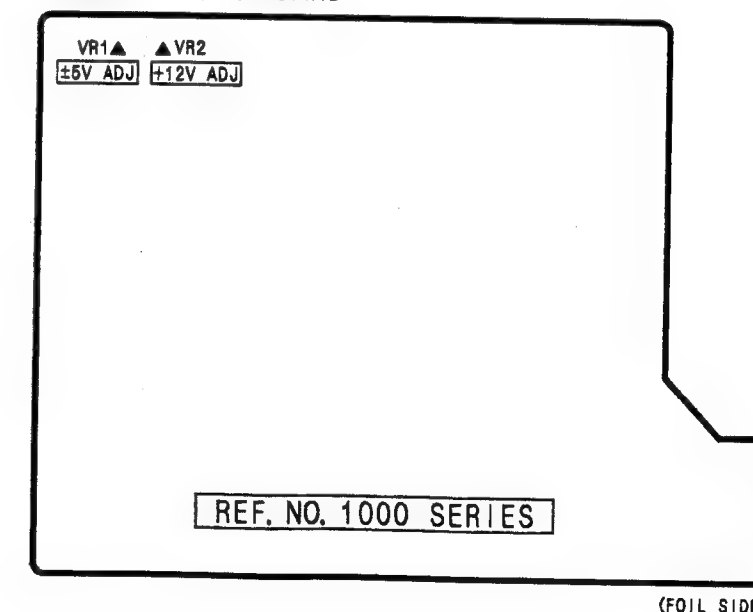




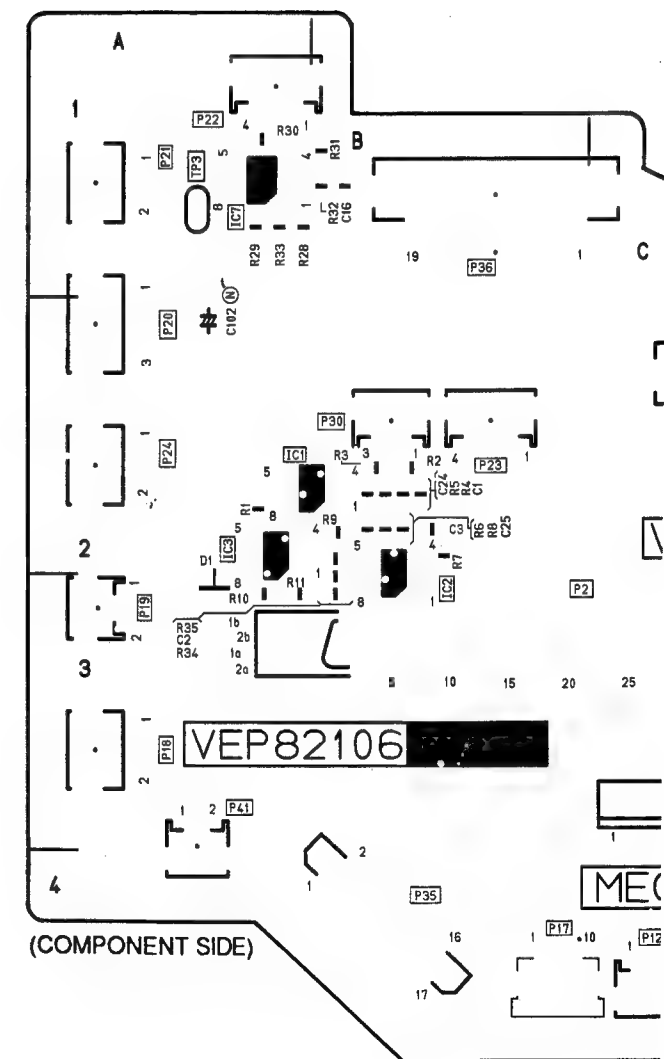
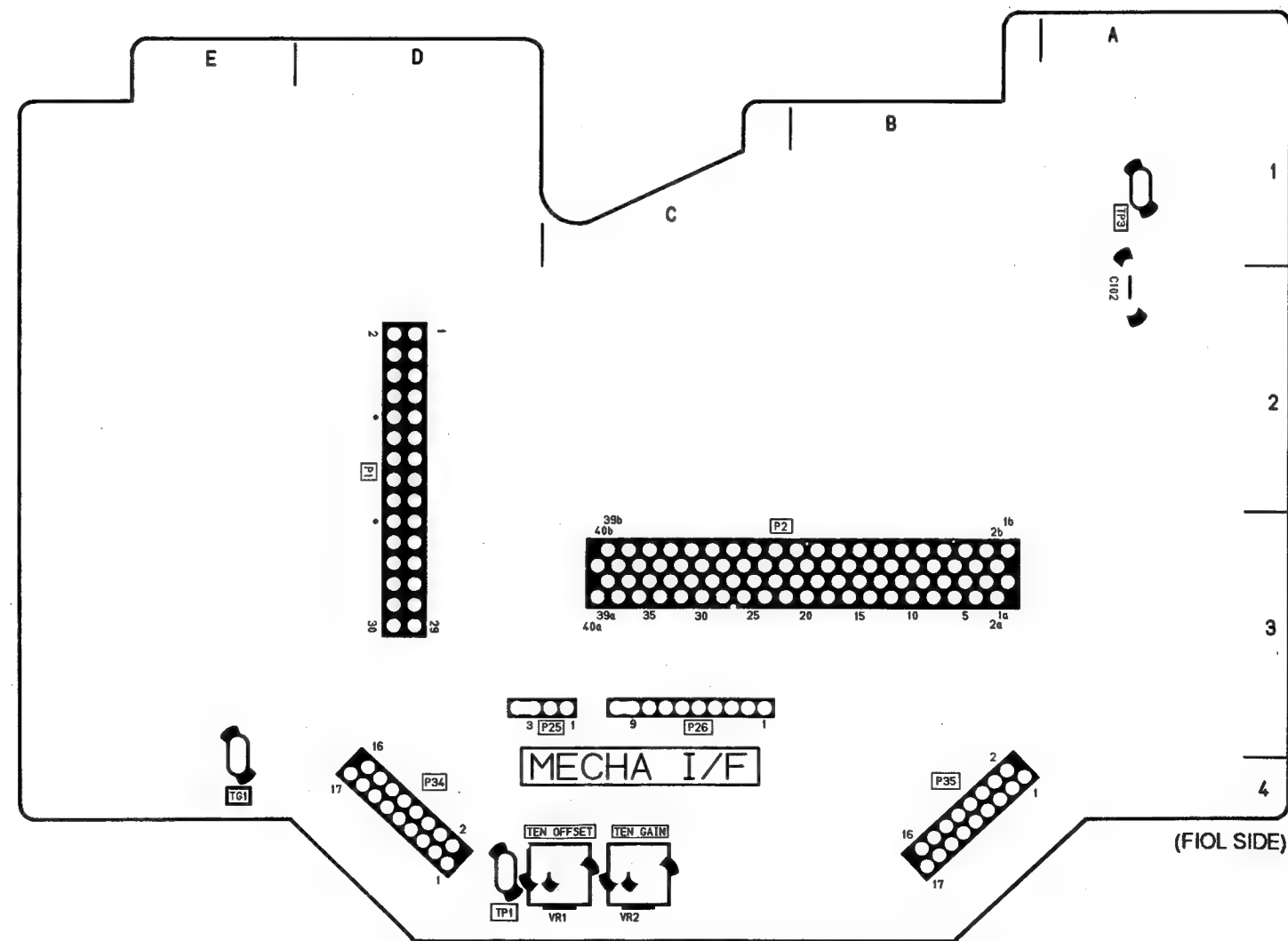
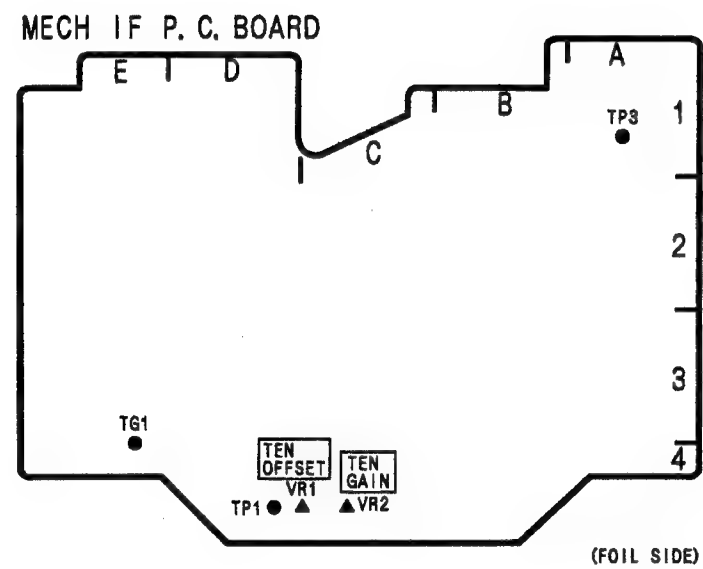
POWER 2	
Transistors	
Q11	C-7, C-2
Q12	C-6, C-3
Q13	B-5, B-3
Q14	C-8, B-1
Q15	C-7, B-1
Q16	B-5, B-3
Q18	B-5, B-3
Q19	B-7, B-1
Integrated Circuits	
IC11	B-8, B-1
IC12	B-8, B-1
Adjustments	
VR1	C-8, C-1
VR2	C-7, C-1
Connectors	
P11	A-7, A-2
P12	A-7, A-2
P13	A-6, A-2
P14	A-5, A-4

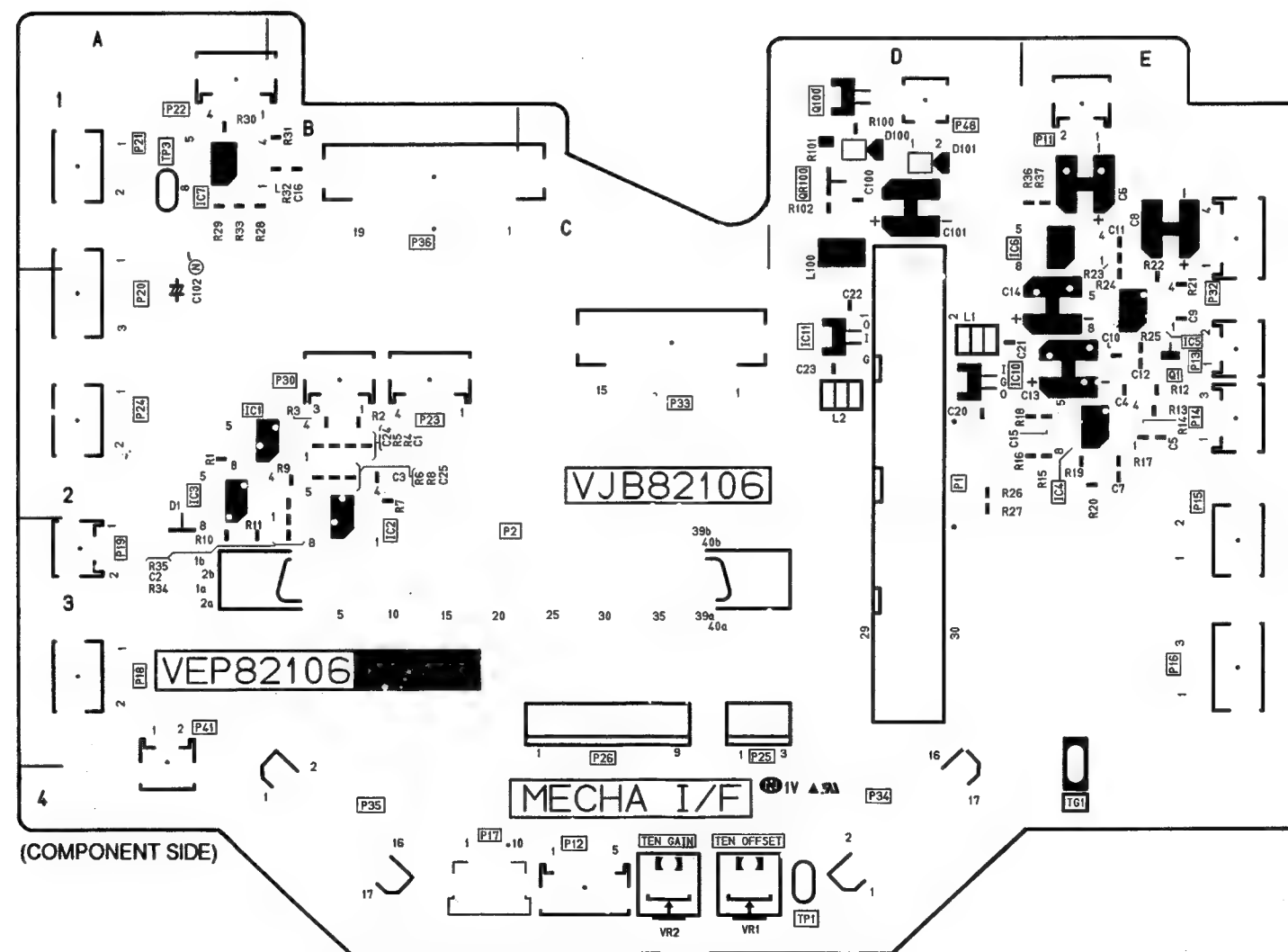
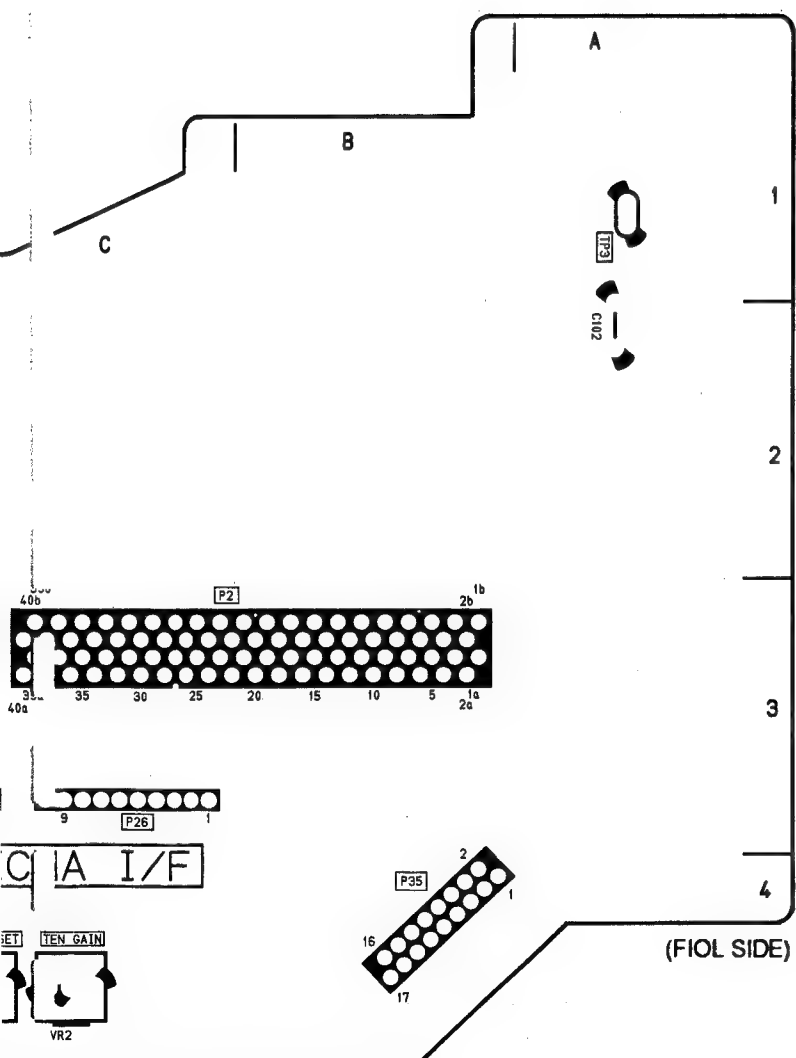
ADDRESS INFORMATION

POWER 2 P. C. BOARD



MECHA I/F P.C. BOARD (VEP82106A)

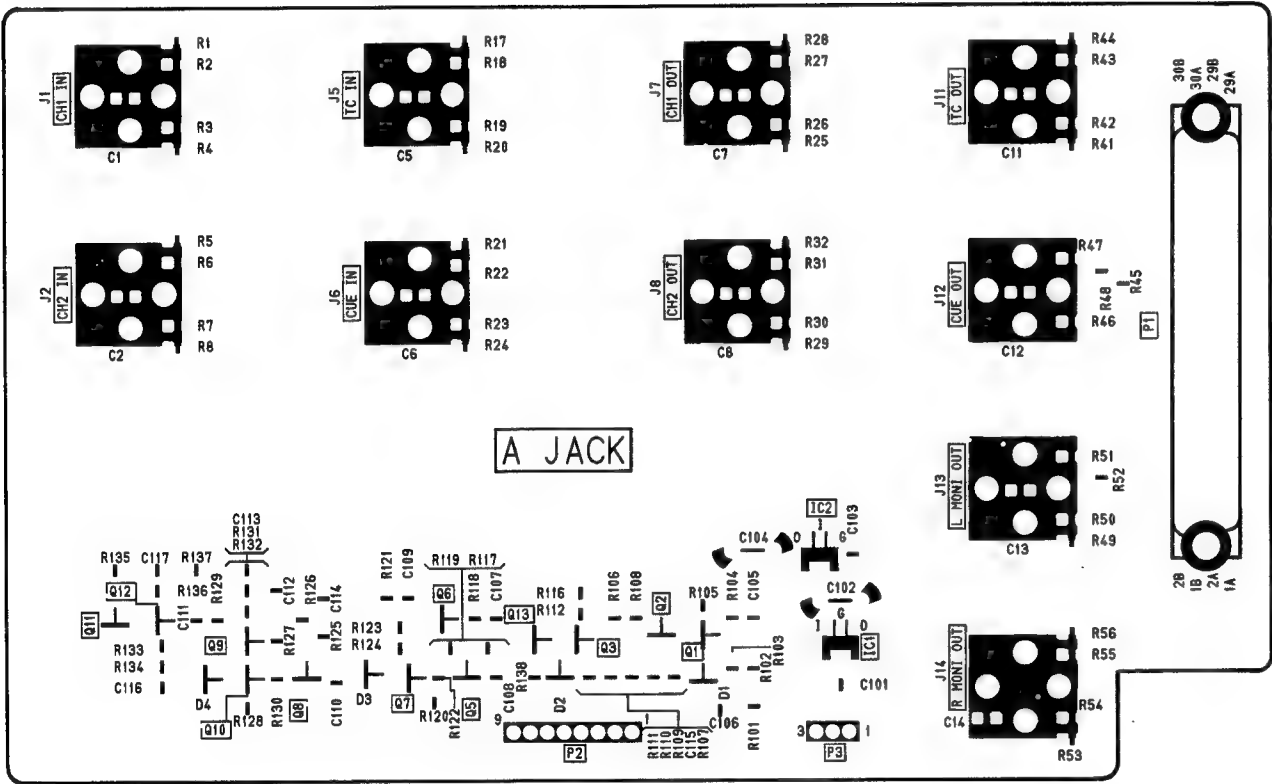




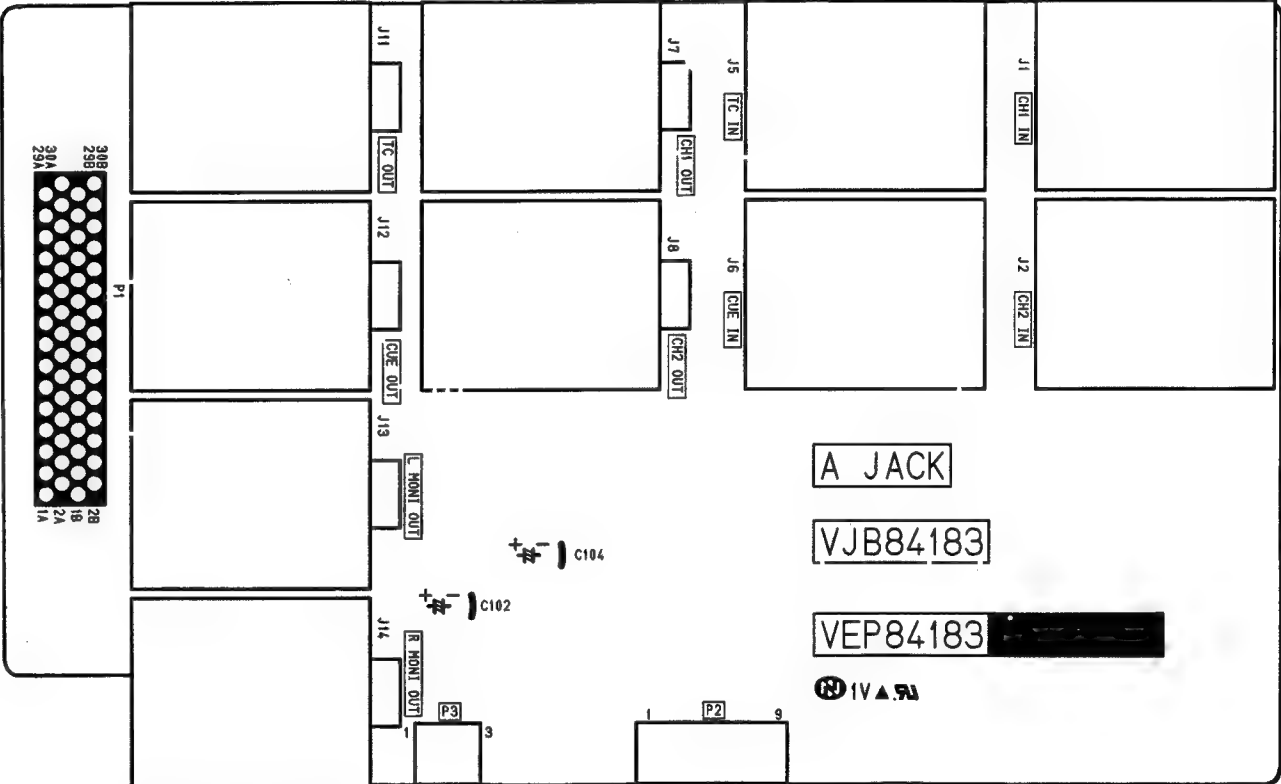
MECH I/F		
Transistors		
Q1	E-2	Ⓢ
Q100	D-1	Ⓢ
Transistor-Resistor		
QR100	D-1	Ⓢ
Integrated Circuits		
IC1	A-2	Ⓢ
IC2	B-2	Ⓢ
IC3	A-2	Ⓢ
IC4	E-2	Ⓢ
IC5	E-2	Ⓢ
IC6	D-1	Ⓢ
IC10	D-2	Ⓢ
IC11	D-2	Ⓢ
Test Points		
TP1	D-4	
TP3	A-1	
TG1	E-4	
Adjustment		
VR1	C-4	
VR2	C-4	
Connectors		
P1	D-2	
P2	C-3	
P11	E-1	Ⓢ
P12	C-4	Ⓢ
P13	E-2	Ⓢ
P14	E-2	Ⓢ
P15	E-2	Ⓢ
P16	E-3	Ⓢ
P17	B-4	Ⓢ
P18	A-3	Ⓢ
P19	A-3	Ⓢ
P20	A-2	
P21	A-1	
P22	A-1	
P23	B-2	Ⓢ
P24	A-2	Ⓢ
P25	C-3	
P26	C-3	
P30	B-2	
P32	E-1	Ⓢ
P33	C-2	Ⓢ
P34	D-4	
P35	B-4	
P36	B-1	Ⓢ
P41	A-3	Ⓢ
P48	D-1	Ⓢ

ADDRESS INFORMATION
 (C) ... COMPONENT SIDE
 (F) ... FOIL SIDE

A JACK P.C. BOARD (VEP84183A)

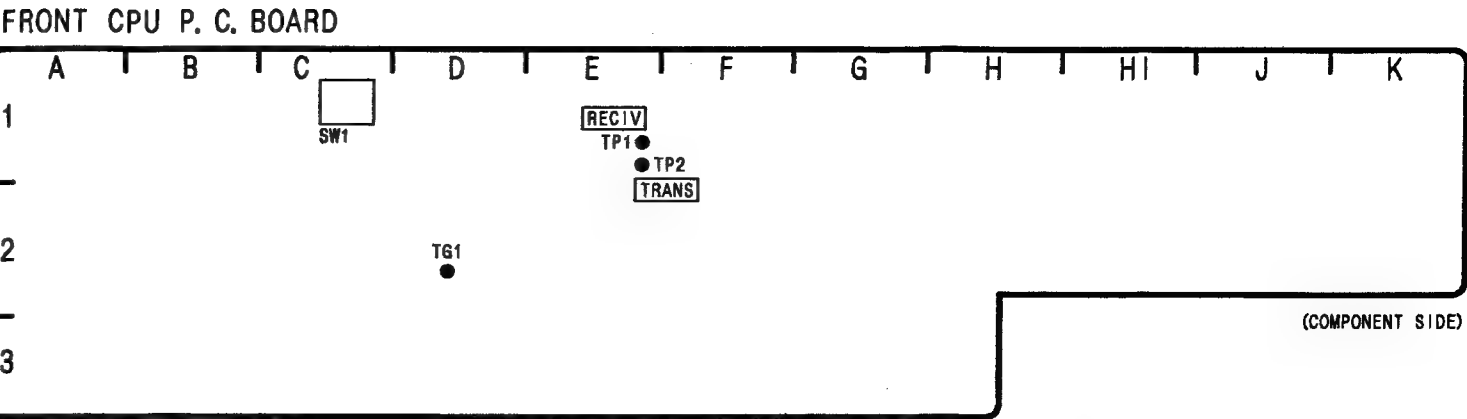
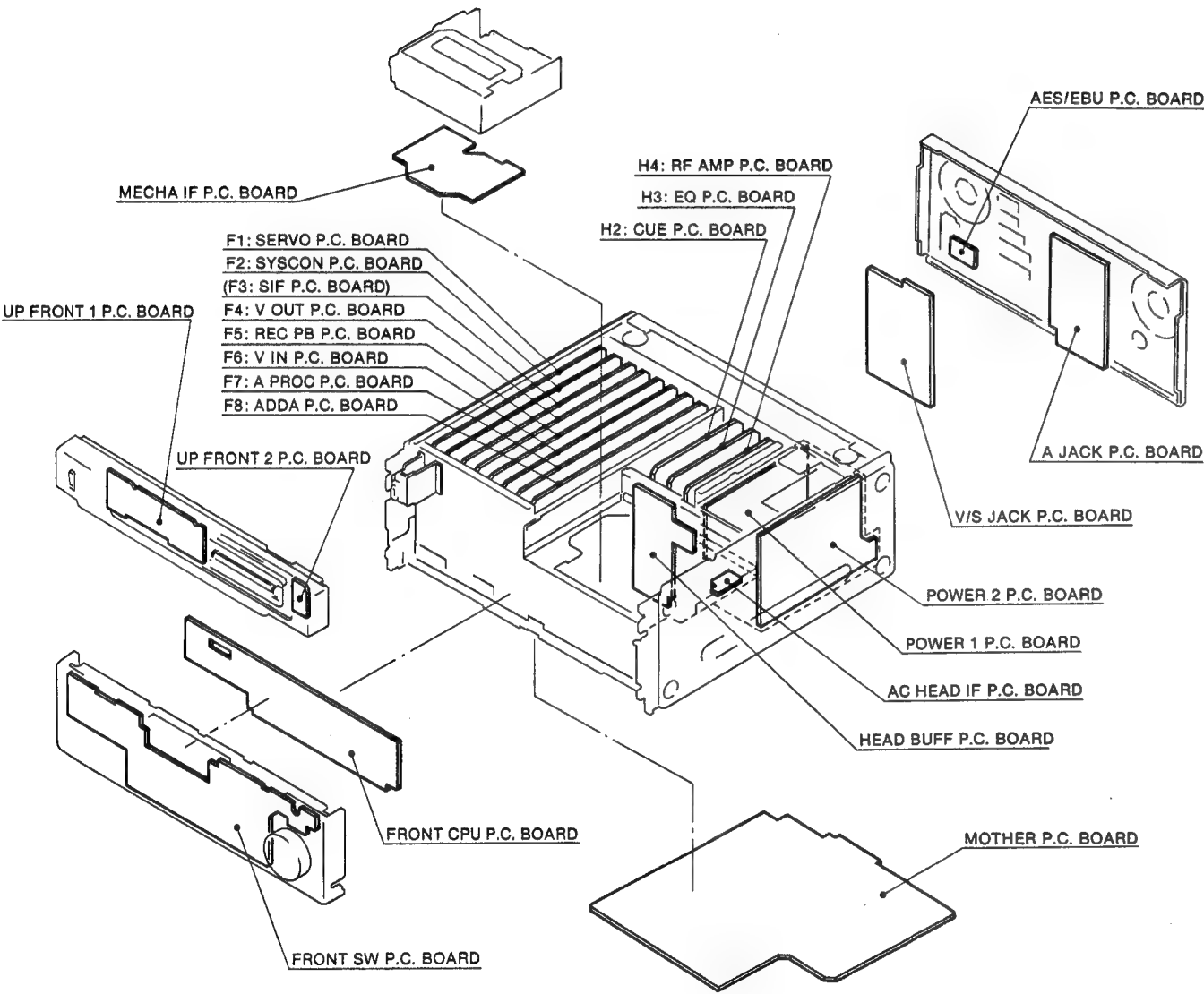


(FIOL SIDE)



(COMPONENT SIDE)

P.C. BOARD LOCATION



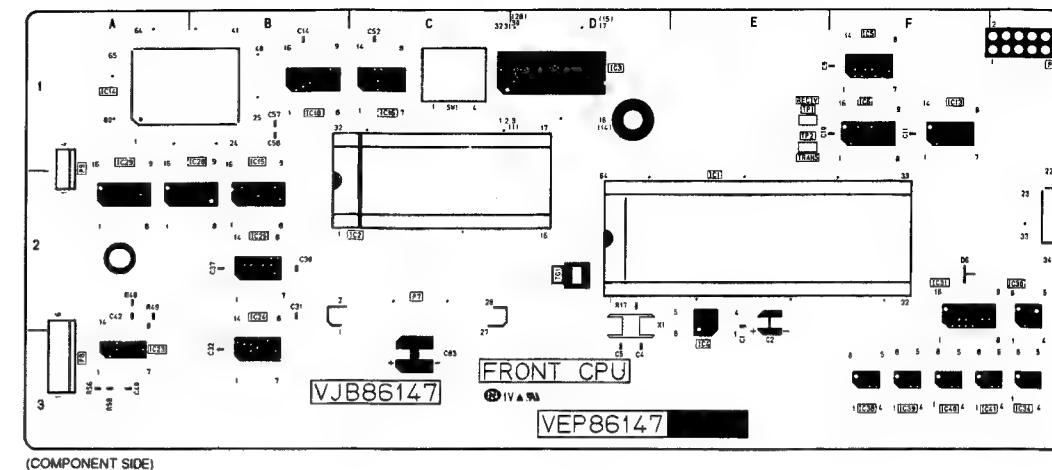
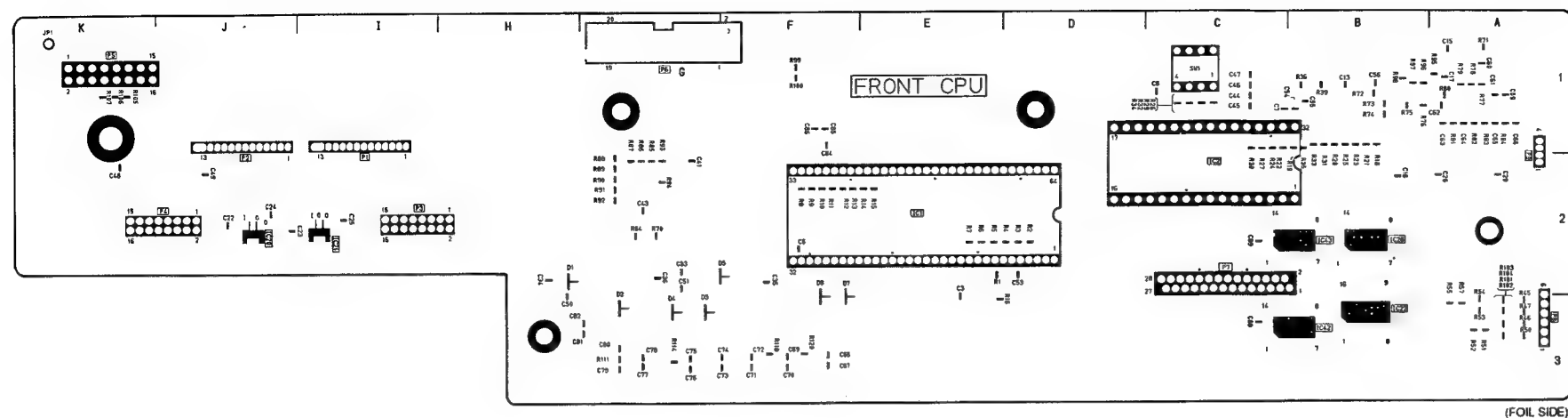
FRONT SW			
Transistors		IC5	
Q45	J-3	IC6	J-2
Q46	I-3	IC7	J-2
Q47	I-3	IC8	E-3
Transistor-Resistors		IC9	F-3
QR1	J-3	IC11	B-2
QR2	J-3	Switches	
QR3	I-3	SW1	K-3
QR4	J-2	SW2	I-3
QR5	J-3	SW3	I-3
QR6	I-3	SW4	K-2
QR7	K-1	SW5	J-2
QR8	I-2	SW6	I-2
QR9	M-1	SW7	K-1
QR10	M-1	SW8	I-2
QR11	L-1	SW9	K-2
QR12	K-2	SW10	J-2
QR13	J-2	SW11	F-3
QR14	F-3	SW12	E-3
QR15	E-3	SW13	F-3
QR16	F-3	SW14	H-3
QR17	M-1	SW15	H-3
QR18	L-1	SW16	G-3
QR19	L-1	SW18	E-2
QR20	J-2	SW20	F-2
QR21	I-2	SW21	G-2
QR22	J-1	SW22	G-2
QR23	I-1	SW23	H-2
QR24	H-3	SW24	H-2
QR26	G-3	SW25	G-3
QR27	E-2	SW26	H-3
QR28	E-2	SW27	H-1
QR29	E-2	SW28	J-1
QR30	F-2	SW29	J-1
QR31	F-2	SW30	I-1
QR32	E-3	SW31	I-1
QR33	F-2	SW32	H-1
QR34	F-2	SW34	H-2
QR35	F-3	SW36	G-2
QR36	G-2	SW37	G-2
QR37	G-2	SW38	G-2
QR38	G-2	SW39	A-1
QR39	H-3	SW40	A-1
Integrated Circuits		SW41	A-2
Connectors		Connectors	
IC1	D-2	P1	C-1
IC2	D-2	P2	B-1
IC3	D-2		
IC4	D-1		

ADDRESS INFORMATION
⊙ ... COMPONENT SIDE
⊗ ... FOIL SIDE

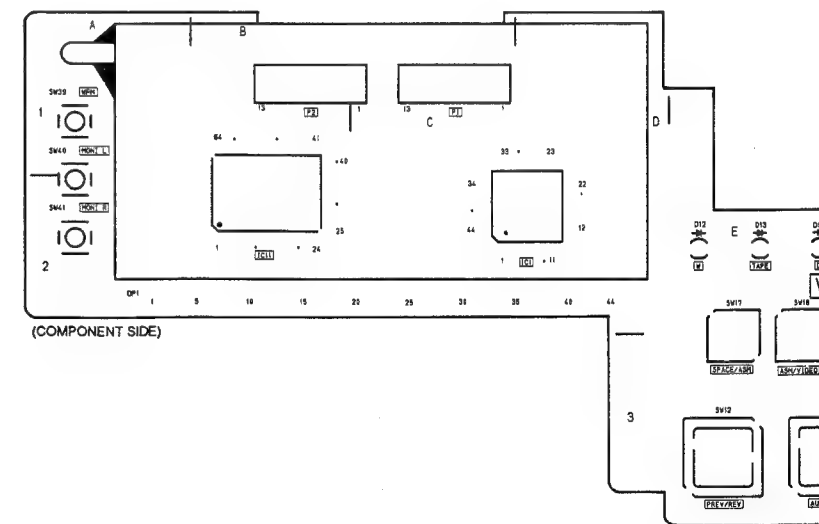
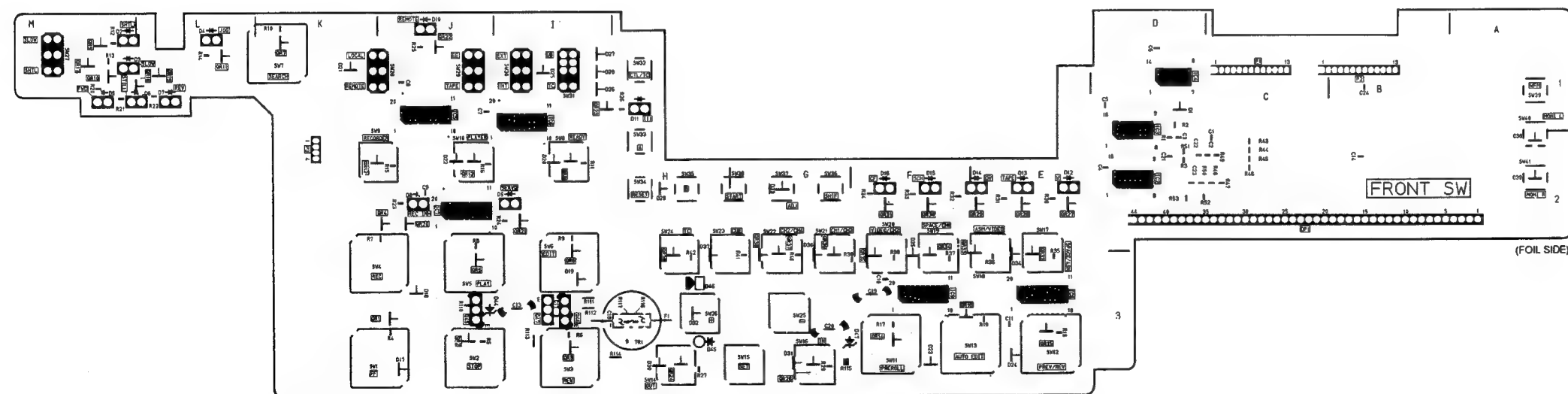
FRONT CPU	
Integrated Circuits	
IC1	E-2
IC2	C-2
IC3	D-1
IC4	E-3
IC5	F-1
IC6	F-1
IC13	F-1
IC14	A-1
IC15	B-1
IC16	C-1
IC17	H-1
IC18	B-1
IC20	J-2
IC21	I-2
IC22	B-3
IC23	A-3
IC24	B-2
IC25	B-2
IC26	B-2
IC27	G-1
IC28	B-1
IC29	A-1
IC30	G-2
IC31	F-2
IC32	H-2
IC33	G-2
IC34	G-3
IC35	G-3
IC36	G-3
IC37	H-3
IC38	F-3
IC39	F-3
IC40	F-3
IC41	G-3
IC42	B-3
IC43	B-2
Test Points	
TP1	E-1
TP2	E-1
TG1	D-2
Switch	
SW1	C-1
Connectors	
P1	I-1
P2	J-1
P3	I-2
P4	J-2
P5	K-1
P6	G-1
P7	C-2
P8	A-3

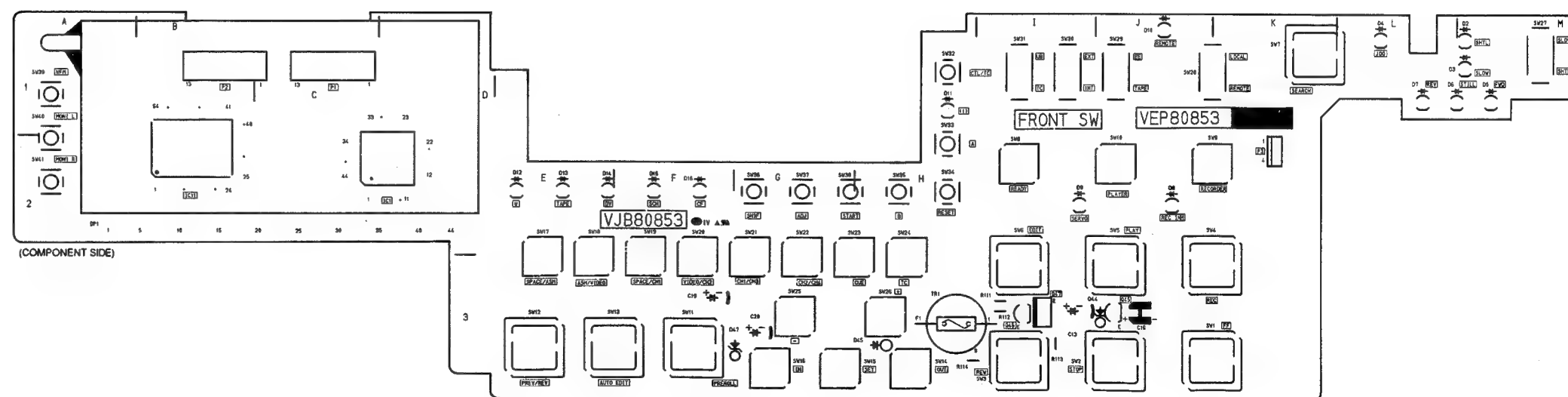
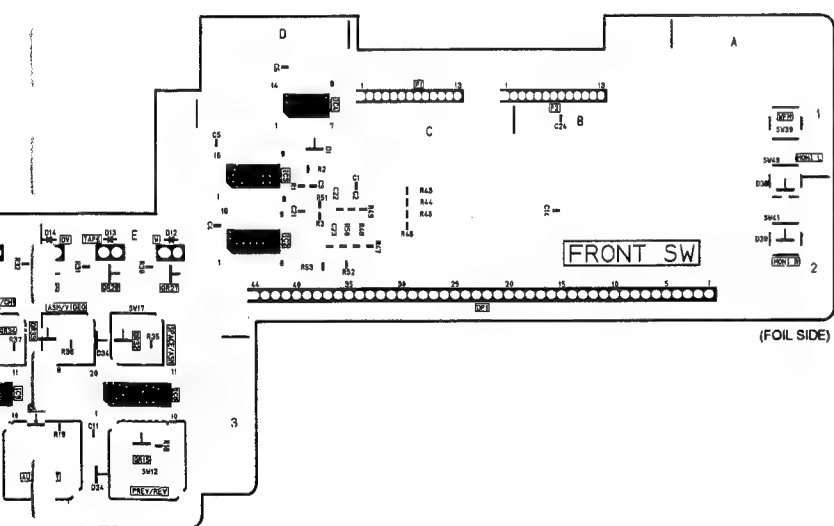
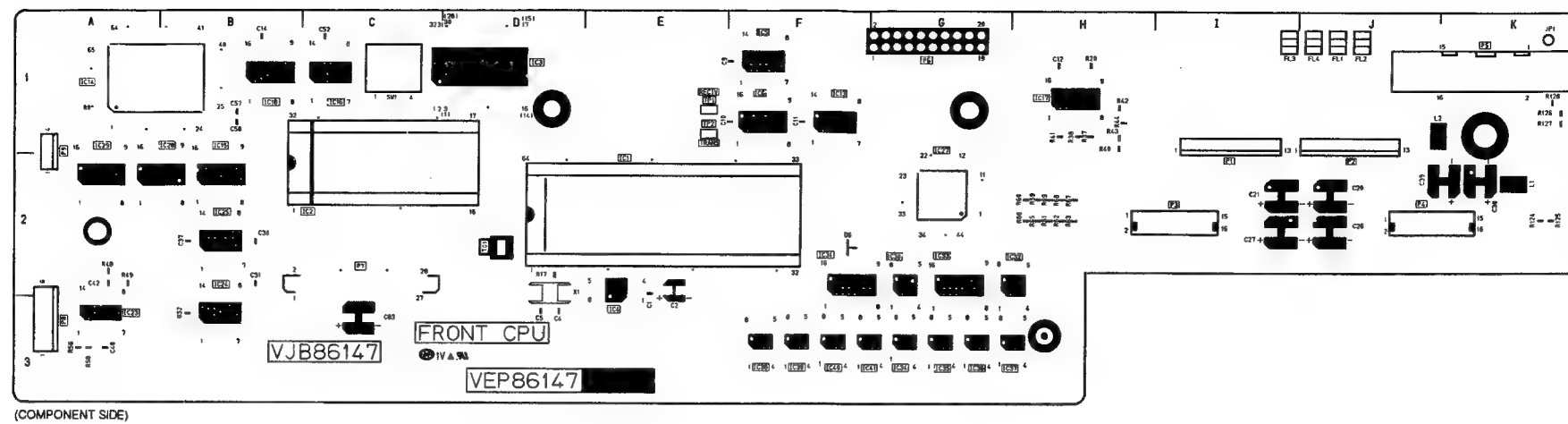
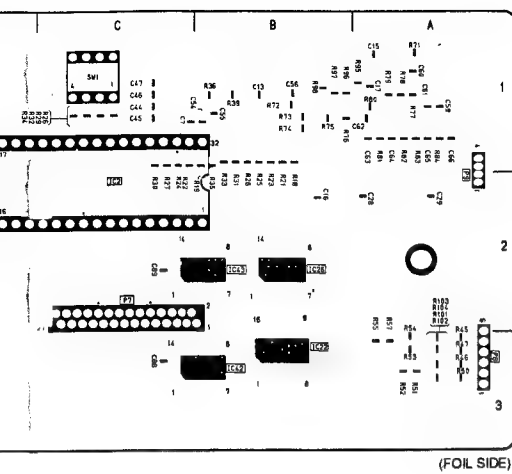
ADDRESS INFORMATION
⊙ ... COMPONENT SIDE
⊗ ... FOIL SIDE

FRONT CPU P.C. BOARD (VEP86147A)



FRONT SW P.C. BOARD (VEP80853A)

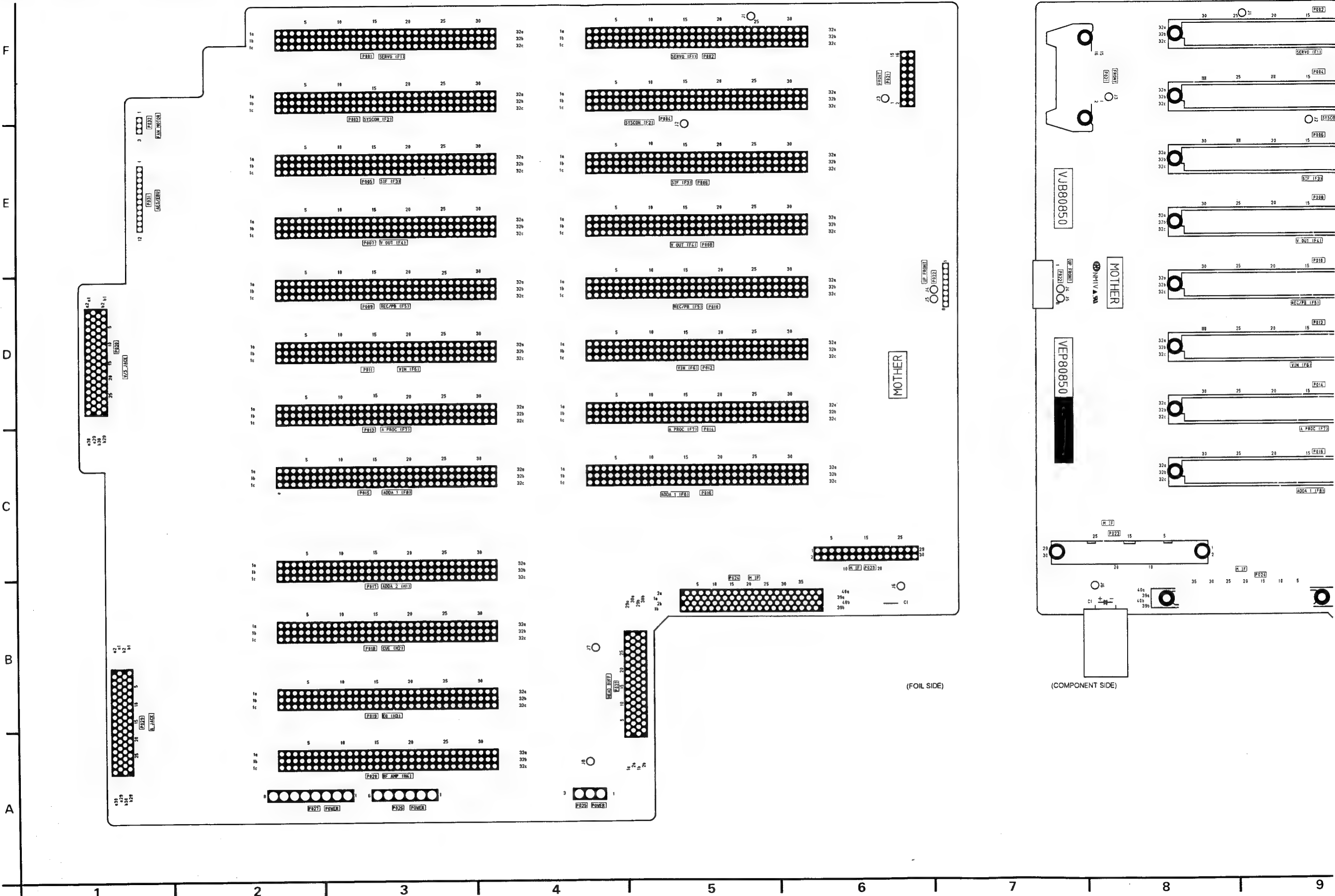




MOTHER P.C. BOARD (VEP80850A)

MOTHER	
Connectors	
P001	F-11, 3
P002	F-9, 5
P003	F-11, 3
P004	F-9, 5
P005	E-11, 3
P006	E-9, 5
P007	E-11, 3
P008	E-9, 5
P009	E-11, 3
P010	E-9, 5
P011	D-11, 3
P012	D-9, 5
P013	D-11, 3
P014	D-9, 5
P015	C-11, 3
P016	C-9, 5
P017	C-11, 3
P018	B-11, 3
P019	B-11, 3
P020	A-11, 3
P021	F-8, 6
P022	D-7, 6
P023	C-8, 6
P024	B-9, 5
P025	A-10, 4
P026	A-11, 3
P027	A-12, 2
P029	B-13, 1
P030	D-13, 1
P031	E-12, 1
P032	E-12, 1
P033	B-9, 4

ADDRESS INFORMATION
⊙... COMPONENT SIDE
⊙... FOIL SIDE



SECTION 4

IC INFORMATION

ICs INFORMATION

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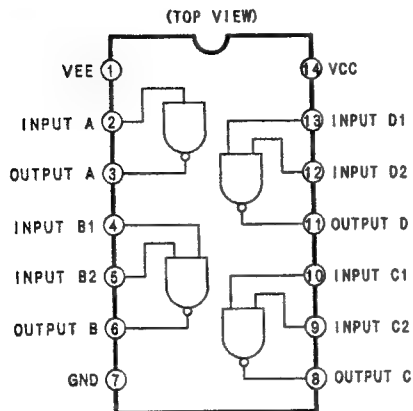
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NJM386M	NJM386	46	TC4S30F	TC4S30F	56
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NJU7112AM			TC7S04FU	TC7S04F	56
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S80727ANDQ	S80700AN	48	TC7S32FU	TC7S32F	57
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S8420BF			TC7S66F	TC7S66F	57
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TMS320C25PHL		
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UPC1663G	UPC1663	61
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UPC317H		
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UPC4082G2	UPC4082	63
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UPC5022GA089		
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UPC5102GS030		
UPD16310GF	UPD16310GF	64
UPD16510GR		
UPD42101G-3	UPD42101G	63
UPD42102G-3	UPD42102G	63
UPD42280G3	UPD42280	65
UPD6456T611Y	UPD6456	66
UPD6486GF3BA	UPD6486GF	67
UPD65013BC16		
UPD65650J203		
UPD65845G039	UPD65845G039	68
UPD65868D022	UPD65868D022	69
UPD71055GB	UPD71055G	71
UPD75316BE58		
UPD75328G742		
UPD75P328		
VSI1997		
VSI2000		
VY06632		
VY06633		
XC62AP2302P	X62APXX02M	72
XC62AP3002ML	X62APXX02M	72
XC62AP3002P	X62APXX02M	72
XC62AP3002PL	X62APXX02M	72
XC62AP3202P		
XC62AP5002ML	X62APXX02M	72
XC62AP5002P	X62APXX02M	72
XC62DN3002ML	X62DNXX02M	72
XC62DN5002P	X62DNXX02M	72

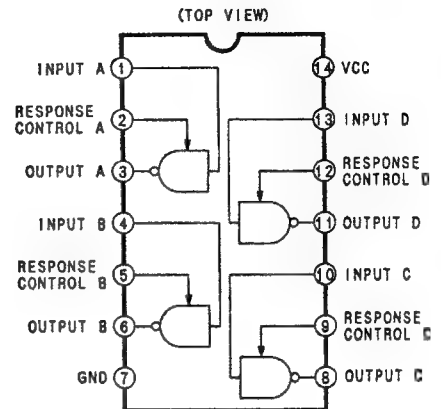
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Y7C19935VC	Y7C19935VC	72
Z84C4310FEC		

NOTE: The following ICs which are not described on the REF. PAGE, are not contained the IC Block drawing in this issue.

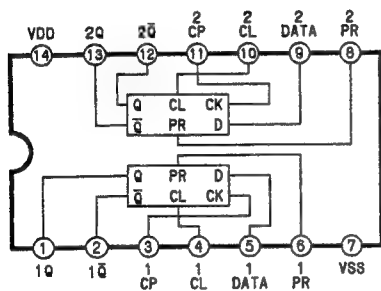
1488
(QUAD LINE (RS232C) DRIVER)



1489
(QUAD LINE (RS232C) RECEIVER)



4013
(DUAL D-TYPE FLIP-FLOP)

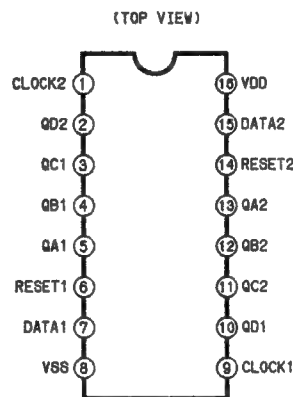


TRUTH TABLE

INPUTS				OUTPUTS	
CLOCK [†]	DATA	RESET	SET	Q	\bar{Q}
0	0	0	0	0	1
1	0	0	0	1	0
0	x	0	0	Q	\bar{Q}
x	x	1	0	0	1
x	x	0	1	1	0
x	x	1	1	1	1

x=DON'T CARE
†=LEVEL CHANGE

4015
(DUAL 4-STAGE SHIFT REGISTER)

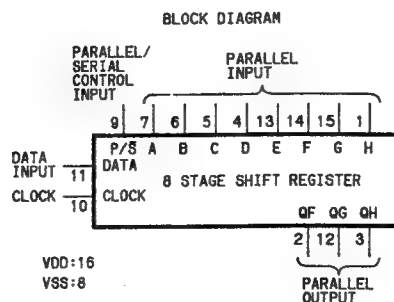
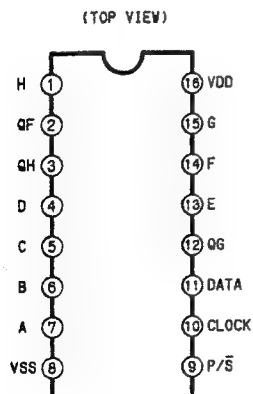


TRUTH TABLE

CL [▲]	D	R	Q1	QN
0	0	0	0	QN-1
1	0	1	1	QN-1
x	x	0	Q1	QN (NO CHANGE)
x	x	1	0	0

▲ LEVEL CHANGE
x DON'T CARE CASE

4021
(8-STAGE STATIC SHIFT REGISTER)

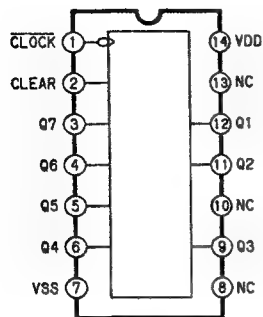


TRUTH TABLE

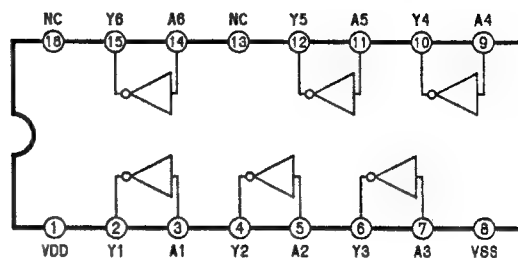
CL [▲]	SERIAL INPUT	PARALLEL/SERIAL CONTROL	PL-1	PL-N (INTERNAL)	Q1	QN
x	x	1	0	0	0	0
x	x	1	0	1	0	1
x	x	1	1	1	1	1
0	0	0	x	x	0	QN-1
1	0	0	x	x	1	QN-1
x	x	0	x	x	Q1	QN

▲-LEVEL CHANGE x-DON'T CARE CASE

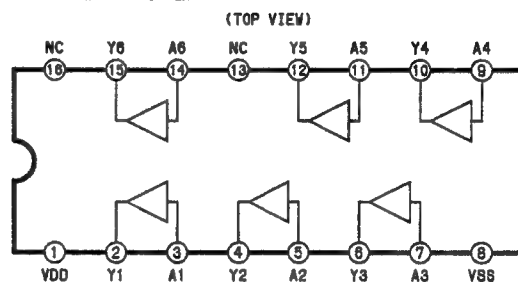
4024
(7-STAGE BINARY RIPPLE COUNTER)
(TOP VIEW)



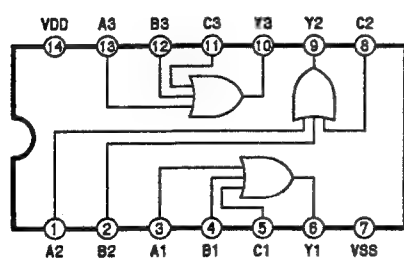
4049
(HEX. INVERTING BUFFER/CONVERTER)
(TOP VIEW)



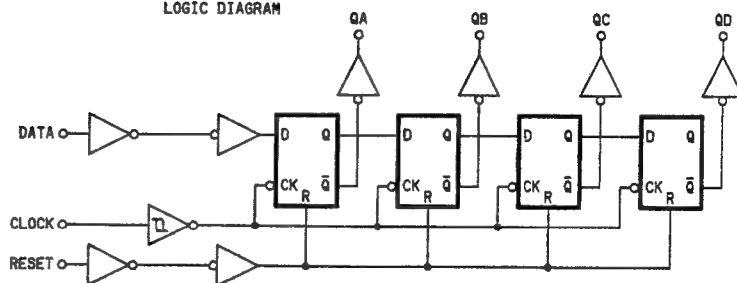
4050
(HEX. BUFFER/CONVERTER)
(TOP VIEW)



4075
(TRIPLE 3-INPUT OR GATE)
(TOP VIEW)



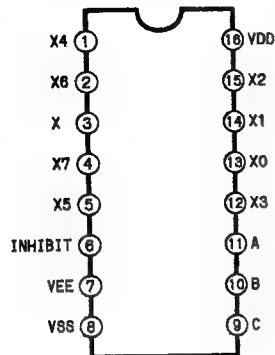
LOGIC DIAGRAM



4051

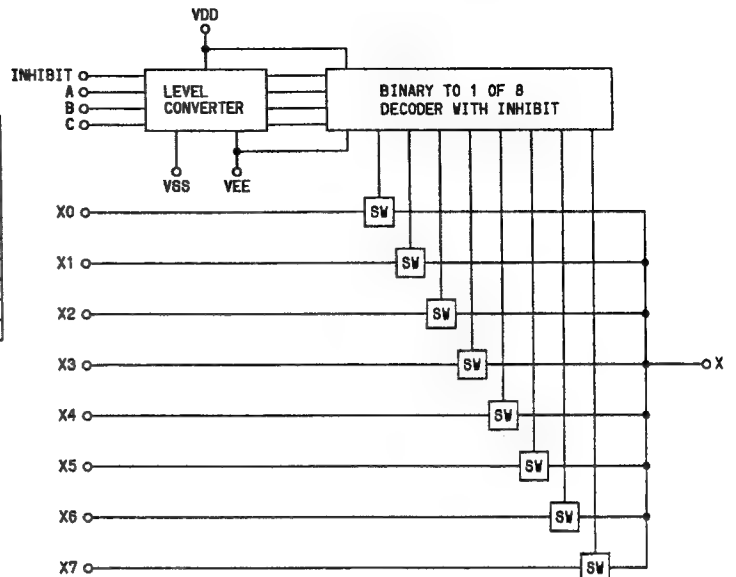
(SINGLE 8-CHANNEL
MULTIPLEXER/DEMULTIPLEXER)

(TOP VIEW)



TRUTH TABLE

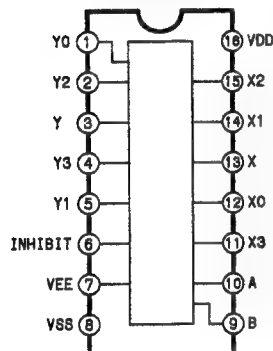
INPUT STATES				"ON" CHANNEL (S)
INHIBIT	C	B	A	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	NONE



4052

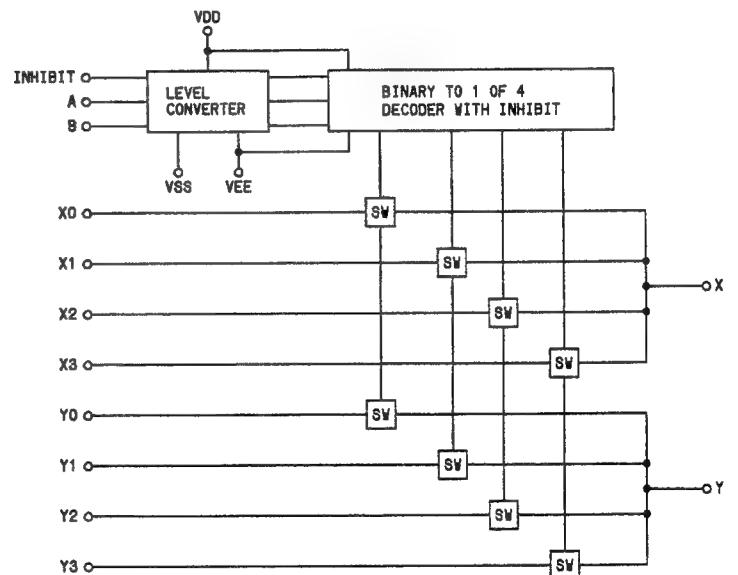
(DIFFERENTIAL 4-CHANNEL
MULTIPLEXER/DEMULTIPLEXER)

(TOP VIEW)



TRUTH TABLE

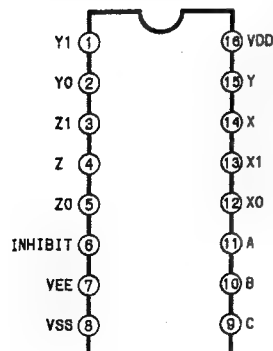
INPUT STATES				"ON" CHANNEL (S)
INHIBIT	B	A		
0	0	0	0	X0, Y0
0	0	1	0	X1, Y1
0	1	0	0	X2, Y2
0	1	1	0	X3, Y3
1	X	X	X	NONE



4053

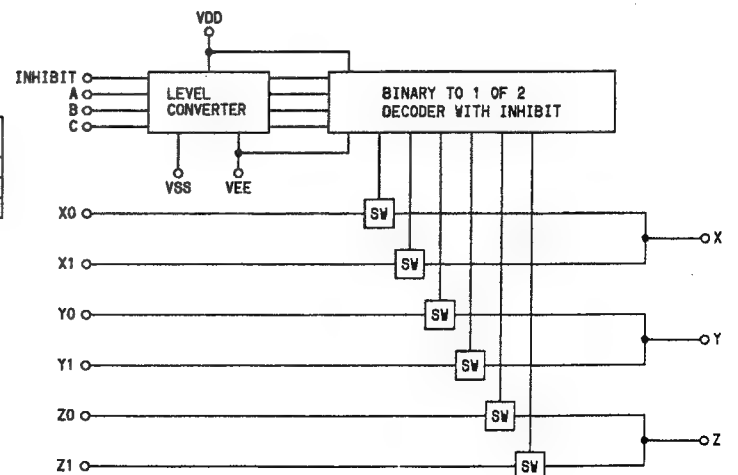
(TRIPLE 2-CHANNEL
MULTIPLEXER/DEMULTIPLEXER)

(TOP VIEW)



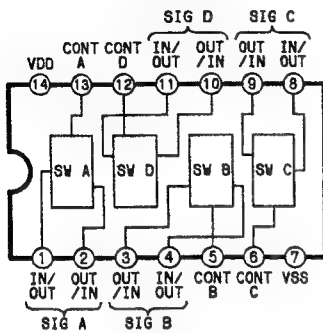
TRUTH TABLE

INPUT STATES				"ON" CHANNEL (S)
INHIBIT	C	B	A	
0	0	0	0	X0, Y0, Z0
0	0	0	1	X1, Y1, Z1
1	X	X	X	NONE



4066

(QUAD BILATERAL SWITCH)
(TOP VIEW)

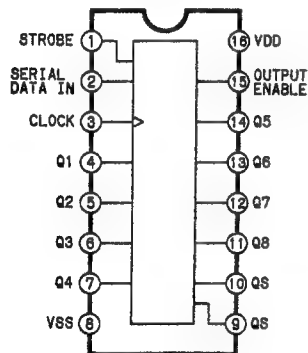


TRUTH TABLE

CONTROL	SWITCH
H	ON
L	OFF

4094

(8-STAGE SHIFT/STORE BUS REGISTER)
(TOP VIEW)



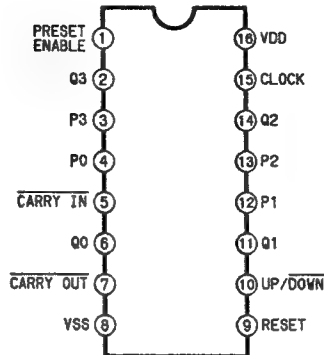
TRUTH TABLE

CL ▲	OUTPUT ENABLE	STROBE	DATA	PARALLEL OUTPUTS		SERIAL OUTPUTS	
				Q1	Q2	Q3	Q4
0	0	x	x	OC	OC	Q7	NC
0	x	x	x	OC	OC	NC	Q7
1	0	x	x	NC	NC	Q7	NC
1	1	0	0	Q1	Q2	Q7	NC
1	1	1	1	Q1	Q2	Q7	NC
1	1	1	1	NC	NC	NC	Q7

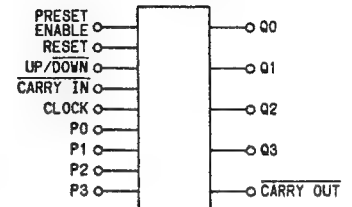
▲-LEVEL CHANGE x-DON'T CARE CASE

4516

(4-BIT UP/DOWN BINARY COUNTER)
(TOP VIEW)



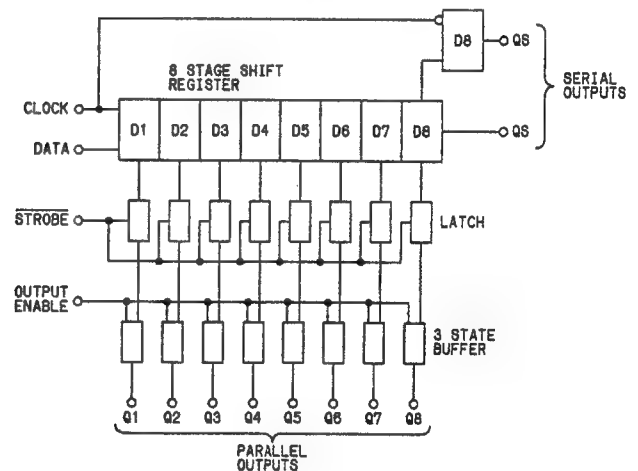
BLOCK DIAGRAM



TRUTH TABLE

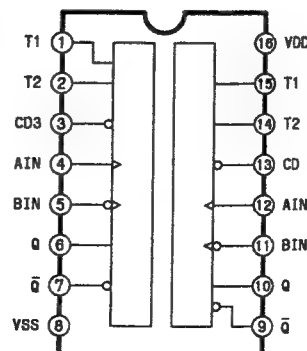
CARRY IN	UP/DOWN	PRESET ENABLE	RESET	ACTION
H	x	L	L	NO COUNT
L	H	L	L	COUNT UP
L	L	L	L	COUNT DOWN
x	x	H	L	PRESET
x	x	x	H	RESET

BLOCK DIAGRAM



4538

(DUAL PRECISION
MONOSTABLE MULTIVIBRATOR)
(TOP VIEW)

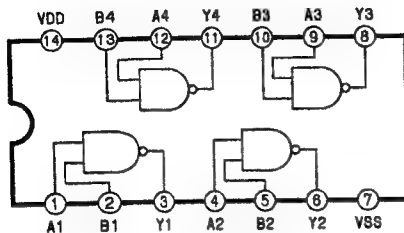


TRUTH TABLE

INPUT			OUTPUT	
A	B	CD	Q	Q̄
0	0	0	0	1
0	0	1	1	0
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	1	0

7400
(QUAD 2-INPUT NAND GATE)

(TOP VIEW)

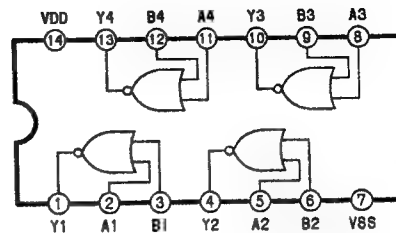


TRUTH TABLE (74HC)

INPUTS		OUTPUTS
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

7402
(QUAD 2-INPUT NOR GATE)

(TOP VIEW)

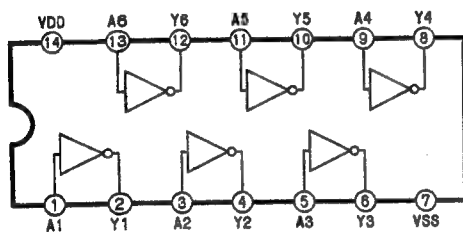


TRUTH TABLE

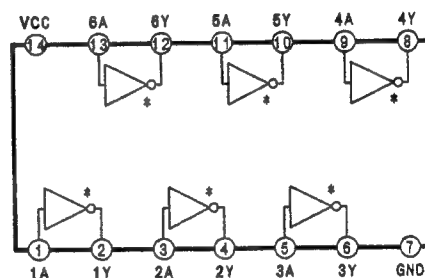
INPUTS		OUTPUTS
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

7404
(HEX. INVERTER)

(TOP VIEW)

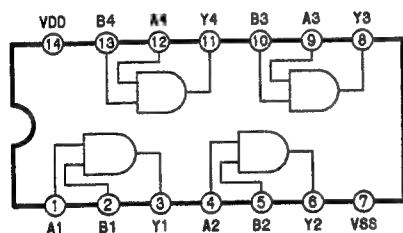


7405
(HEX O. C. INVERTER)



7408
(QUAD 2-INPUT AND GATE)

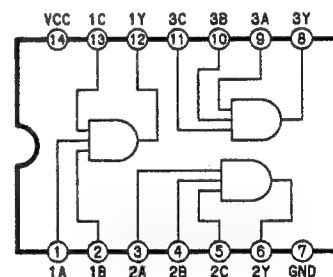
(TOP VIEW)



TRUTH TABLE

INPUTS		OUTPUTS
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

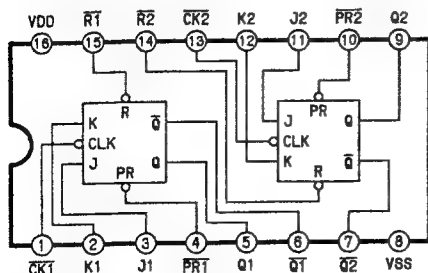
7411
(TRIPLE 3-INPUT AND GATE)



Y=A.B.C

74112
(DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR)

(TOP VIEW)



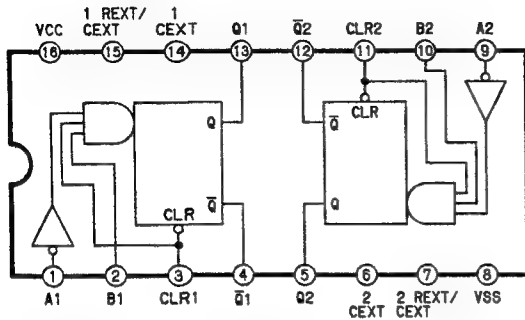
CLK: CLOCK
PR: PRESET
R: RESET

TRUTH TABLE (74HC112)

INPUTS					OUTPUTS	
PR	CLR	CLK	J	L	Q	Q̄
L	H	x	x	x	H	L
H	L	x	x	x	L	H
L	L	x	x	x	L*	L*
H	H	↓	L	L	Q0	Q0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	TOGGLE
H	H	H	x	x	Q0	Q0

■ : UNSTABLE

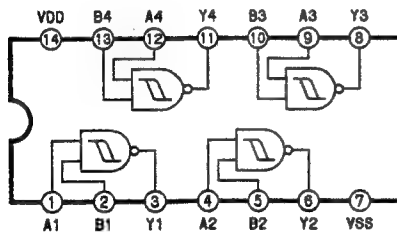
74123
(DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR)
(TOP VIEW)



TRUTH TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	Q̄
L	x	x	L	H
x	H	x	L	H
x	x	L	L	H
H	L	↑	L	↑
H	↓	H	↑	↑
↑	L	H	↑	↑

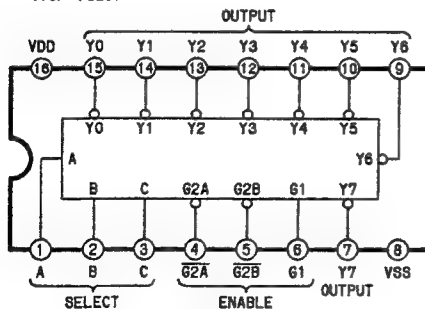
74132
(QUAD 2-INPUT NAND SCHMITT TRIGGER)
(TOP VIEW)



TRUTH TABLE

INPUTS		OUTPUTS
A	B	Y
0	0	1
1	0	1
0	1	1
1	1	0

74138
(3-TO-8 LINE DECODER)
(TOP VIEW)

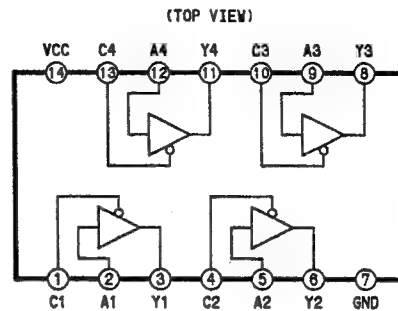


TRUTH TABLE (74HC138)

INPUTS				OUTPUTS							
ENABLE	SELECT			Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
G1	G2	C	B	A							
x	H	x	x	x	H	H	H	H	H	H	H
L	x	x	x	x	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	L	H
H	L	L	L	H	H	H	H	H	H	H	L

* G2=G2A+G2B

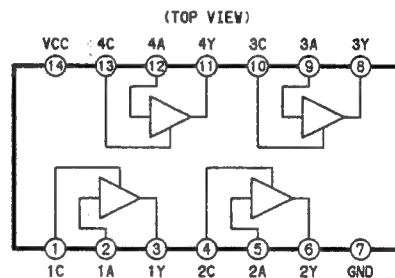
74125
(3 STATE QUAD BUFFER)
(TOP VIEW)



TRUTH TABLE

INPUTS		OUTPUT
A	C	Y
H	L	H
L	L	L
X	H	Z

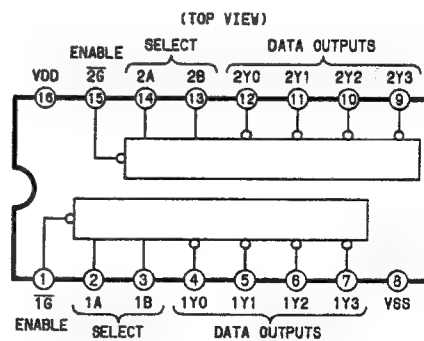
74126
(QUAD 3 STATE BUS BUFFERS)
(TOP VIEW)



TRUTH TABLE

INPUTS		OUTPUTS
A	C	Y
H	H	H
L	H	L
X	L	Z

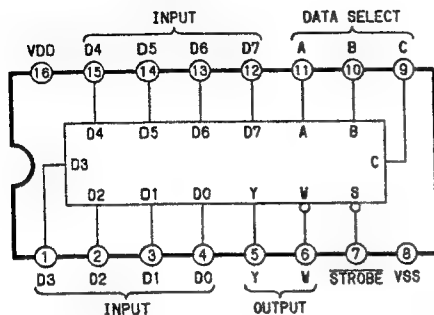
74139
(DUAL 2-TO-4 LINE DECODER)
(TOP VIEW)



TRUTH TABLE

INPUTS			OUTPUTS			
ENABLE	SELECT		Y0	Y1	Y2	Y3
G	B	A				
H	x	x	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

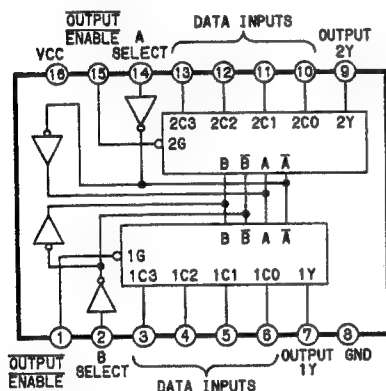
74151
(8-CHANNEL DIGITAL MULTIPLEXER)
(TOP VIEW)



TRUTH TABLE

INPUTS				OUTPUTS	
SELECT	STROBE			Y	W
C B A	S				
X X X	H			L	H
L L L	L			D0	D0
L L H	L			D1	D1
L H L	L			D2	D2
L H H	L			D3	D3
H L L	L			D4	D4
H L H	L			D5	D5
H H L	L			D6	D6
H H H	L			D7	D7

74153
(DUAL 4 TO 1 DATA SELECTORS)
(TOP VIEW)

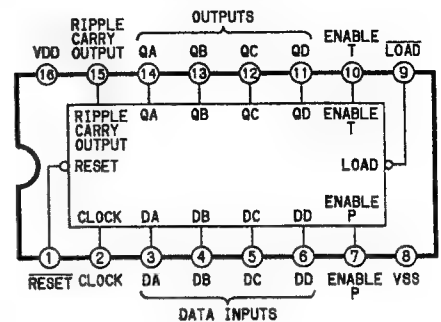


TRUTH TABLE

INPUT		OUTPUT	
SELECT	OUTPUT	ENABLE	Y
B A			
X X	H	L	L
L L	L	C0	
L H	L	C1	
H L	L	C2	
H H	L	C3	

H:HIGH L:LOW X:H or L

74161
(4-BIT SYNCHRONOUS BINARY COUNTER)
(TOP VIEW)



TRUTH TABLE (74HC160/74HC161)

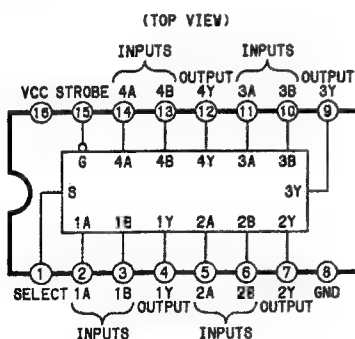
INPUT					OUTPUT
CLOCK	RESET	LOAD	ENABLE P	ENABLE T	Qn
X	L	X	X	X	L
	H	L	X	X	LOAD
	H	H	H	H	COUNT
X	H	H	L	X	NO COUNT
X	H	H	X	L	NO COUNT

H:HIGH L:LOW X:H or L
n:A~D

FUNCTION TABLE (74161)

INPUT				OUTPUT				FUNCTION
CLEAR	LOAD	CK	ENABLE P T	QA QB QC QD	RIPPLE CARRY			
H	H		H H	—	—			COUNT
H	L		X X	DA DB DC DD	—			DATA SET
	X	X	X X	L L L L	—			CLEAR
H	X	X	X H	H H H H	H			

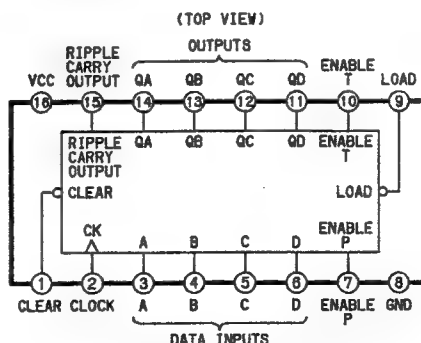
74157, 74158
(QUAD 2-INPUT MULTIPLEXER)
(TOP VIEW)



TRUTH TABLE (74HC157)

INPUTS		OUTPUT Y	
STROBE	SELECT	A B	HC157 HC158
H	X	X X	L
L	L	L X	L
L	L	H X	H
L	H	X L	L
L	H	X H	H

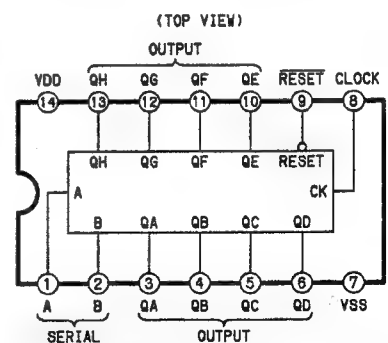
74163
(4-BIT SYNCHRONOUS BINARY COUNTER WITH SYNCHRONOUS CLEAR)
(TOP VIEW)



TRUTH TABLE

CLK	CLR	ENP	ENT	LOAD	FUNCTION
↑	L	X	X	X	CLEAR
X	H	H	L	H	COUNT & RC DISABLED
X	H	L	H	H	COUNT DISABLED
X	H	L	L	H	COUNT & RC DISABLED
↑	X	H	X	L	LOAD
↑	H	H	H	H	INCREMENT COUNTER

74164
(8-BIT SERIAL-IN/PARALLEL-OUT SHIFT REGISTER)
(TOP VIEW)



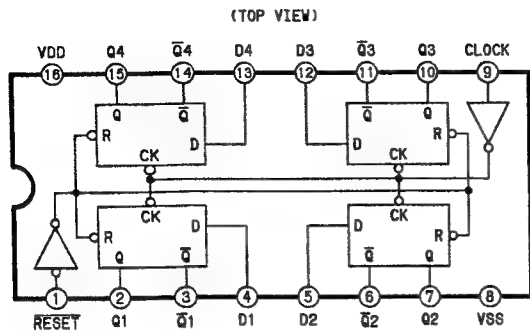
TRUTH TABLE (74HC164)

INPUT		OUTPUT		
RESET	CLOCK	A B	QA QB QH	
L	X	X X	L L L	
H		X X	NO CHANGE	
H	↑	L X	L QA QG	
H	↑	X L	L QA QG	
H	↑	H H	H QA QG	

H:HIGH L:LOW X:H or L

74175

(QUAD D-TYPE FLIP-FLOP WITH CLEAR)



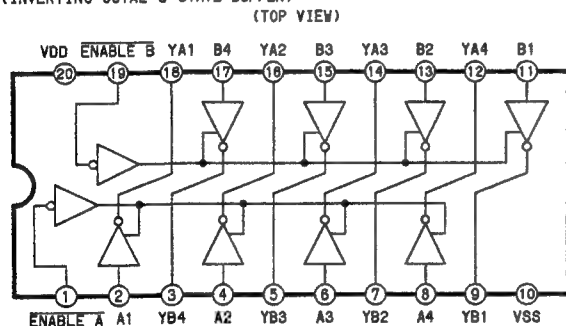
TRUTH TABLE (74HC175)

INPUT		OUTPUT	
CLOCK	RESET	Q	Q̄
x	L	x	H
↗	H	H	L
↘	H	L	H
L	H	x	NO CHANGE

H=HIGH L=LOW X=H or L

74240

(INVERTING OCTAL 3-STATE BUFFER)

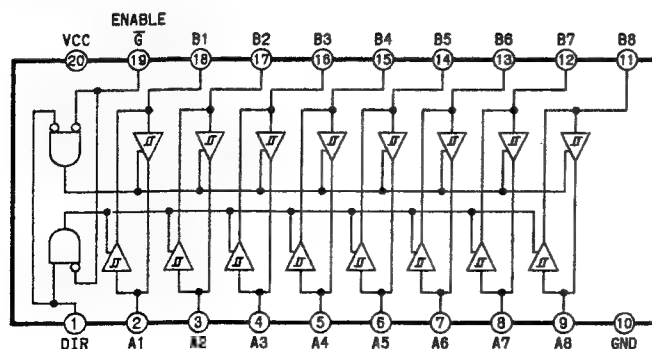


TRUTH TABLE (74HC240)

1G	1A	1Y	2G	2A	2Y
L	L	H	L	L	H
L	H	L	L	H	L
H	L	Z	L	L	Z
H	H	Z	L	H	Z

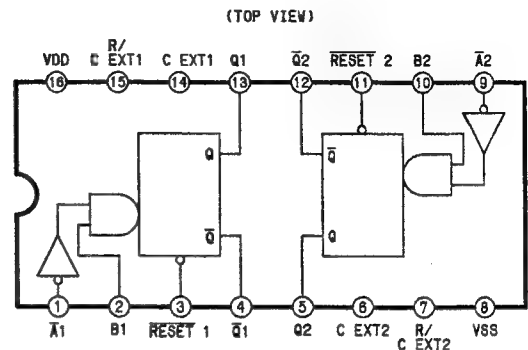
74245

(OCTAL 3-STATE BUS TRANSCEIVERS)

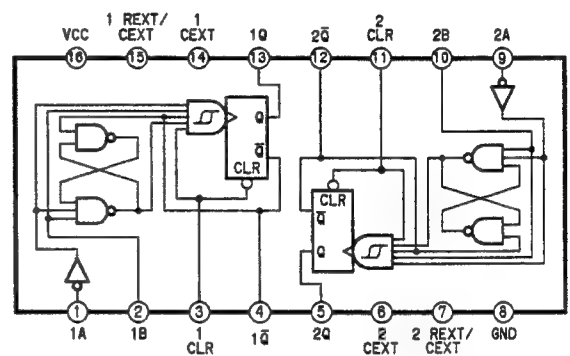


74221

(DUAL NON-RETRIGGERABLE MONOSTABLE MULTIVIBRATOR)



(74HC221)



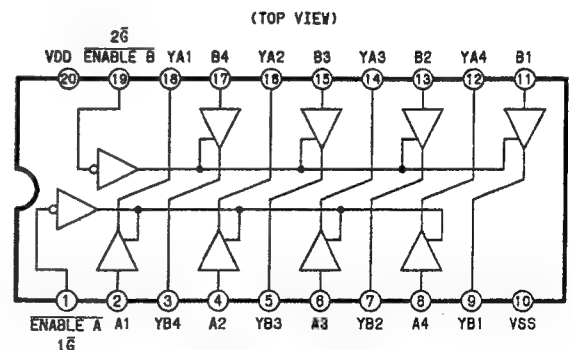
(74221)

TRUTH TABLE (74HC221)

INPUTS		OUTPUTS	
CLEAR	A	Q	Q̄
L	x	x	H
x	H	x	H
x	x	L	H
H	L	↑	↓
H	↓	H	↓
↑	L	H	↓

74244

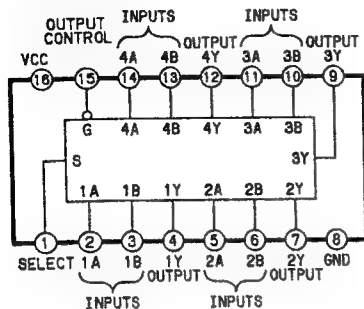
(OCTAL 3-STATE BUFFER)



TRUTH TABLE (74HC244)

1G	1A	1Y	2G	2A	2Y
L	L	L	L	L	L
L	H	L	L	H	L
H	L	Z	L	L	Z
H	H	Z	L	H	Z

74257
(QUAD 2-CHANNEL 3-STATE MULTIPLEXER)



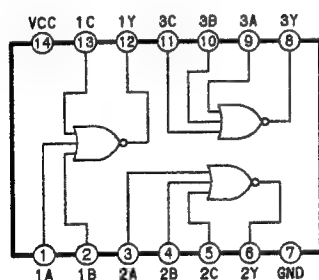
FUNCTION TABLE (74257)

INPUTS		OUTPUT Y
SELECT	OUTPUT CONTROL	
X	H	Z
L	L	A
H	L	B

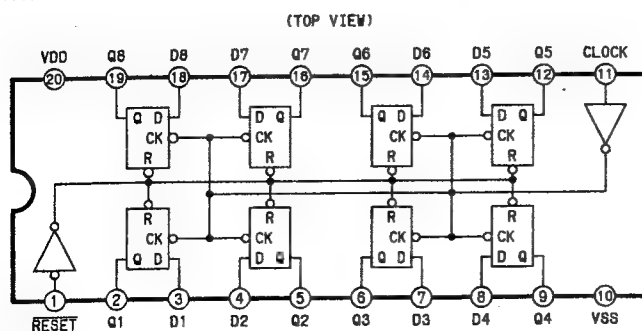
TRUTH TABLE (74HC257)

INPUTS			OUTPUT Y
OUTPUT CONTROL	SELECT	A B	
H	X	X X	Z
L	L	L X	L
L	L	H X	H
L	H	X L	L
L	H	X H	H

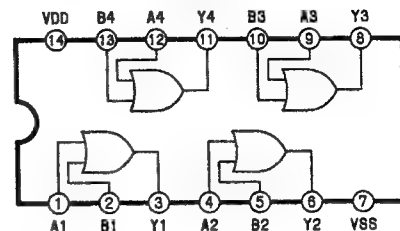
7427
(TRIPLE 3-INPUT NOR GATE)



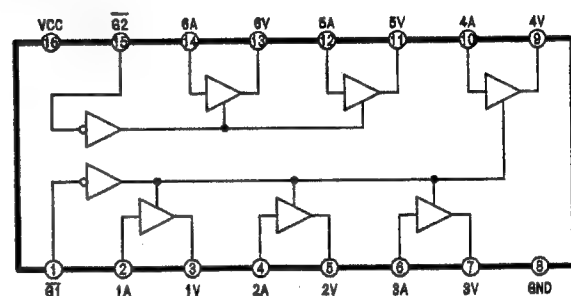
74273
(OCTAL D-TYPE FLIP-FLOP WITH CLEAR)



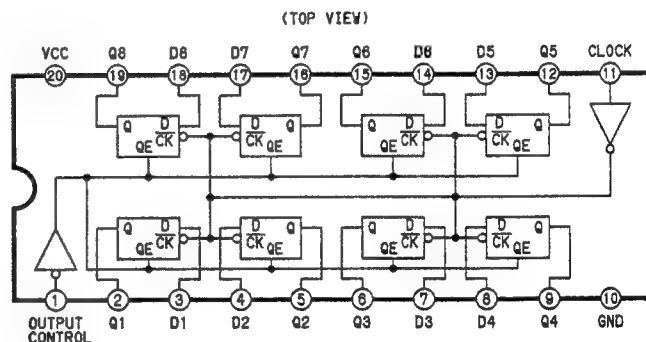
7432
(QUAD 2-INPUT OR GATE)
(TOP VIEW)



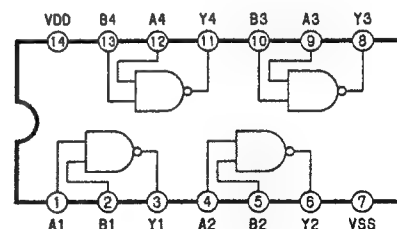
74367
(HEX 3-STATE BUS BUFFERS)



74374
(3-STATE OCTAL D-TYPE FLIP-FLOP)



7438
(QUAD 2-INPUT O.C. NAND BUFFER)
(TOP VIEW)



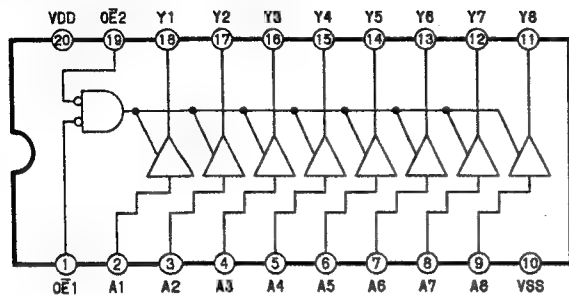
TRUTH TABLE (74HC273)

INPUTS			OUTPUTS Q
CLEAR	CLOCK	D	
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q0

74541

(OCTAL 3-STATE BUFFER)

(TOP VIEW)



OE1, OE2: OUTPUT ENABLE

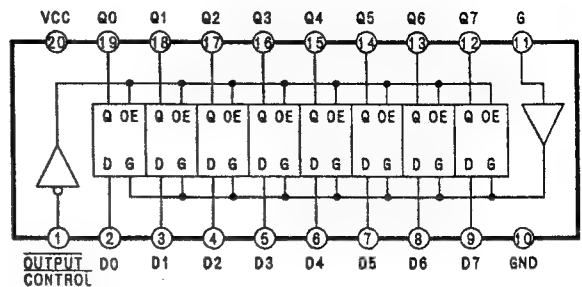
TRUTH TABLE

INPUT			OUTPUT
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

X: H or L Z: HIGH IMPEDANCE

74573

(OCTAL 3 STATE D-LATCHES)

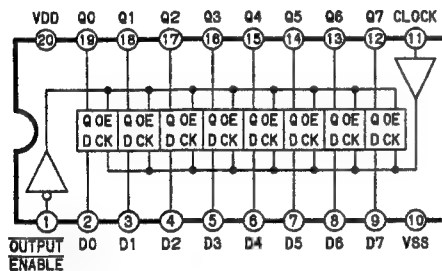


INPUT		FUNCTION
OUTPUT CONTROL	LATCH ENABLE	
L	L	LATCH (HOLD)
L	H	Q=D
H	X	HIGH-Z

74574

(OCTAL D-TYPE FLIP-FLOP)

(TOP VIEW)



TRUTH TABLE (74HC574)

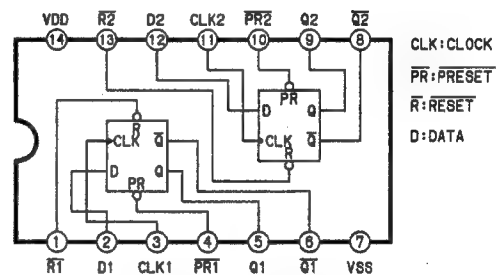
INPUT			OUTPUT
OUTPUT ENABLE	CLOCK	DATA D	Q
L	—	H	H
L	—	L	L
L	—	X	NO CHANGE
H	X	X	Z

X: H or L Z: HIGH IMPEDANCE

7474

(DUAL D-TYPE FLIP-FLOP)

(TOP VIEW)



TRUTH TABLE (74HC74)

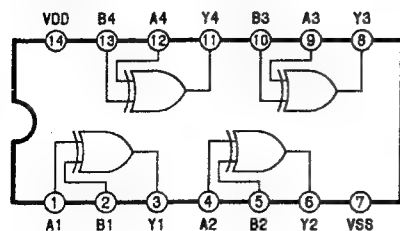
INPUTS				OUTPUTS	
PR	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	Q0

*: UNSTABLE

7486

(QUAD EXCLUSIVE OR GATE)

(TOP VIEW)



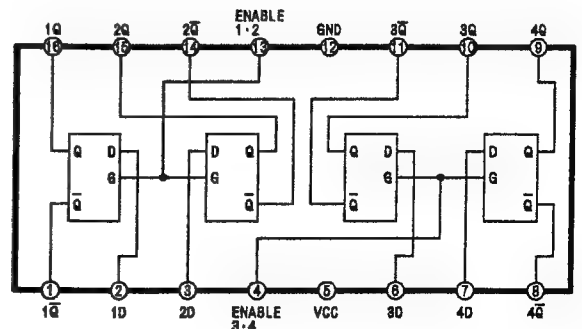
$$Y = A \oplus B = \bar{A}B + A\bar{B}$$

TRUTH TABLE

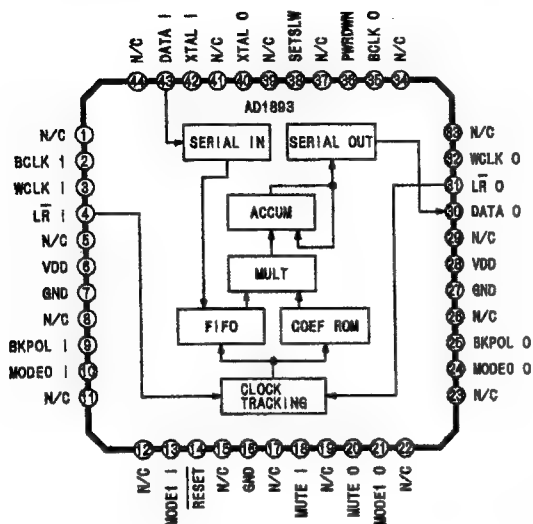
INPUTS		OUTPUTS	
A	B	Y	Y
L	L	L	L
L	H	H	H
H	L	H	H
H	H	L	L

7475

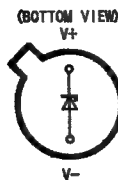
(4-BIT LATCHES)



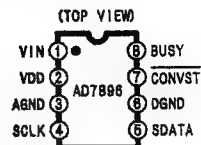
AD1893JST
(SAMPLING RATE CONVERTER)



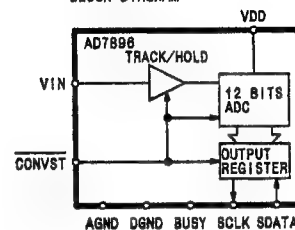
AD589
(VOLTAGE REGULATOR)



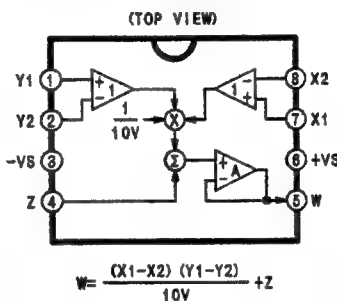
AD7898AR
(12 BITS A/D CONVERTER)



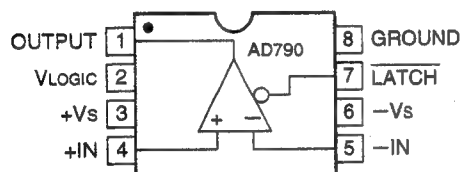
BLOCK DIAGRAM



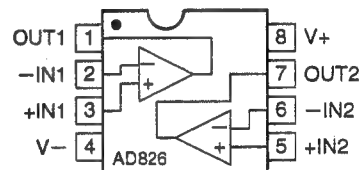
AD633JR
(ANALOG MULTIPLIER)



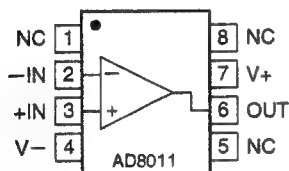
AD790 (FAST, PRECISION COMPARATOR)



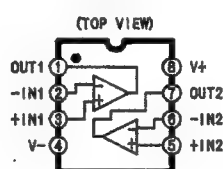
AD826AR (HIGH SPEED, LOW POWER DUAL OP AMP)



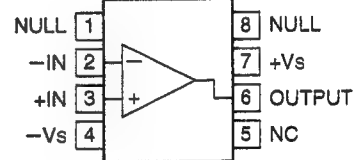
AD8011AR
(300MHz, 1mA CURRENT FEEDBACK OP AMP)



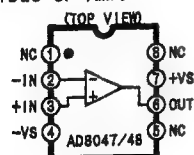
AD828AR
(VIDEO OP AMP)



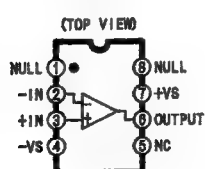
AD848JR
(TOP VIEW)



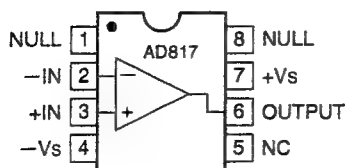
AD8047AR
(VIDEO OP AMP)



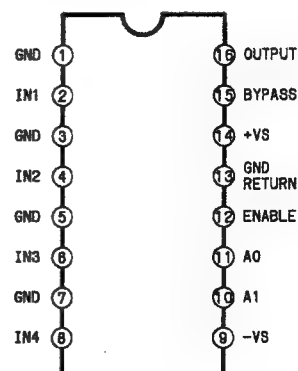
AD818AR
(VIDEO OP AMP)



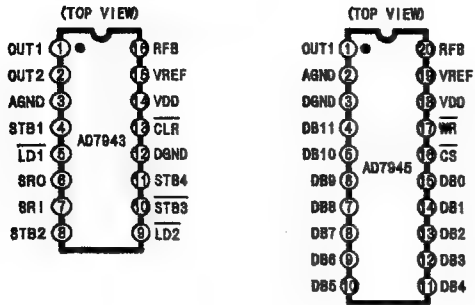
AD817AR (HIGH SPEED, LOW POWER OP AMP)



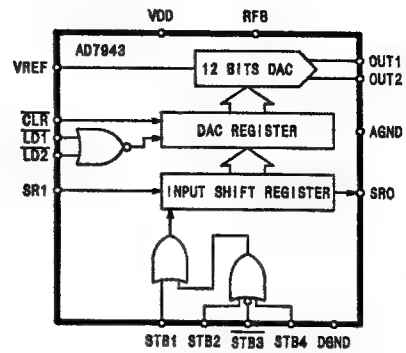
AD9300 (SELECT SWITCH)
(TOP VIEW)



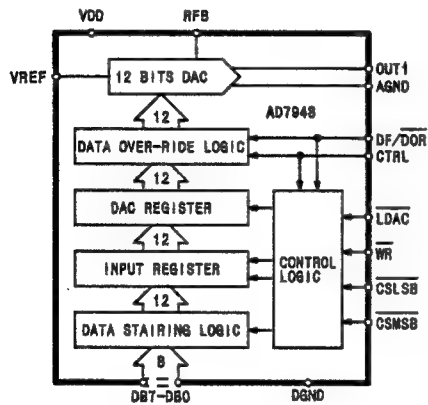
AD7943BR/AD7945BR (12 BITS D/A CONVERTER)



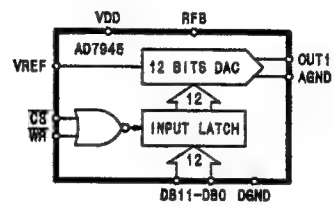
BLOCK DIAGRAM



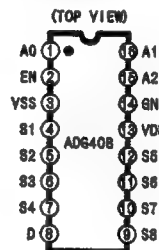
BLOCK DIAGRAM



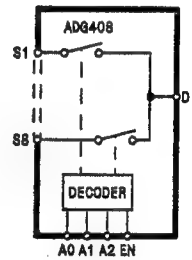
BLOCK DIAGRAM



ADG408BR (CMOS SWITCH)

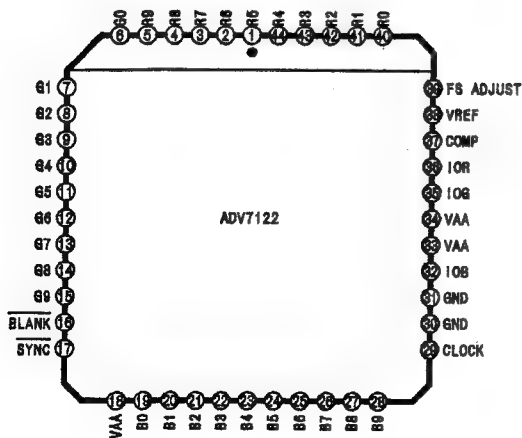


BLOCK DIAGRAM

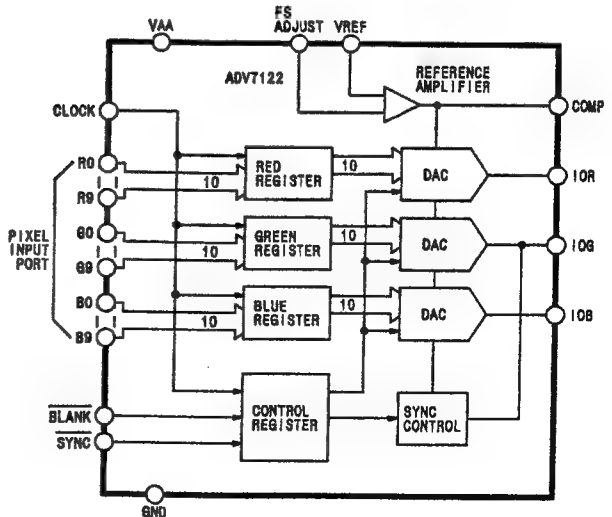


ADV7122 (VIDEO 10 BIT DA CONVERTER)

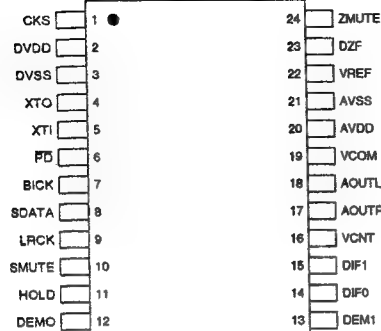
(TOP VIEW)



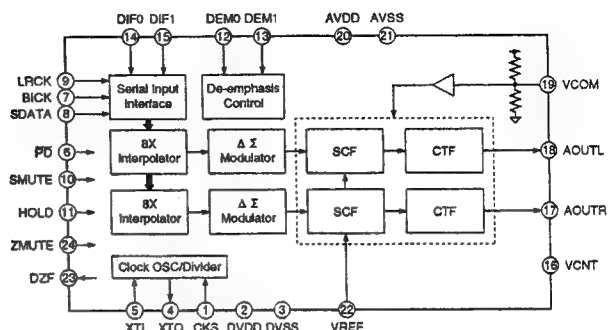
BLOCK DIAGRAM



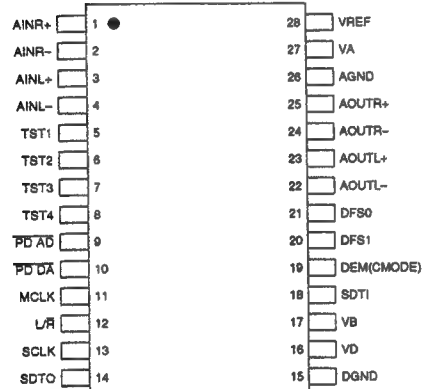
(TOP VIEW)



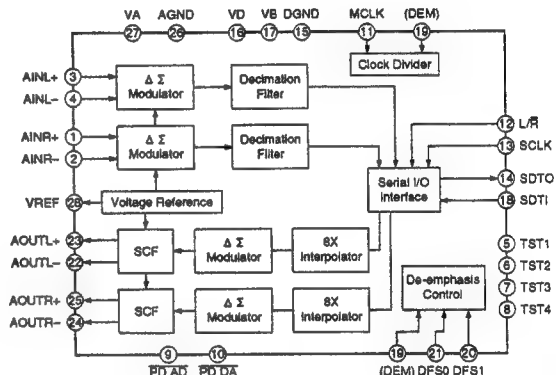
BLOCK DIAGRAM



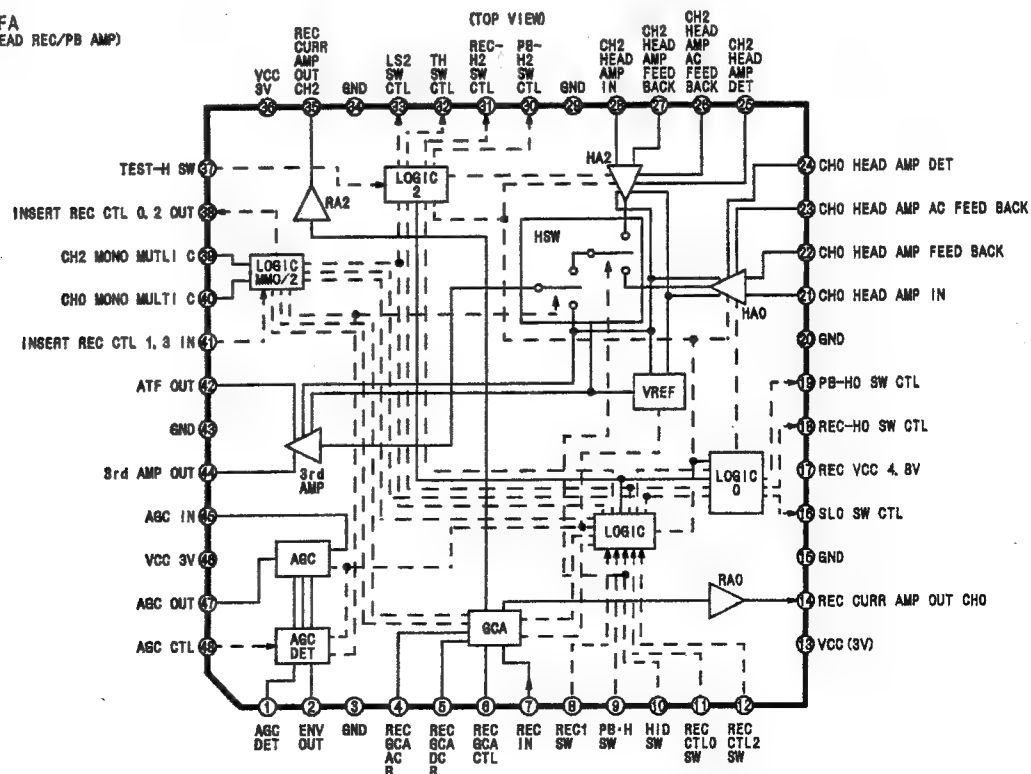
TOP VIEW



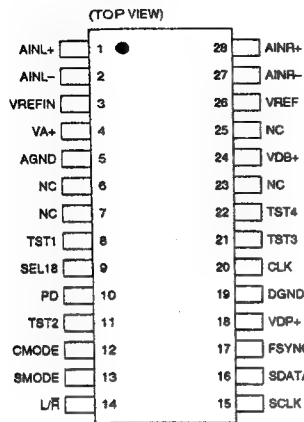
BLOCK DIAGRAM



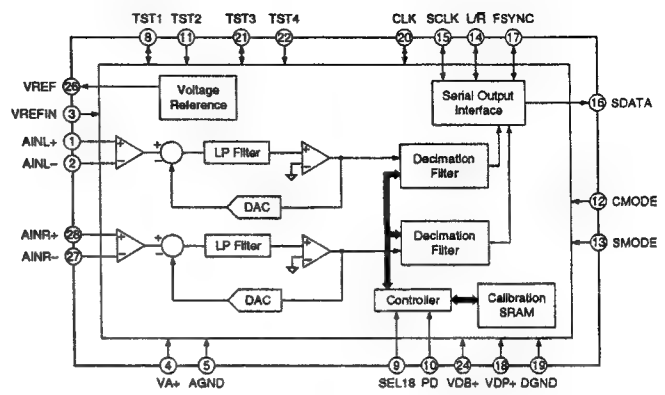
AN3730FA
(DVC 2 HEAD REC/PB AMP)



AK5340 (DA CONVERTER)

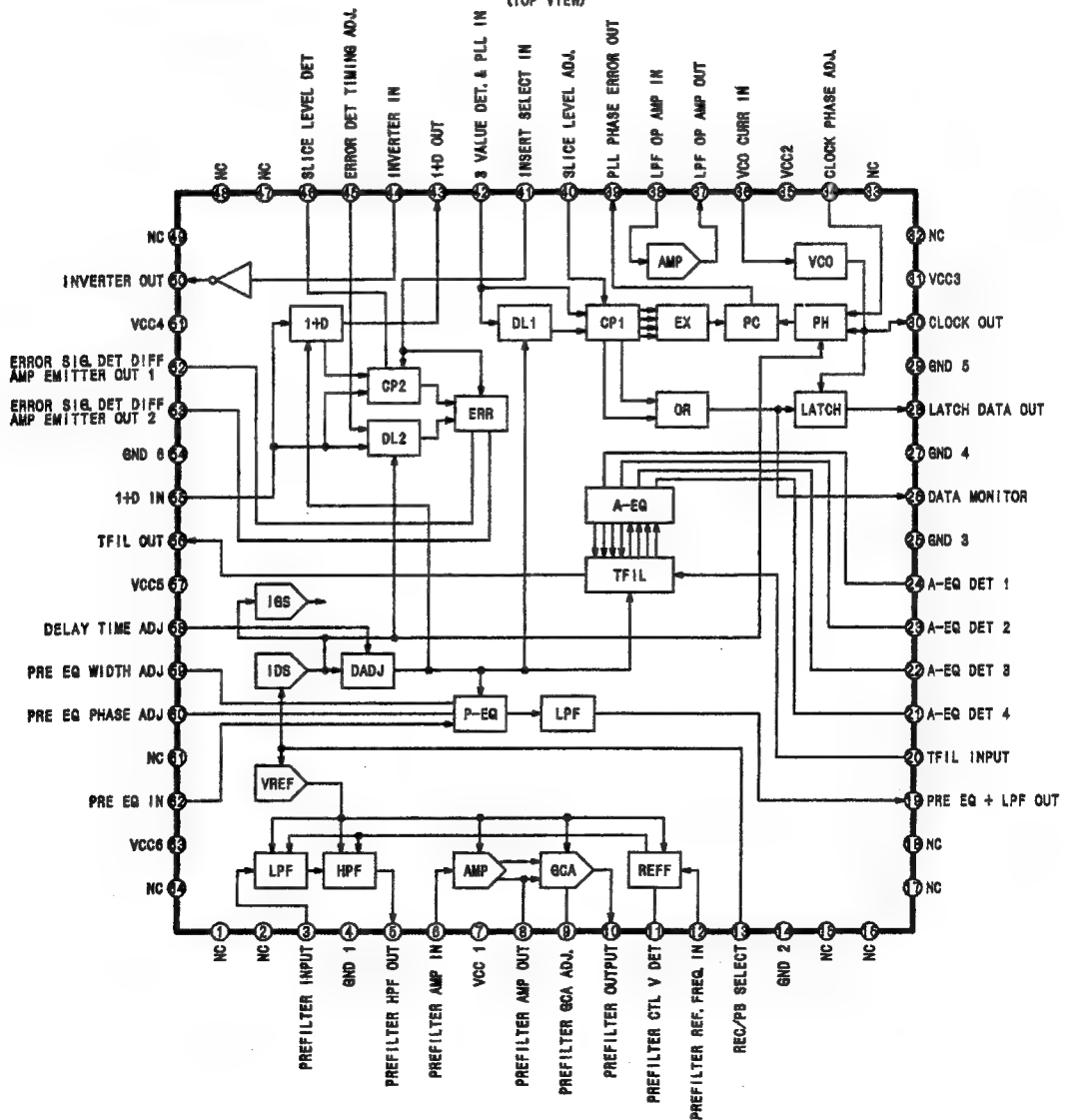


BLOCK DIAGRAM



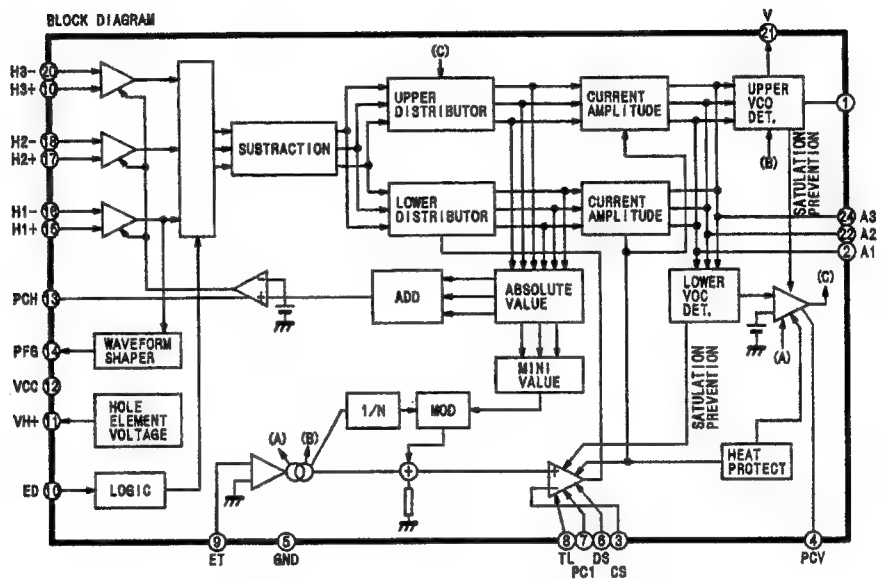
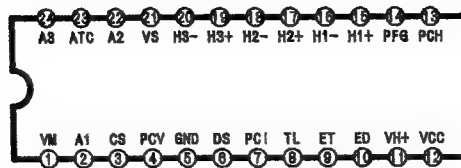
AN3740FAP (PLAYBACK EQUALIZER)

(TOP VIEW)

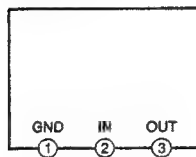


AN3834S

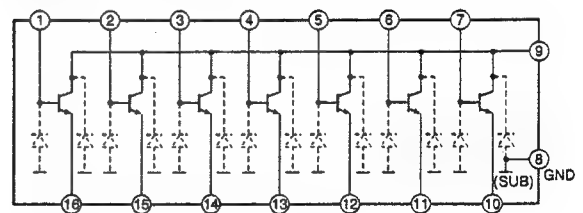
(TOP VIEW)



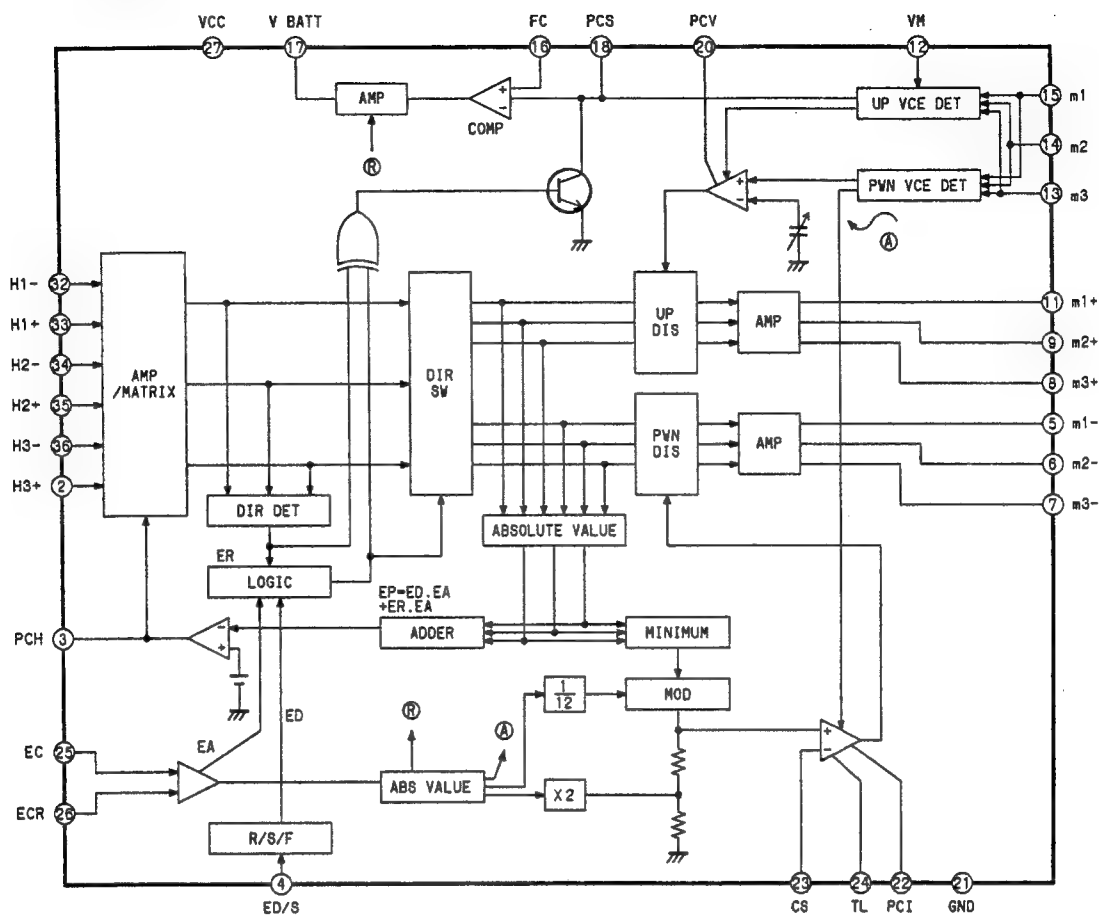
AN7905F



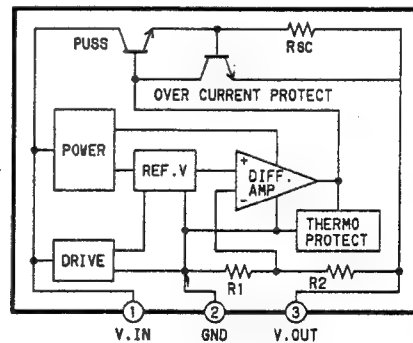
AN90B60S (EQUIVALENT CIRCUIT)



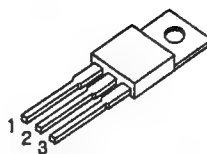
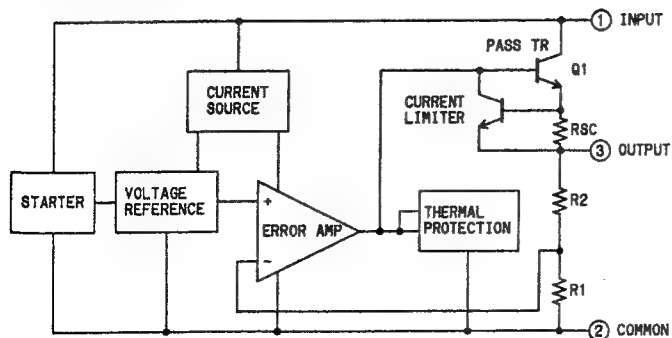
AN3890FBS



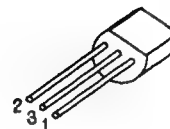
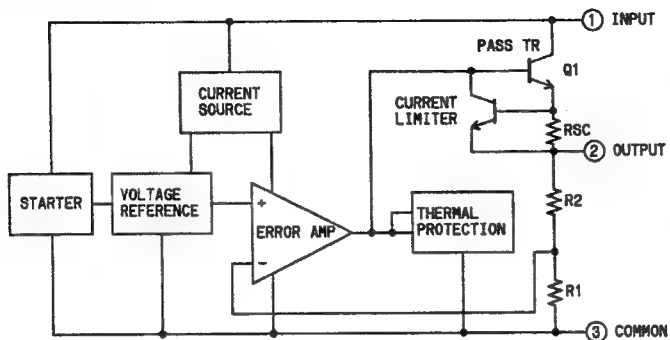
AN7805



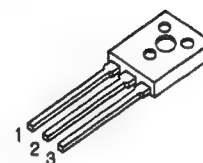
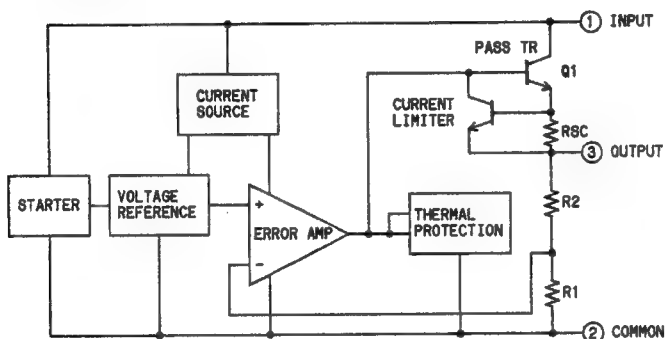
AN78M00 (3-TERMINAL POSITIVE OUTPUT VOLTAGE REGULATOR)



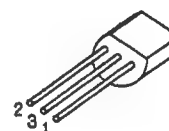
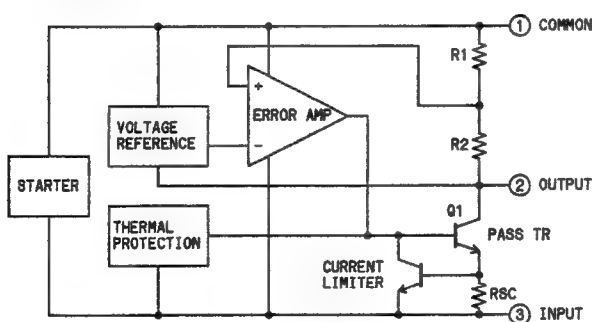
AN78L00
(3-TERMINAL POSITIVE OUTPUT VOLTAGE REGULATOR)



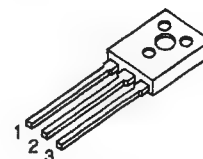
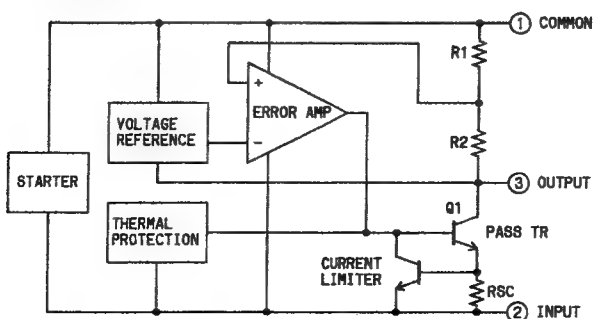
AN78N00
(3-TERMINAL POSITIVE OUTPUT VOLTAGE REGULATOR)



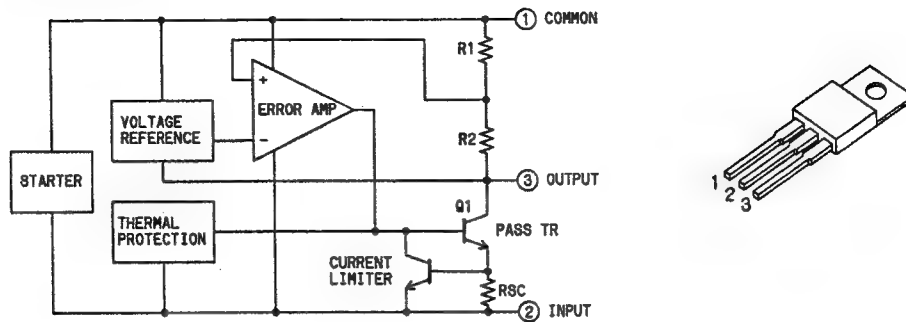
AN79L00
(3-TERMINAL NEGATIVE OUTPUT VOLTAGE REGULATOR)



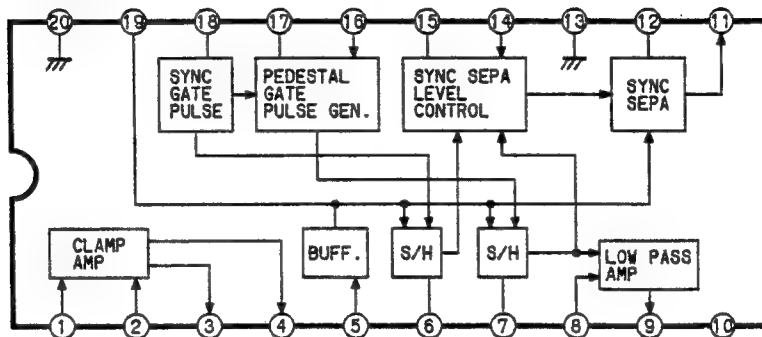
AN79N00
(3-TERMINAL NEGATIVE OUTPUT VOLTAGE REGULATOR)



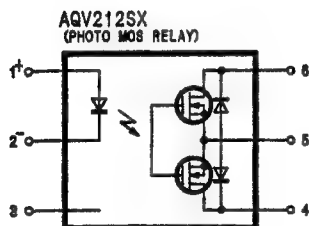
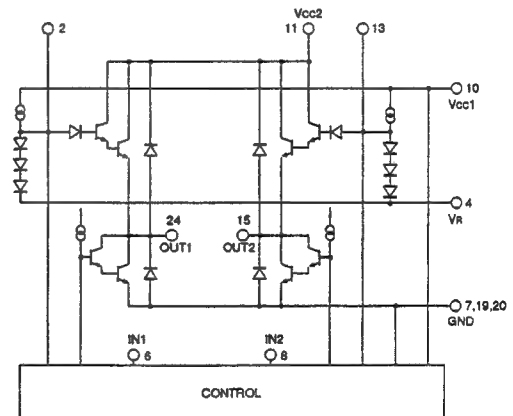
AN79M00
(3-TERMINAL NEGATIVE OUTPUT VOLTAGE REGULATOR)



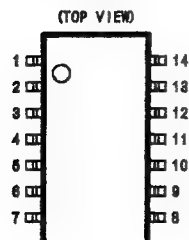
AN91A12S
(SYNC SEPARATOR)



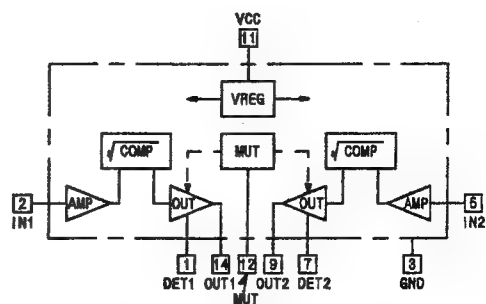
BA6219BFPY
BLOCK DIAGRAM



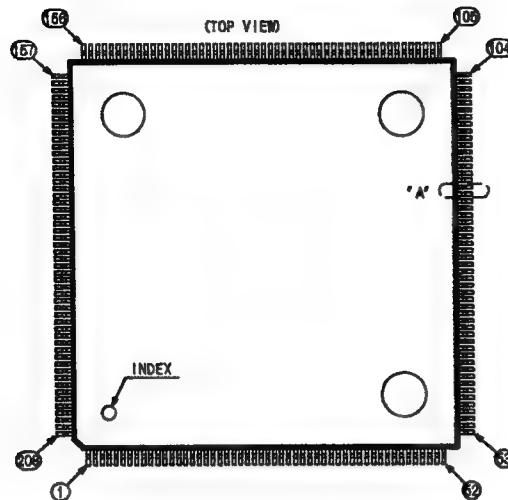
BA6138F
(1/2 MULTIPLE COMPRESSION AMP)



BLOCK DIAGRAM



CG31793-2153
(GATE ARRAY)

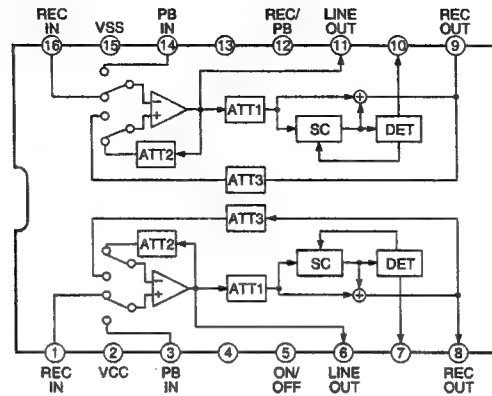


PIN ALIGNMENT

PIN NO.	I/O	PIN NAME	PIN NO.	I/O	PIN NAME	PIN NO.	I/O	PIN NAME	PIN NO.	I/O	PIN NAME
1	I/O	ADR1	53	I/O	BM OUT13	105	I	D IN7	157	I	SYSAD0
2	I/O	ADR2	54	I/O	BM OUT14	106	I	D IN8	158	I	SYSAD1
3	-	VSS	55	I/O	BM OUT15	107	-	VSS	159	I	SYSAD2
4	I/O	ADR3	56	I	JOGMWE	108	I	D IN9	160	I	SYSAD3
5	I/O	ADR4	57	I	VR IN2	109	I	D IN10	161	I	SYSAD4
6	I/O	ADR5	58	I/O	VR OUT2	110	I	D IN11	162	I	SYSAD5
7	I/O	ADR6	59	I	EEXP CLK	111	I	D IN12	163	I	BCK
8	I/O	ADR7	60	-	VSS	112	I	D IN13	164	-	VSS
9	I/O	ADR8	61	-	VDD	113	I	D IN14	165	-	VDD
10	-	VDD	62	I	EEXP REF	114	-	VDD	166	I	TEST8
11	I/O	ADR9	63	I	PRTY1	115	I	D IN15	167	I	TEST8
12	I/O	ADR10	64	I	PRTY2	116	I	IA DATA	168	I/O	BLKSYNC
13	I/O	ADR11	65	I	LCK2	117	I	ID DATA	169	I	TEST RST
14	I/O	ADR12	66	-	N.C.	118	I	SG DATA	170	I	HIZ
15	-	VSS	67	I/O	ARECFRP	119	-	VSS	171	O	TDO
16	I/O	ADR13	68	I/O	RFRP ERR	120	I/O	REC DATA	172	I	TDI
17	I/O	ADR14	69	I/O	REC LEAP	121	I/O	QUE MIXO	173	I	TMS
18	I/O	DATA0	70	I/O	RFR GATE	122	I	PBDATA	174	I	TR8
19	I/O	DATA1	71	I	PB LEAP2	123	I	CUENDATA	175	I	TCK
20	I/O	DATA2	72	-	VSS	124	I/O	MONIDATA	176	-	VSS
21	I/O	DATA3	73	I	MCK	125	-	N.C.	177	I	FS266
22	I/O	DATA4	74	I	TEST4	126	I	RXLCK1	178	I	CLK REF2
23	I/O	DATA5	75	I	REC FRP	127	I	RXBCK1	179	I	CLK REF1
24	I/O	DATA6	76	I/O	T OUT1	128	I	RXLCK2	180	I/O	FS64
25	I/O	DATA7	77	I/O	T OUT2	129	I	RXBCK2	181	I/O	FS
26	-	VSS	78	I/O	T OUT3	130	-	VSS	182	I/O	FS128
27	-	VDD	79	-	VDD	131	-	VDD	183	-	VDD
28	I/O	WE	80	I/O	T OUT4	132	I/O	RRST	184	-	N.C.
29	I/O	WRITE H	81	I	PBFRP	133	I/O	WRST1	185	I	QUEPP
30	I/O	M FAST	82	I	FEND	134	I/O	WRST2	186	I	SSD
31	I/O	M SLOW	83	I	APF18	135	I/O	WRST3	187	I	TTD
32	I/O	BUFERROR	84	I	CLK18	136	I/O	FIF GATE	188	I	VCO24M
33	I/O	JOSMCK	85	-	VSS	137	I	VR IN	189	-	VSS
34	I/O	FIELD	86	I	PB LEAP1	138	I/O	VR OUT	190	I	VCO9M
35	I/O	VALID	87	I	TEST3	139	I	PONRST	191	I	HALF L
36	I/O	LEAP	88	I	FR	140	I	PALH	192	I/O	COMPFH
37	I/O	BM OUT0	89	I/O	NOM OUT	141	I	LCK	193	I/O	REF12K
38	-	VSS	90	I	NOM IN	142	-	VSS	194	I/O	COMP12K
39	I/O	BM OUT1	91	I	LR2	143	I	PB LCK	195	-	N.C.
40	I/O	BM OUT2	92	I/O	DOUT	144	I	SYSOS	196	-	N.C.
41	I/O	BM OUT3	93	I	MUT	145	I	SYSRD	197	I	TEST1
42	I/O	BM OUT4	94	I	NDOWR	146	I	SYSWE	198	I	TEST2
43	-	VDD	95	I	PB LCK2	147	-	VDD	199	I	PB BCK
44	I/O	BM OUT5	96	-	VSS	148	I/O	SYSDA0	200	-	VSS
45	I/O	BM OUT6	97	-	VDD	149	I/O	SYSDA1	201	-	VDD
46	I/O	BM OUT7	98	I	D IN0	150	I/O	SYSDA2	202	I	D1R
47	I/O	BM OUT8	99	I	D IN1	151	I/O	SYSDA3	203	I	TP0
48	I/O	BM OUT9	100	I	D IN2	152	I/O	SYSDA4	204	I	TP1
49	I/O	BM OUT10	101	I	D IN3	153	I/O	SYSDA5	205	I	TP2
50	-	VSS	102	I	D IN4	154	-	VSS	206	I	BM IN
51	I/O	BM OUT11	103	I	D IN5	155	I/O	SYSDA6	207	I/O	INIT
52	I/O	BM OUT12	104	I	D IN6	156	I/O	SYSDA7	208	I/O	ADR0

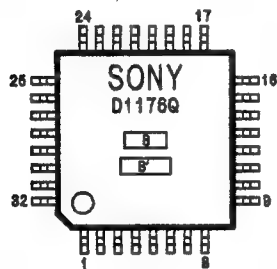
CXA1102M

BLOCK DIAGRAM

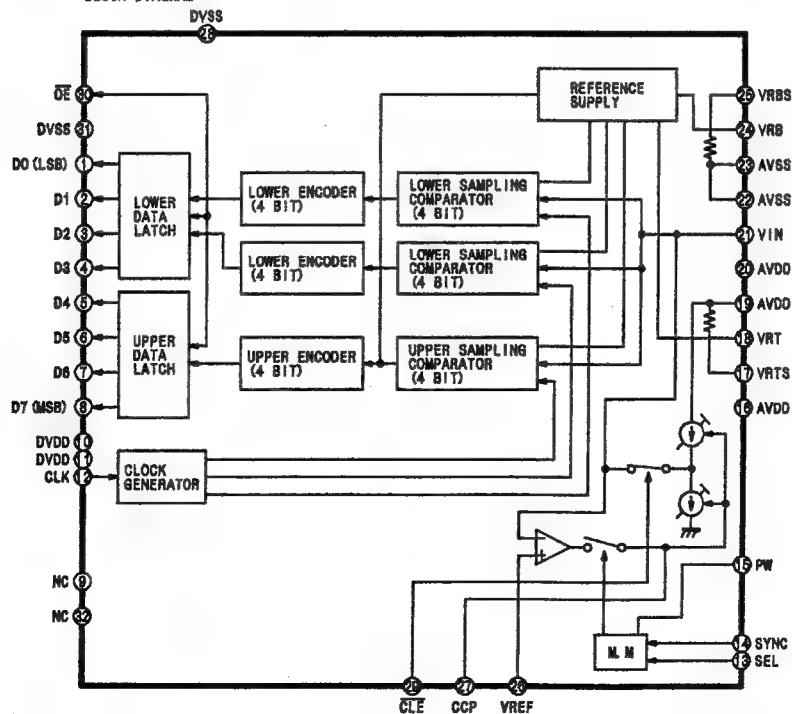


CXD1176Q

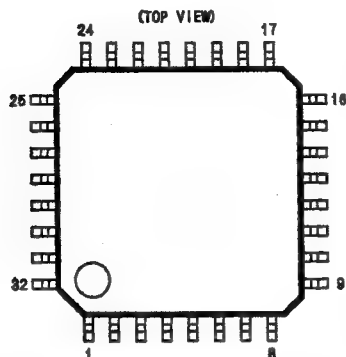
(8 BITS 20 MSPS VIDEO A/D CONVERTER WITH CLAMP FUNCTION)



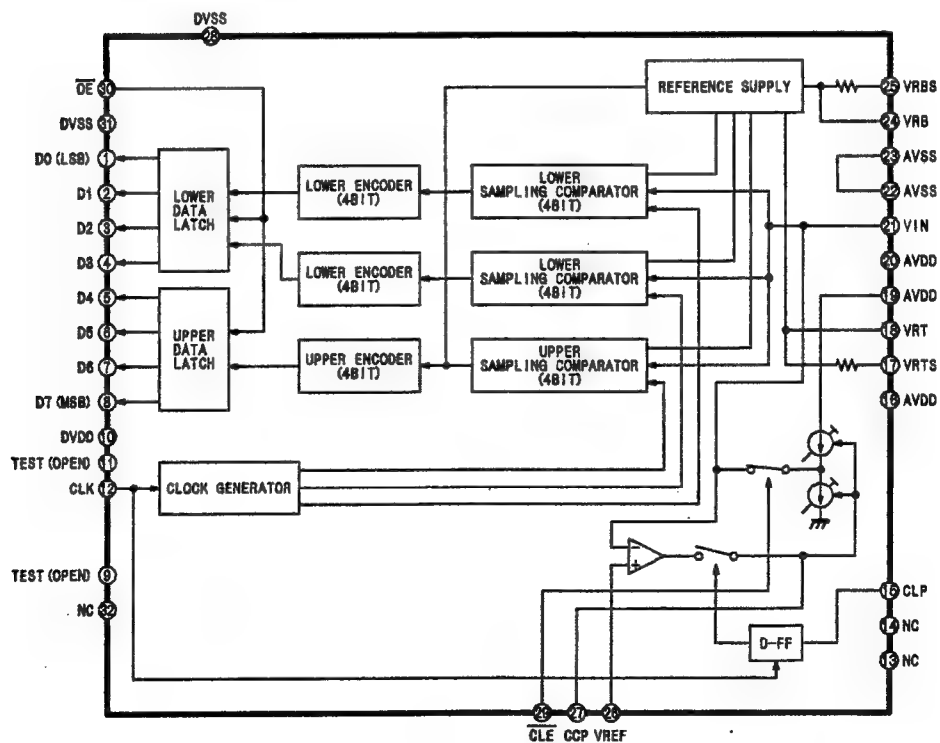
BLOCK DIAGRAM



CXD2302Q
(8 BITS 50MSPS VIDEO A/D CONVERTER)
(WITH CLAMP OPERATION)

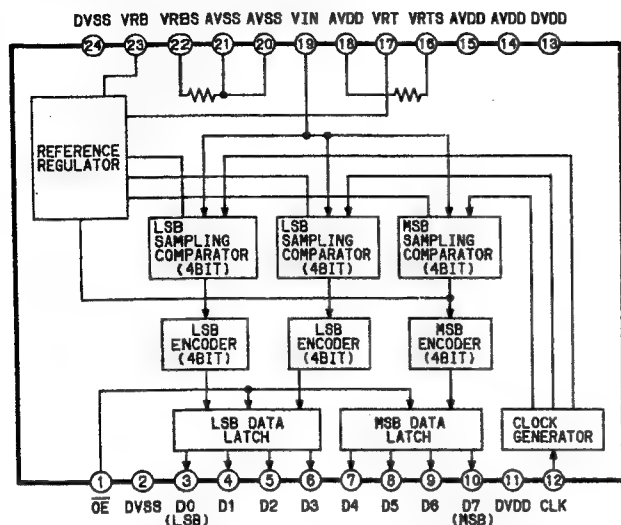


BLOCK DIAGRAM



CXD1175AM

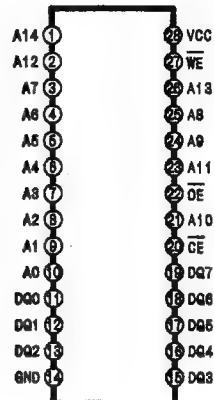
(8BIT 20MSPS VIDEO A/D CONVERTER)



DS1230Y100

(256K NONVOLATILE SRAM)

PIN ASSIGNMENT



PIN DESCRIPTION

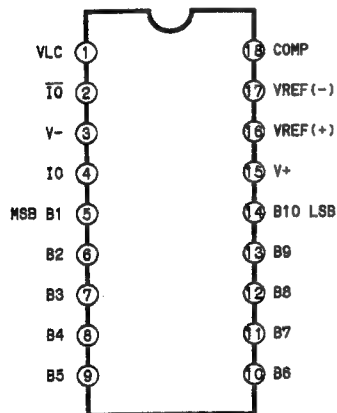
- A0-A14 - ADDRESS INPUTS
- CE - CHIP ENABLE
- GND - GROUND
- DQ0-DQ7 - DATA IN/DATA OUT
- VCC - POWER (+5V)
- WE - WRITE ENABLE
- OE - OUTPUT ENABLE

DAC10-GX

(10-BIT D/A CONVERTER)

(18PIN HERMETIC DIP)

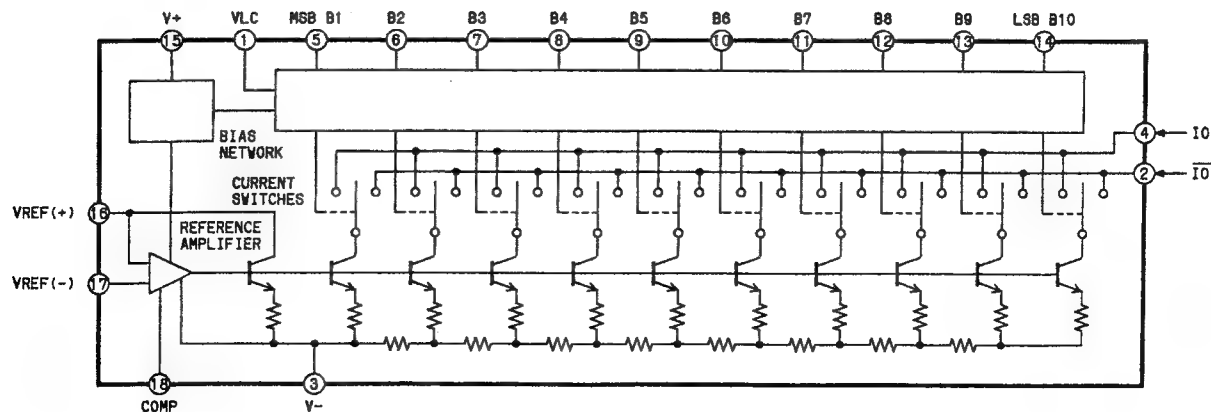
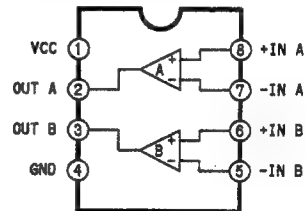
(TOP VIEW)



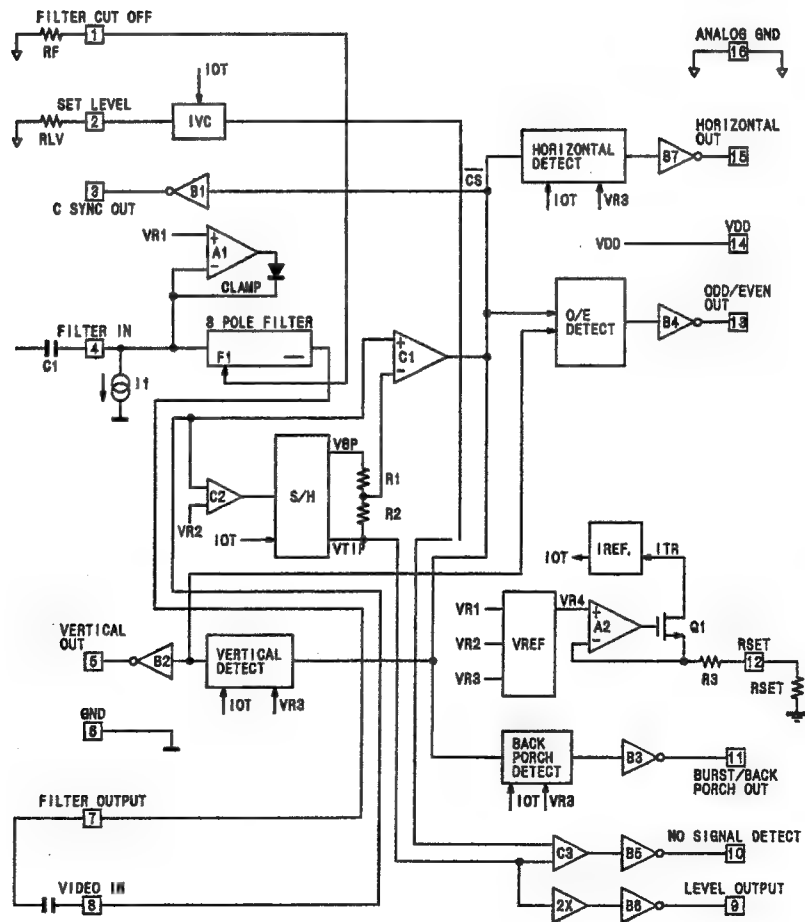
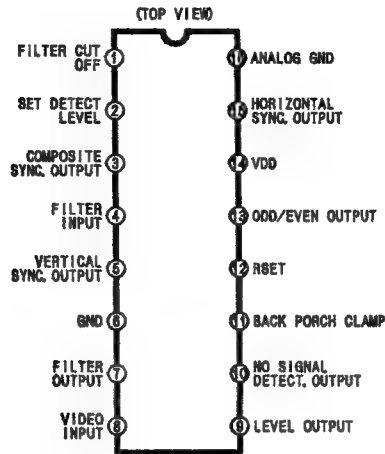
DS9637A

(DUAL DIFFERENTIAL LINE RECEIVER)

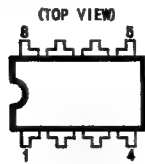
(TOP VIEW)



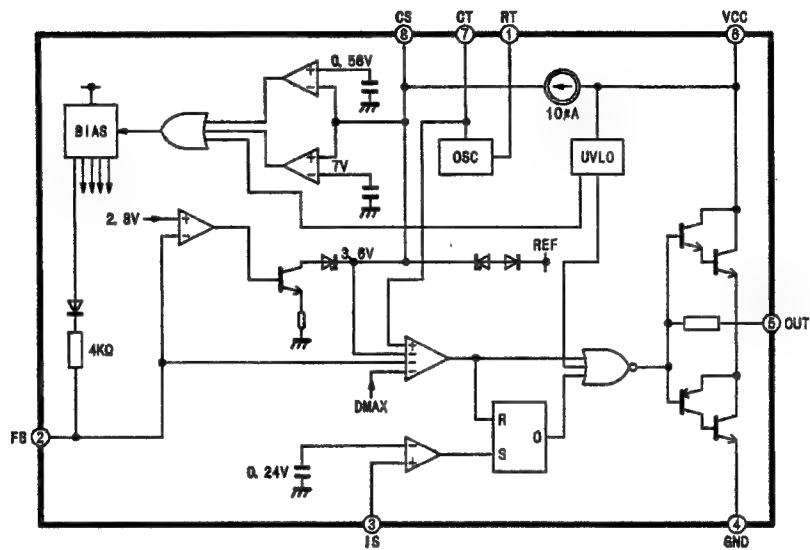
EL4583CS
(VIDEO SYNC SEPARATOR)



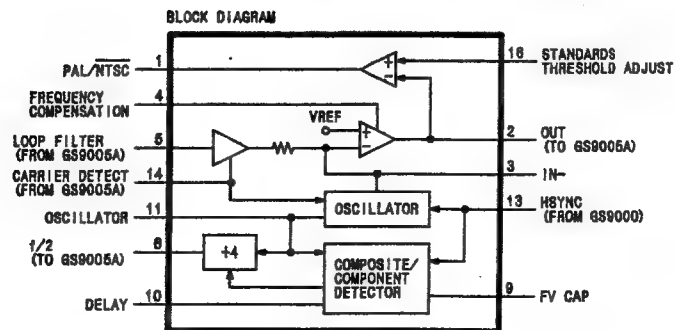
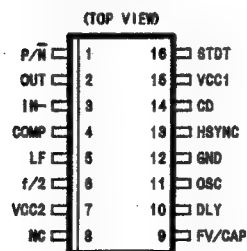
FA5311P
(PWM SWITCHING POWER CONTROL)



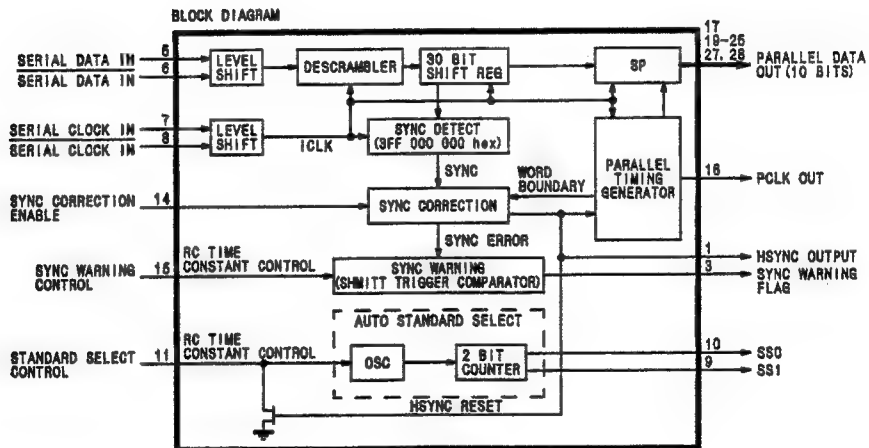
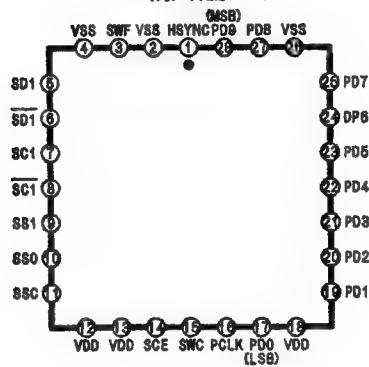
BLOCK DIAGRAM



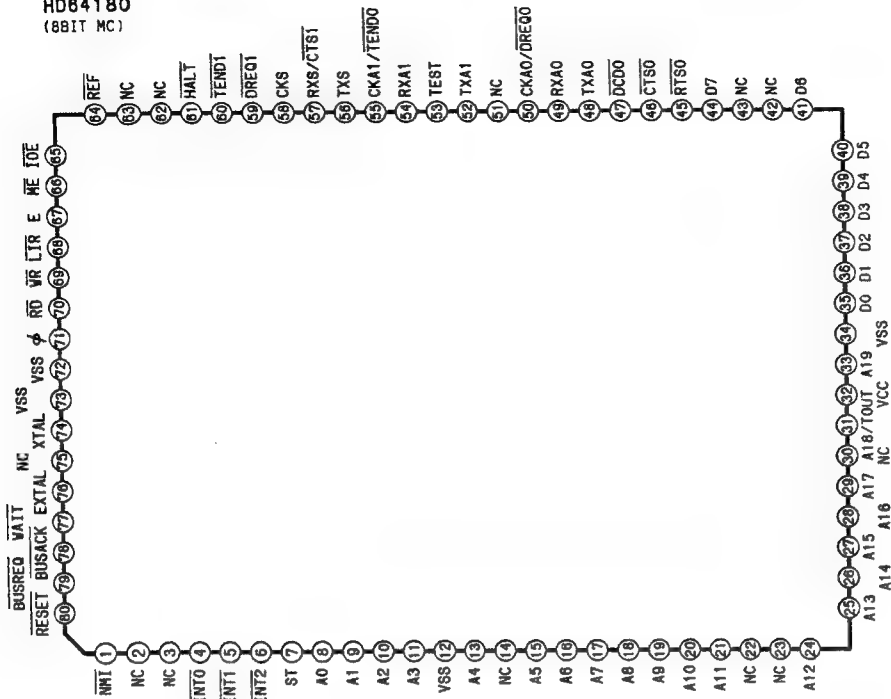
GS9010
SERIAL DIGITAL AUTO TUNING SUB SYSTEM



GS9000
(SERIAL DIGITAL DECODER)
(TOP VIEW)

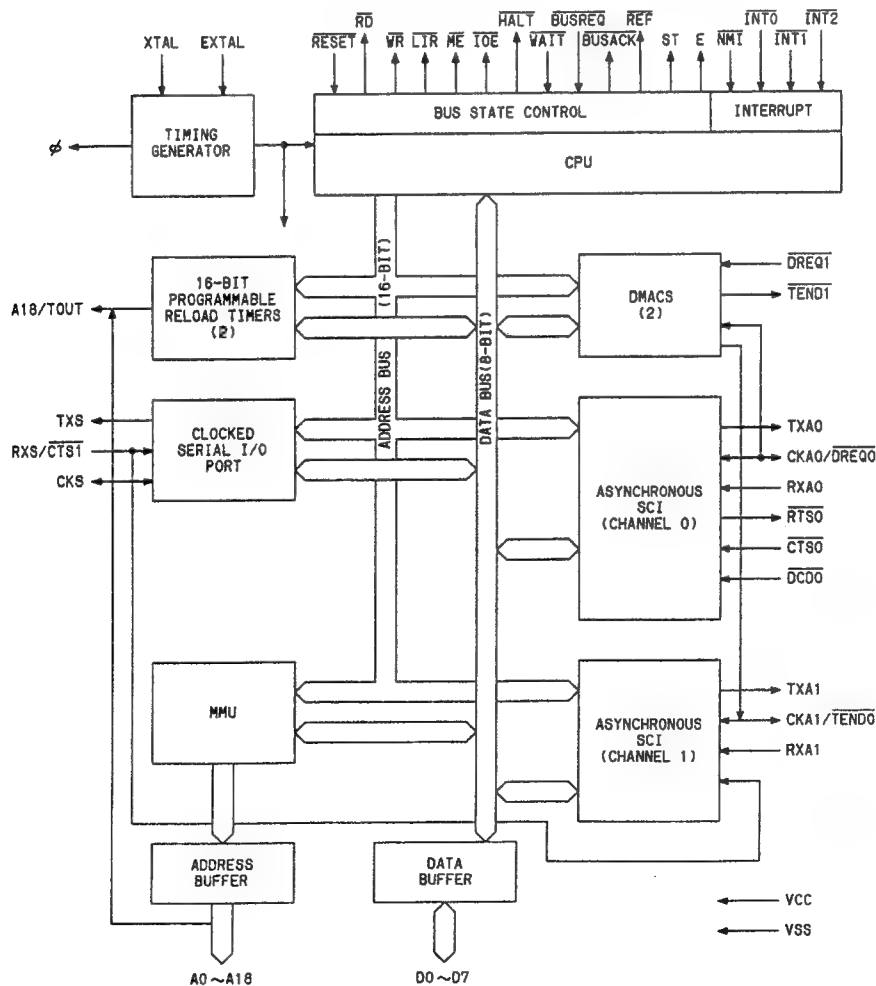
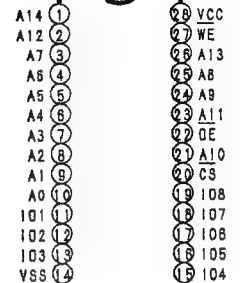


HD64180
(8BIT MC)

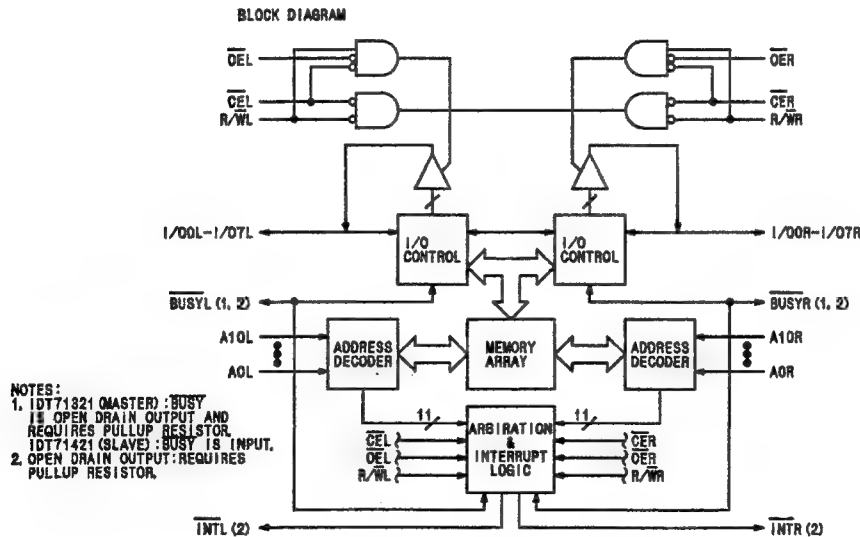
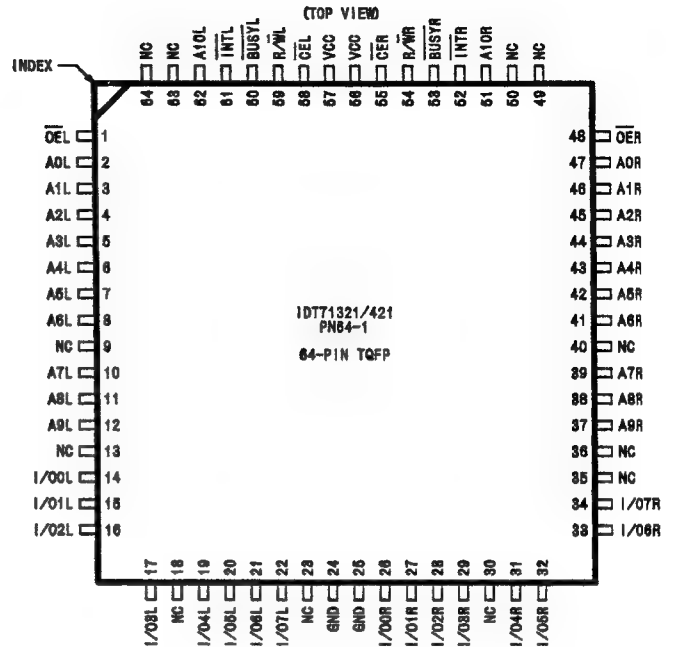
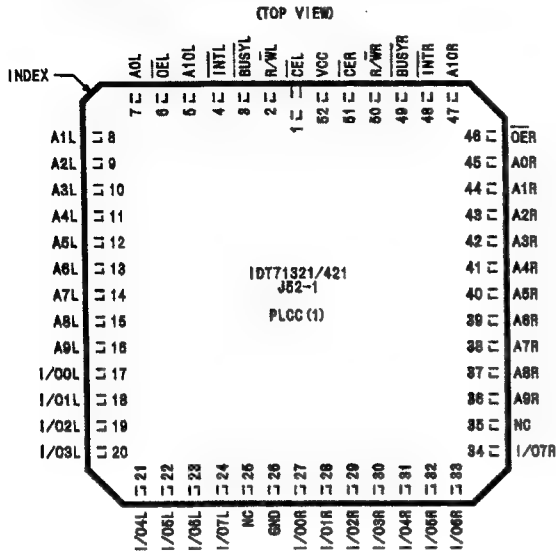


K6256BLG7L
K6256CLG7L

(TOP VIEW)

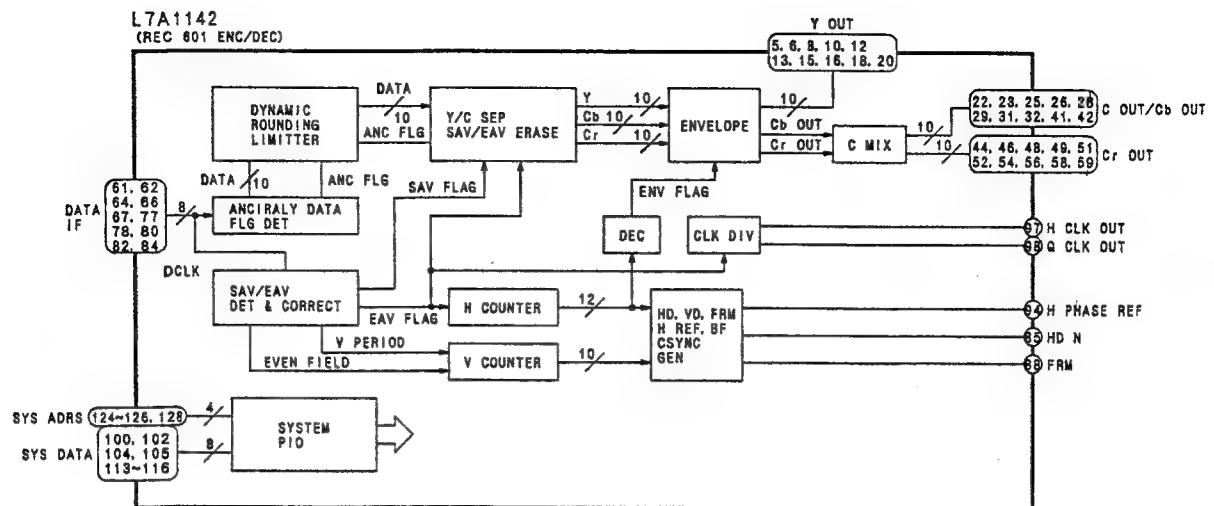


IDT71321A55T
(CMOS DUAL-PORT RAM 16K (2Kx8 BIT) WITH INTERRUPTS)

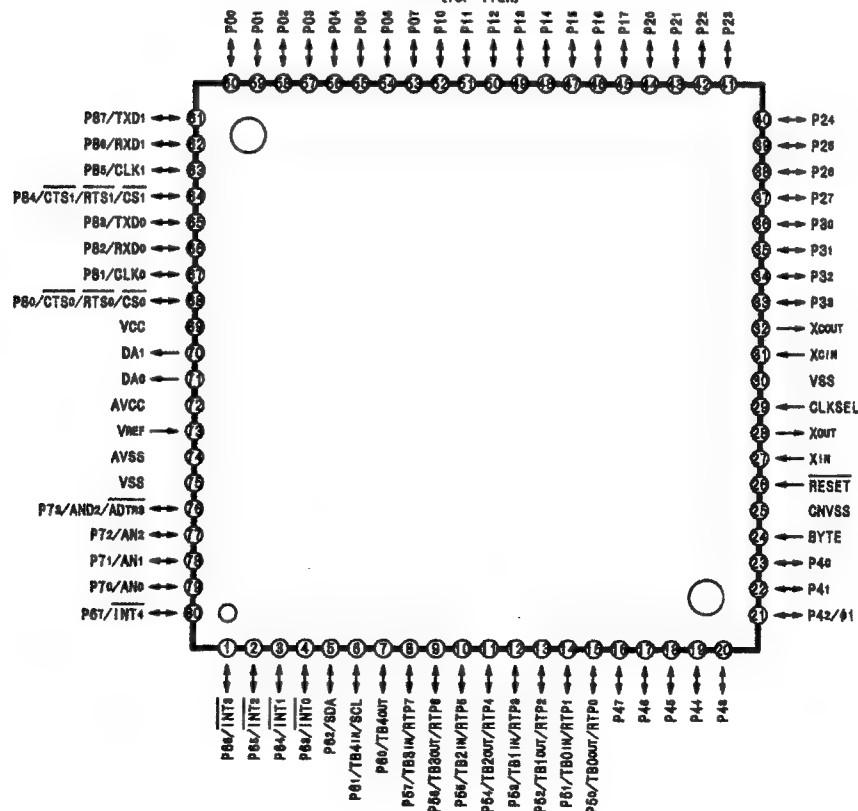


(TOP VIEW)

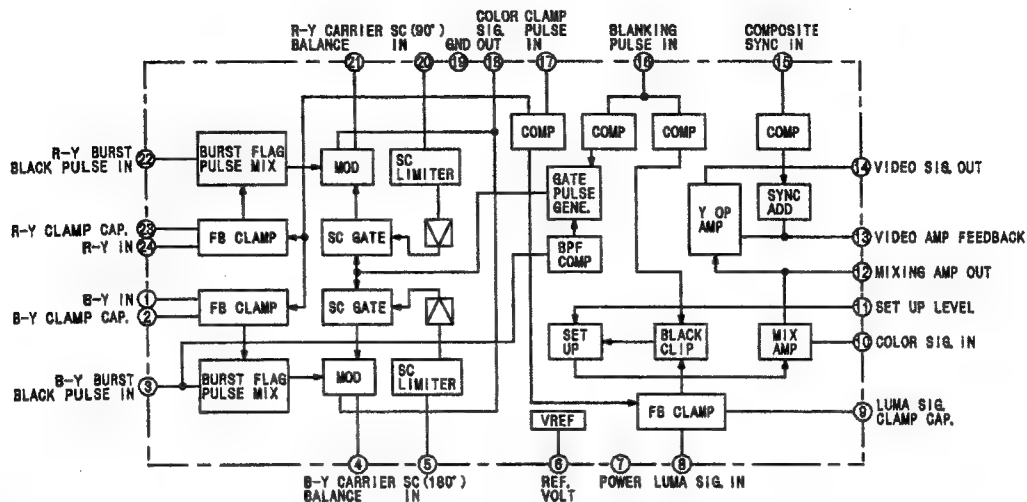




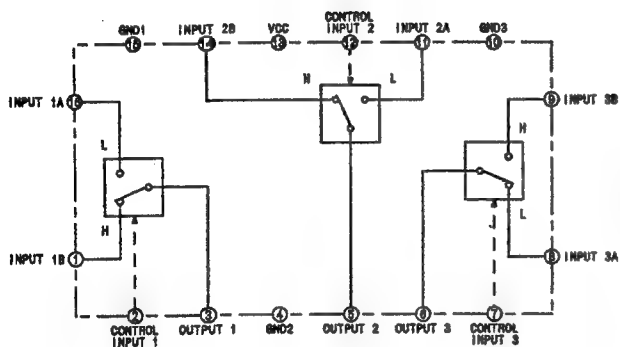
M37709E4LGP
(SINGLE CHIP 16 BITS MICROCOMPUTER)
(TOP VIEW)



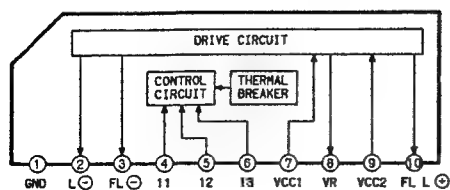
BLOCK DIAGRAM



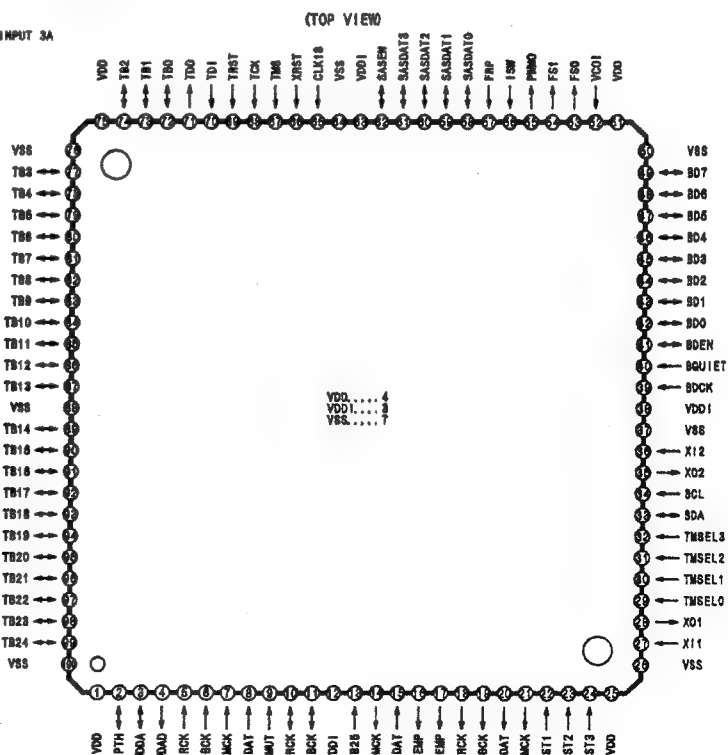
M52055P
(3 CH ANALOG SWITCH)

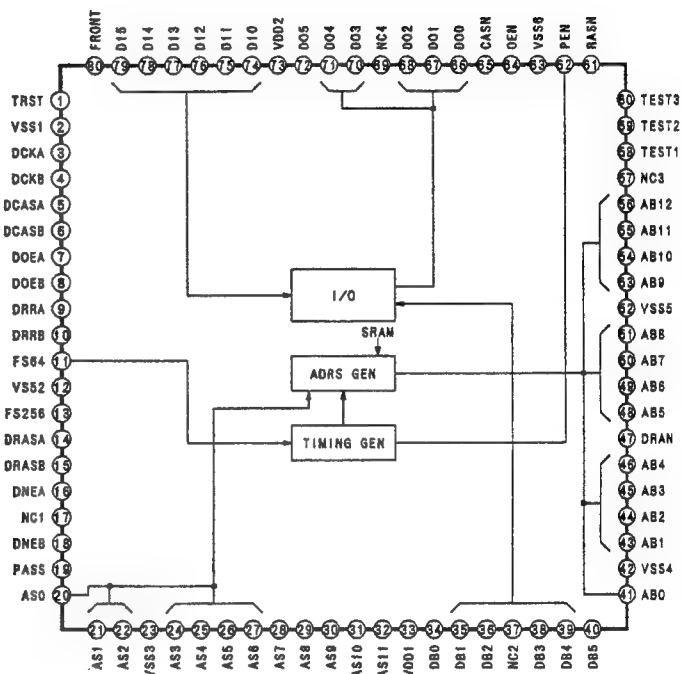


M54649L



M85401FP
(DIGITAL AUDIO SIGNAL PROCESSOR)

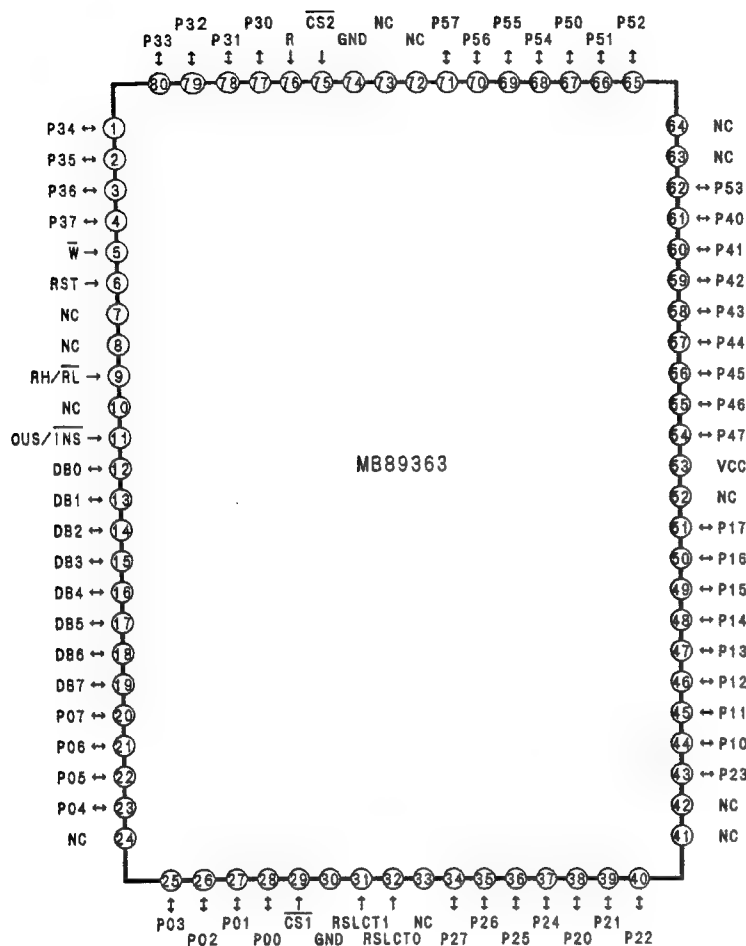


[illegible]

(TOP VIEW)

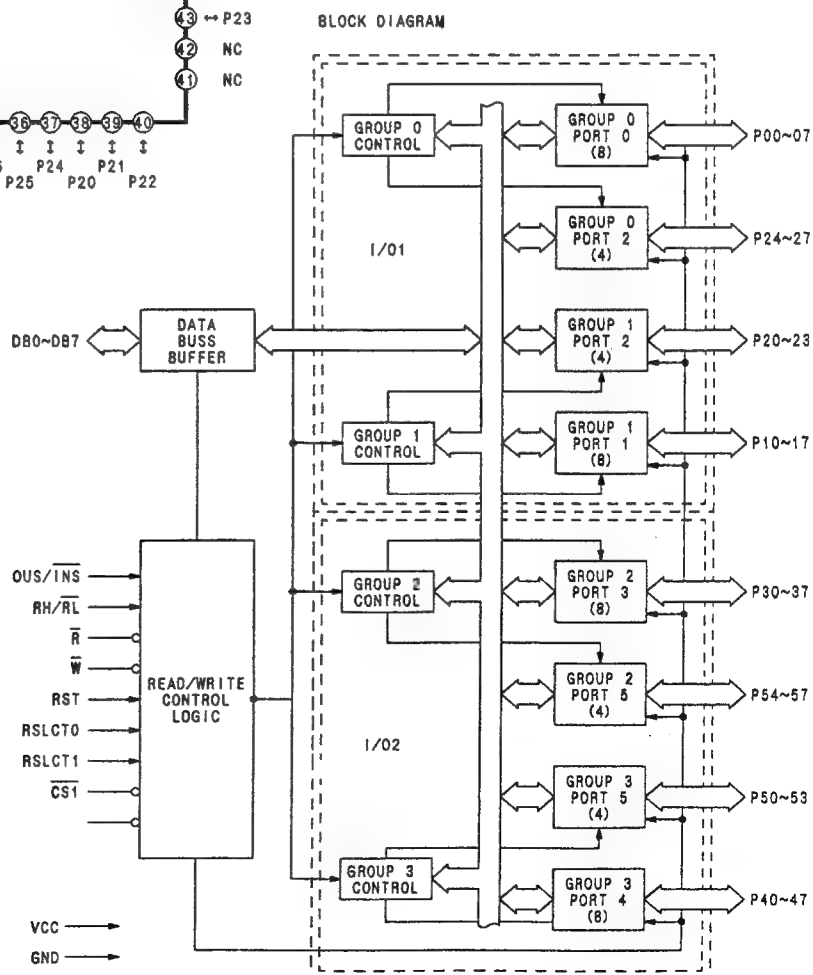
VCC	1	44	VSS
DQ1	2	43	DQ16
DQ2	3	42	DQ15
DQ3	4	41	DQ14
DQ4	5	40	DQ13
VCC	6	39	VSS
DQ5	7	38	DQ12
DQ6	8	37	DQ11
DQ7	9	36	DQ10
DQ8	10	35	DQ9
NC	13	32	NC
NC	14	31	LCAS
WE	15	30	UCAS
RAS	16	29	OE
NC	17	28	A8
A0	18	27	A7
A1	19	26	A6
A2	20	25	A5
A3	21	24	A4
VCC	22	23	VSS



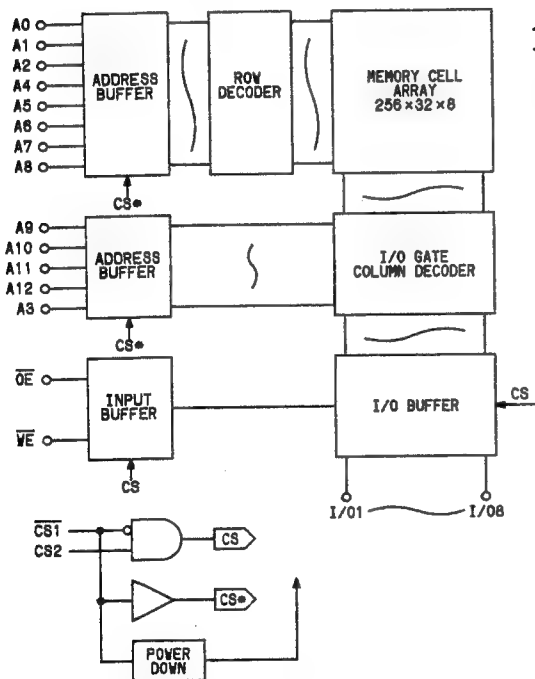
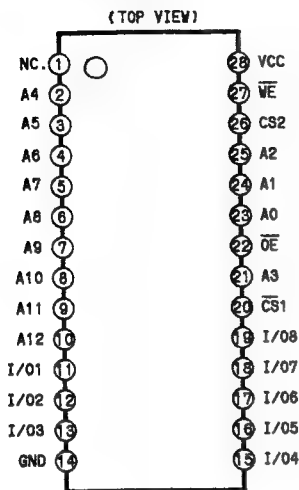


MB889363

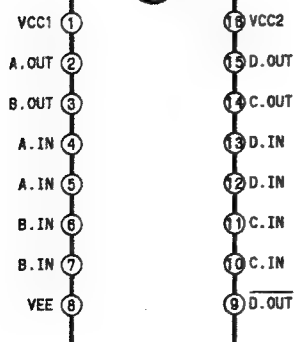
MB889363
(PROGRAMMABLE PERIPHERAL INTERFACE)
(TOP VIEW)



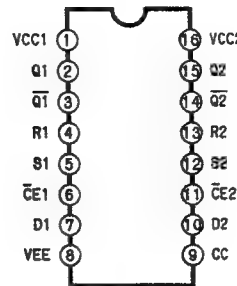
MB81C78A35PF (8K MEMORY)



MC10H102 (QUAD 2-INPUT NOR GATE) (TOP VIEW)



MC10131 (DUAL TYPED MASTER-SLAVE FLIP-FLOP)



CLOCKED TRUTH TABLE

C	D	QN-1
L	φ	QN
H	L	L
H	H	H

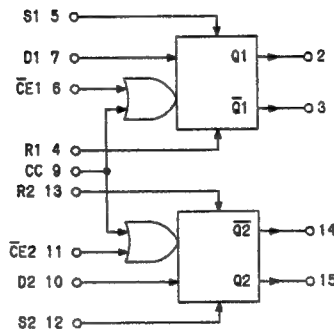
φ - DON'T CARE
C = CE + CC
A CLOCK H IS A CLOCK TRANSITION FROM A LOW TO A HIGH STATE.

R-S TRUTH TABLE

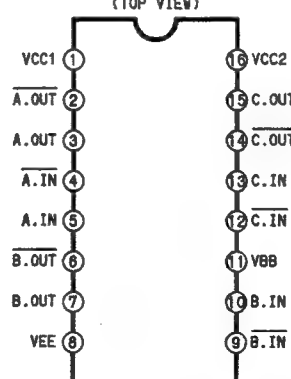
R	S	QN-1
L	L	QN
L	H	H
H	L	L
H	H	N.D.

N.D. - NOT DEFINED

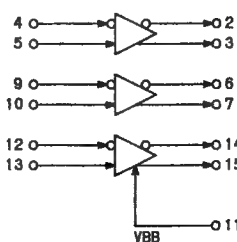
(LOGIC DIAGRAM)



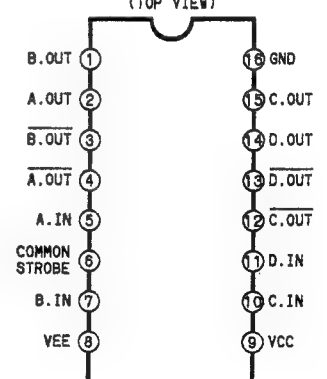
MC10H116 (TRIPLE LINE RECEIVER) (TOP VIEW)



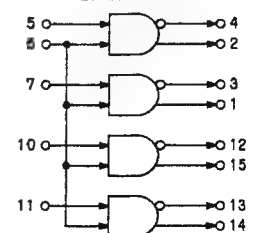
LOGIC DIAGRAM



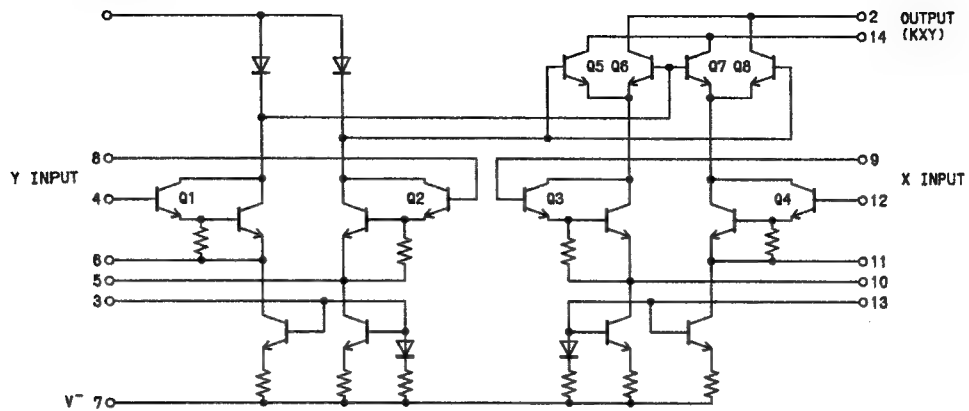
MC10124 (QUAD TTL TO MECL TRANSLATOR) (TOP VIEW)



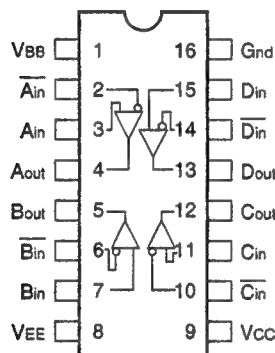
LOGIC DIAGRAM



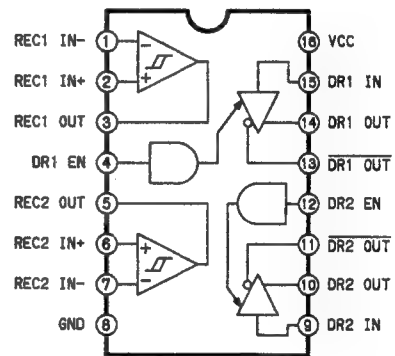
MC1495L
(ANALYSIS AND BASIC OPERATION)



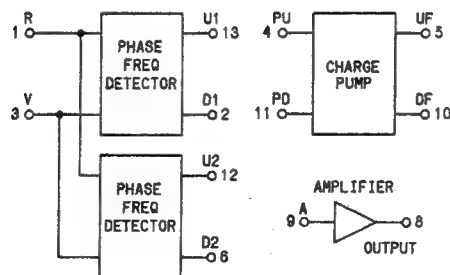
MC10H125(QUAD MECL-TO-TTL TRANSULATOR)



MC34051
(DUAL RS-422/423 TRANSCEIVER)



MC4044

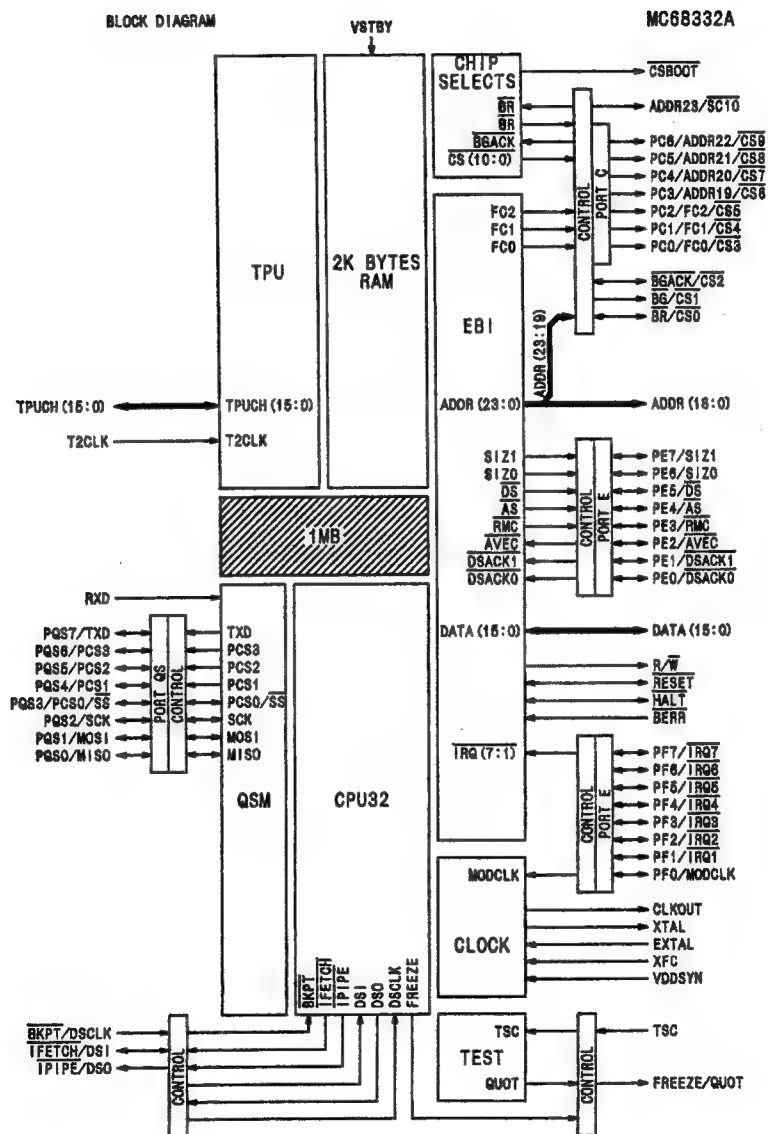


TRUTH TABLE

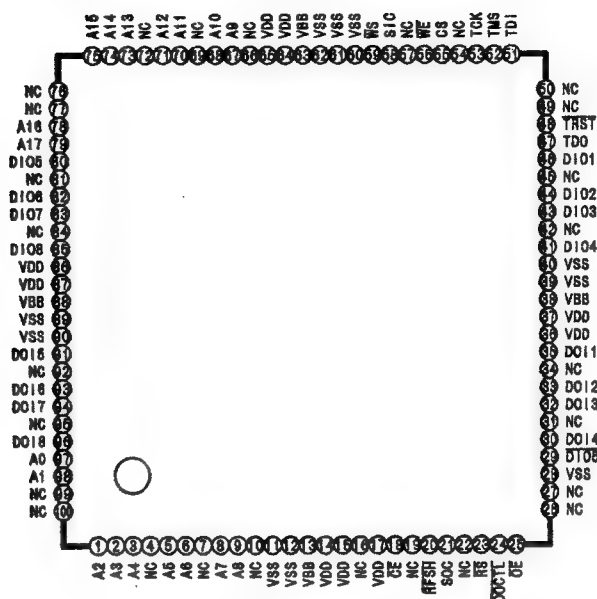
INPUT STATE	INPUT		OUTPUT			
	R	V	U1	D1	U2	D2
1	0	0	x	x	1	1
2	1	0	x	x	0	1
3	1	1	x	x	1	0
4	1	0	x	x	0	1
5	0	0	x	x	1	1
6	1	0	x	x	0	1
7	0	0	x	x	1	1
8	1	0	x	x	0	1
9	0	0	0	1	1	1
10	0	1	0	1	1	1
11	0	0	1	1	1	1
12	0	1	1	1	1	1
13	0	0	1	0	1	1
14	0	1	1	0	1	1
15	0	0	1	0	1	1
16	1	0	1	0	0	1
17	0	0	1	1	1	1

STOP VIEW

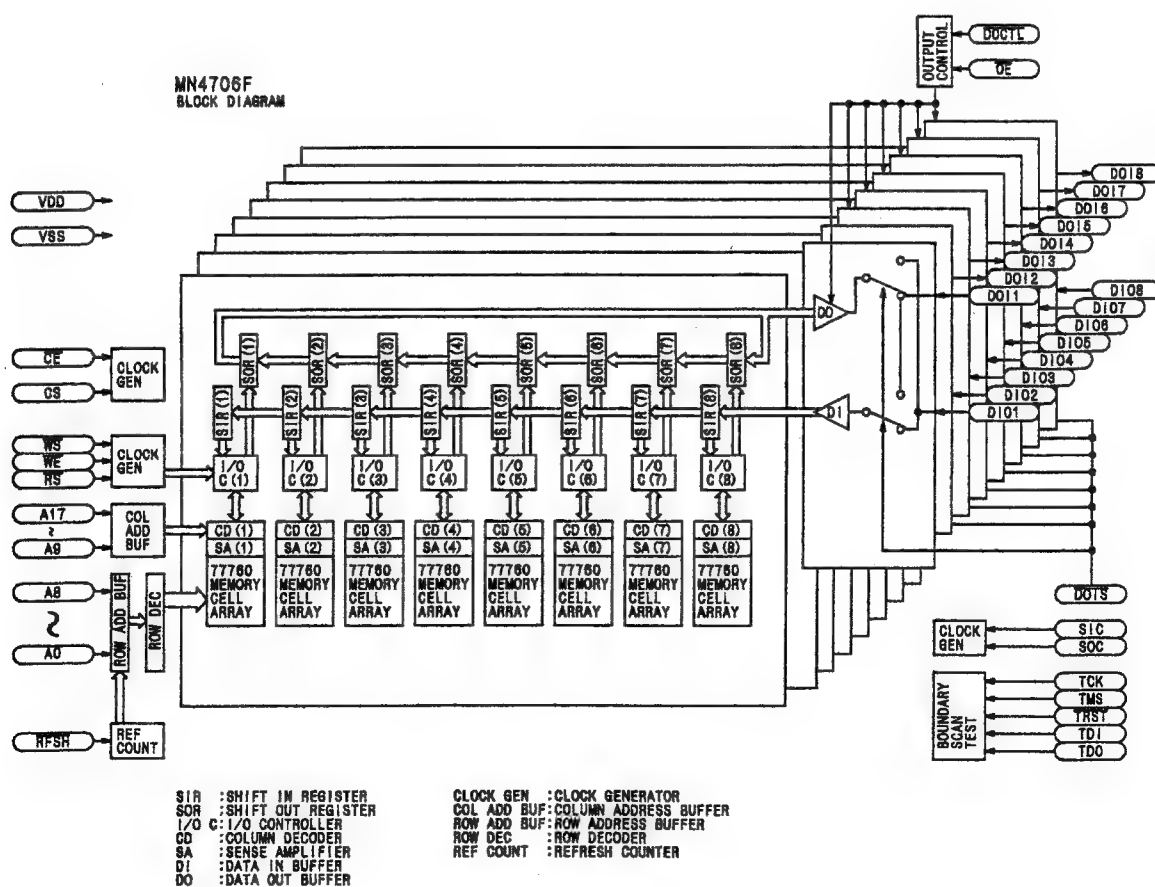




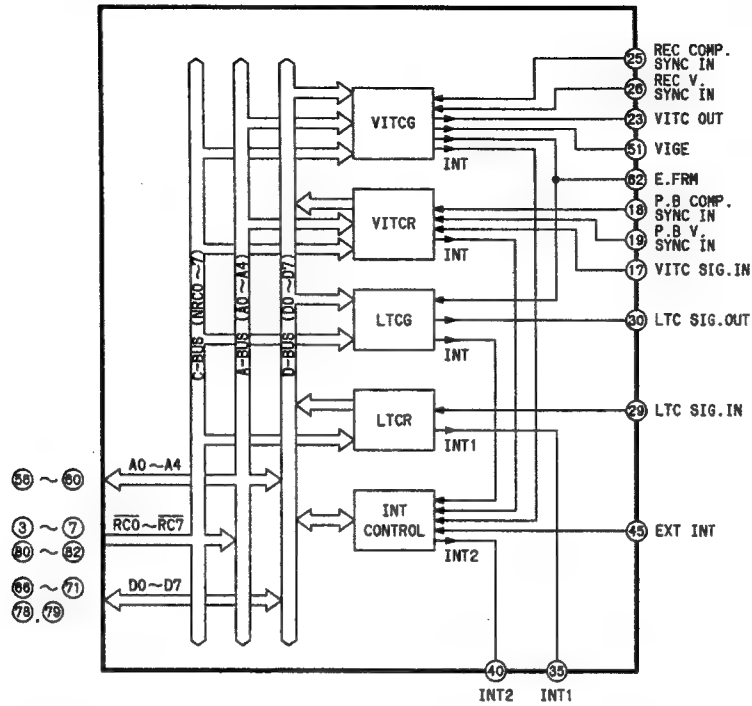
(TOP VIEW)



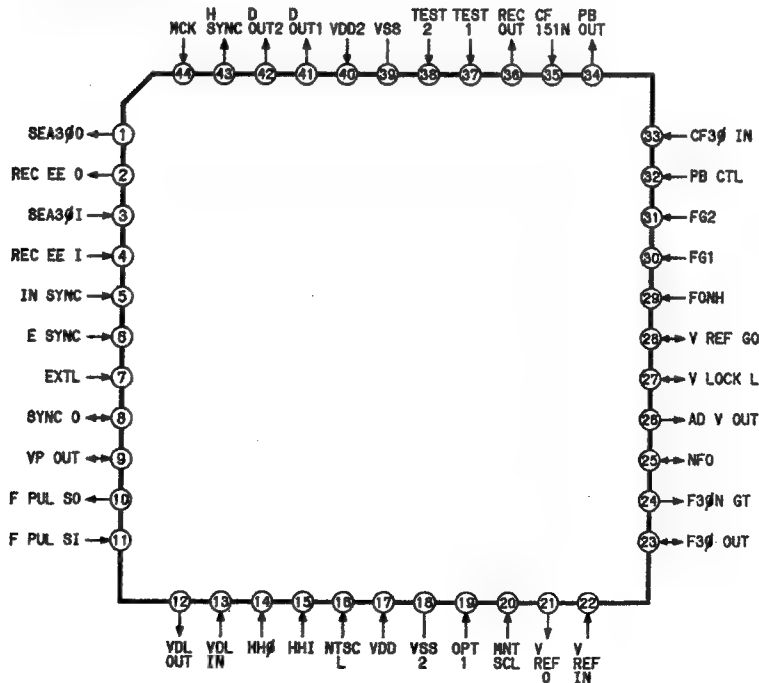
MN4706F
BLOCK DIAGRAM



MN51040
(TIME CODE GENERATOR/READER)

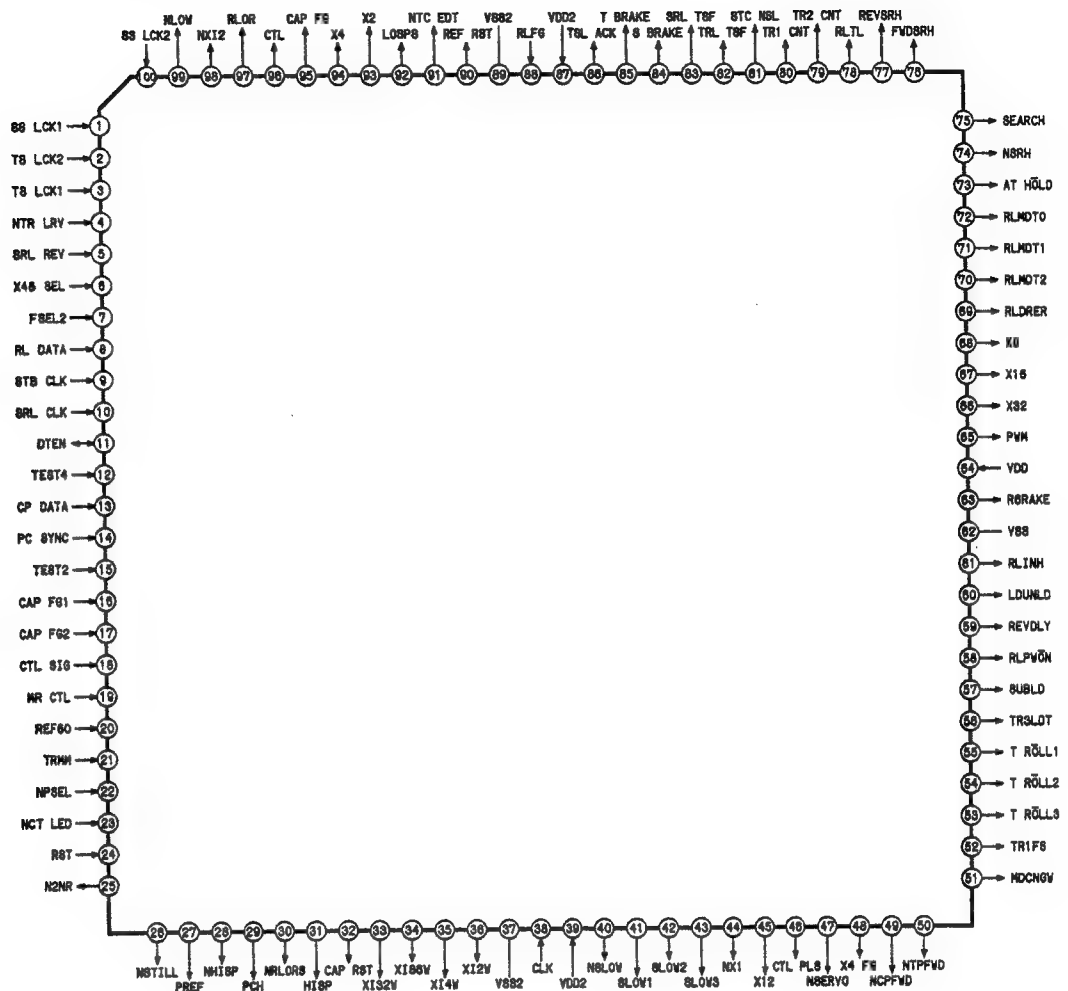


MN53015VZV
(1500 GATES C-MOS GATE ARRAY)

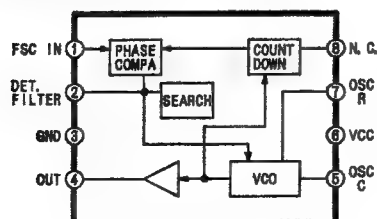


MN53030VYA (CONTROL FOR J06)

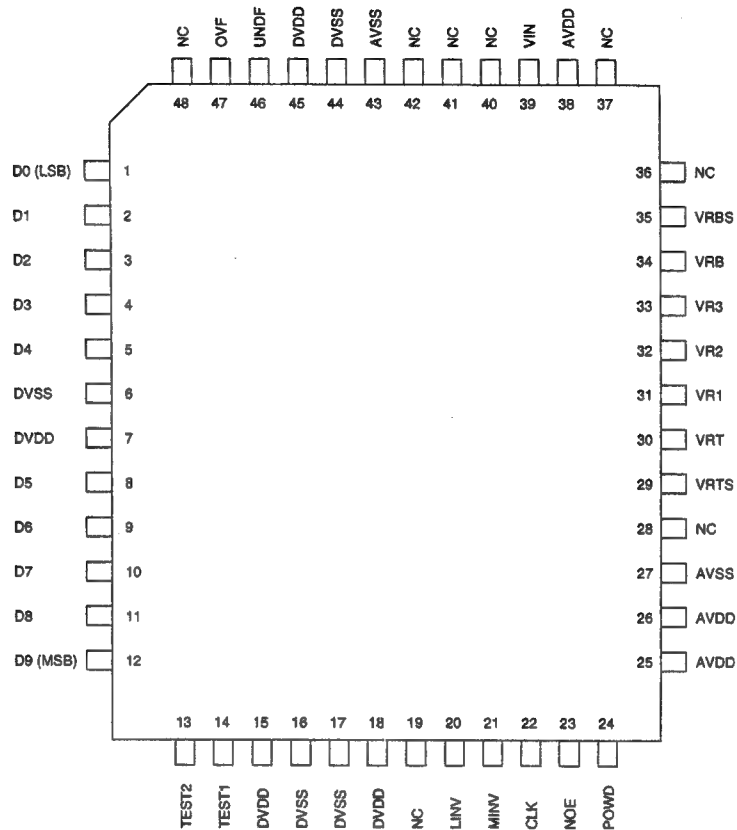
(TOP VIEW)



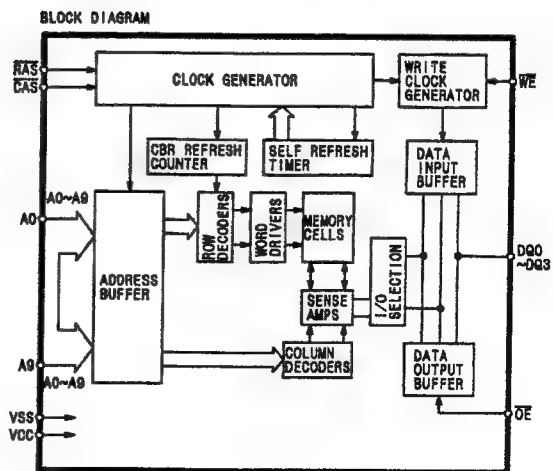
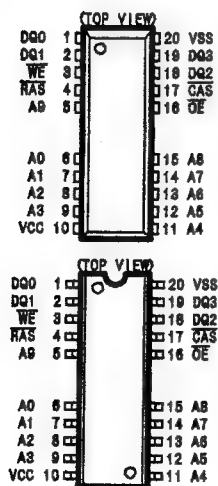
MST003MS (NTSC/PAL 4FSC-MULTIPLEXER)



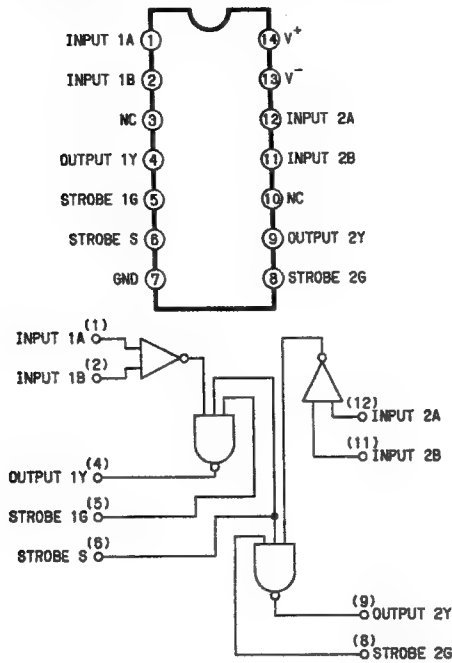
MN6577H



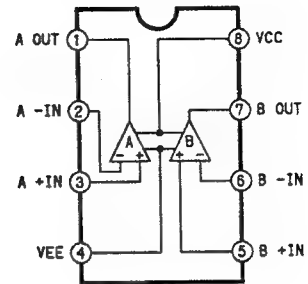
MNS4400CJ7



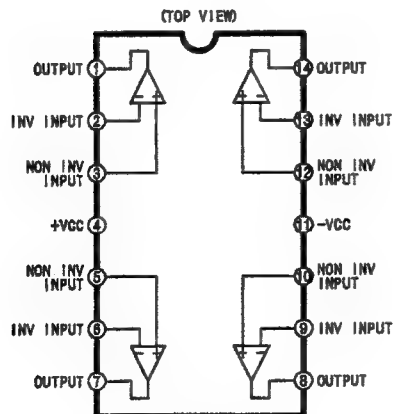
NE521
(HIGH SPEED DUAL DIFFERENTIAL COMPARATOR)



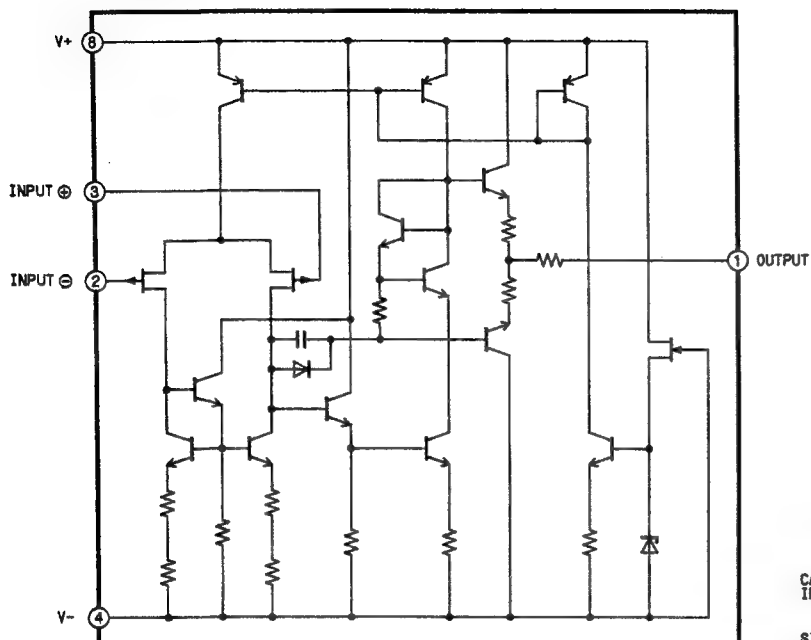
NJM062M
(OPERATIONAL AMPLIFIER)
(TOP VIEW)



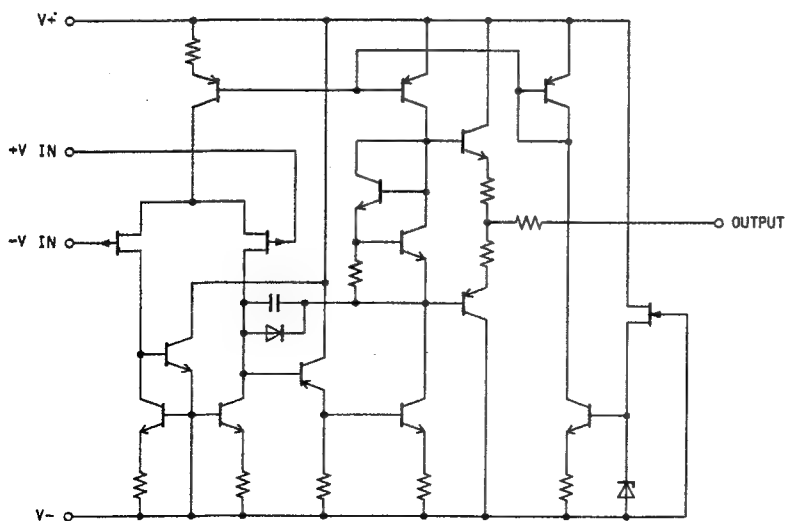
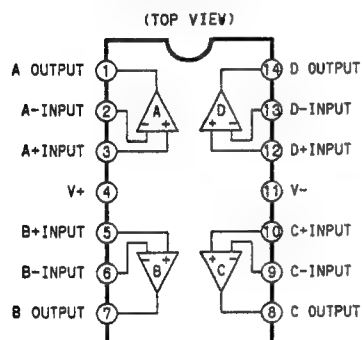
NJM064
(OP AMP, LOW POWER, JFET INPUT)



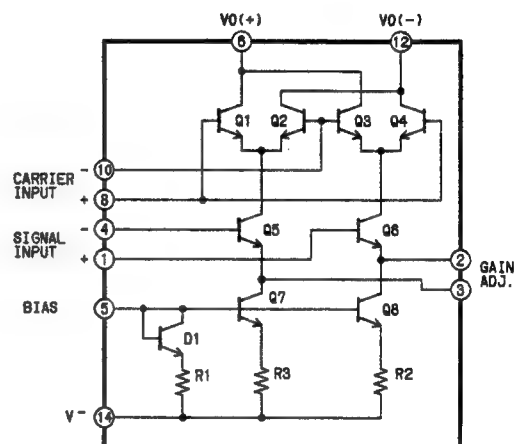
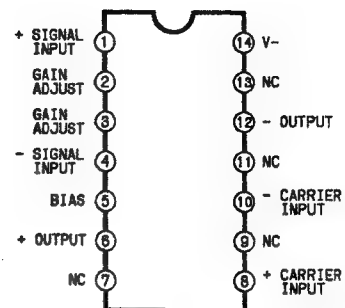
NJM082BM
(OPERATIONAL AMPLIFIER)



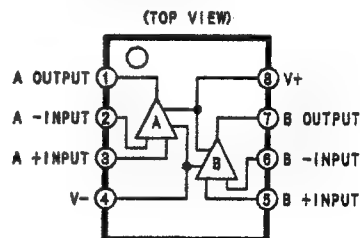
NJM084
(QUAD J-FET INPUT
OPERATIONAL AMPLIFIER)



NJM1498
(BALANCED MODULATOR/DEMODULATOR)

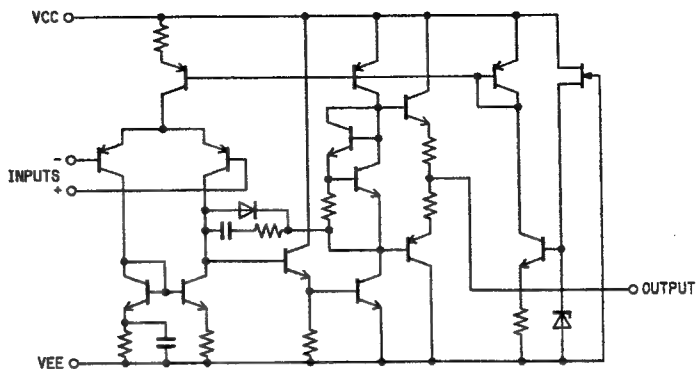
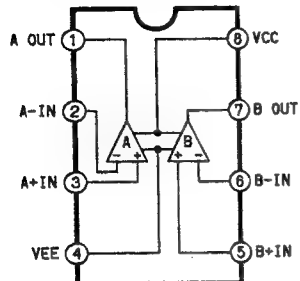


NJM2043MD
(OP AMP)



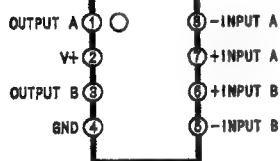
NJM2068MD (OPERATIONAL AMPLIFIER)

(TOP VIEW)

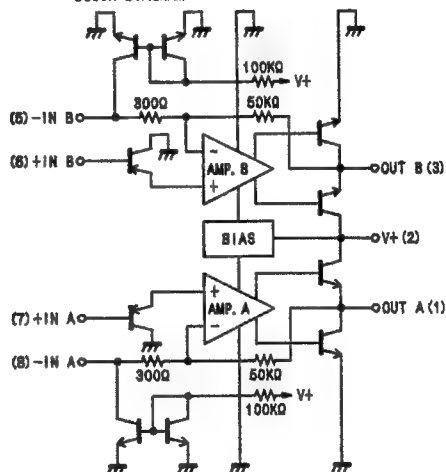


NJM2073N (DUAL LOW POWER OPERATION POWER AMP)

(TOP VIEW)

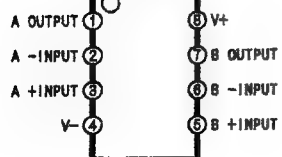


BLOCK DIAGRAM

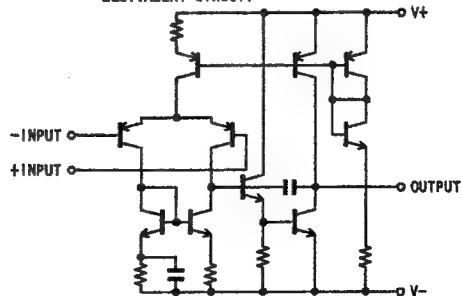


NJM2100MD (OP AMP)

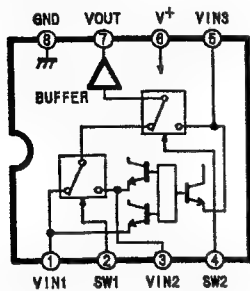
(TOP VIEW)



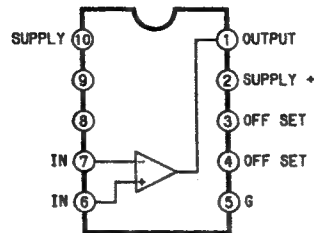
EQUIVALENT CIRCUIT



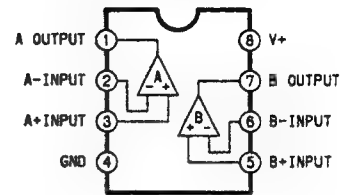
NJM2535M
(8 INPUTS SINGLE VIDEO SWITCH)



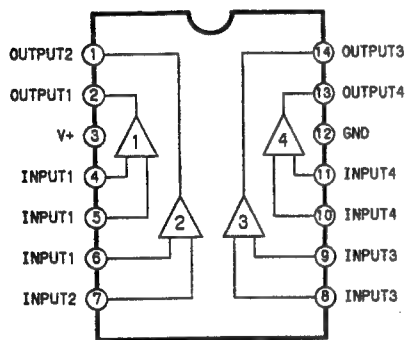
NJM2903M
(VOLTAGE COMPARATOR)
(TOP VIEW)



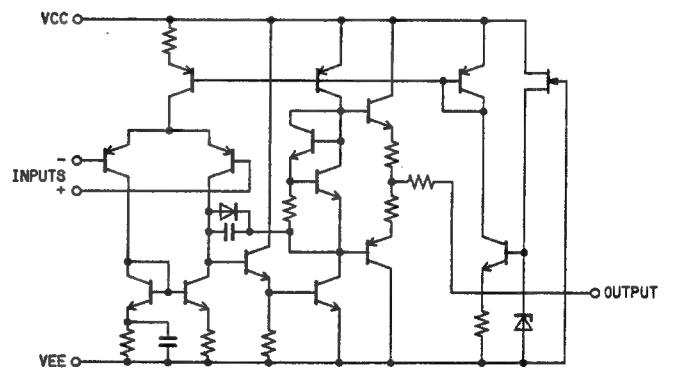
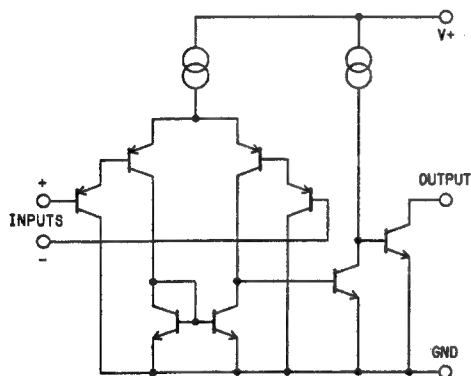
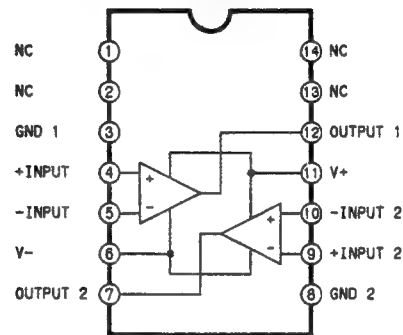
NJM2904M
(DUAL SIGNAL SUPPLY
OPERATIONAL AMPLIFIER)
(TOP VIEW)



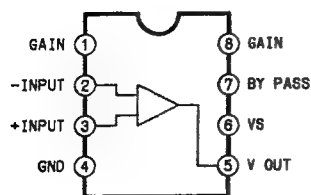
NJM2901
(QUAD VOLTAGE COMPARATOR)
(TOP VIEW)



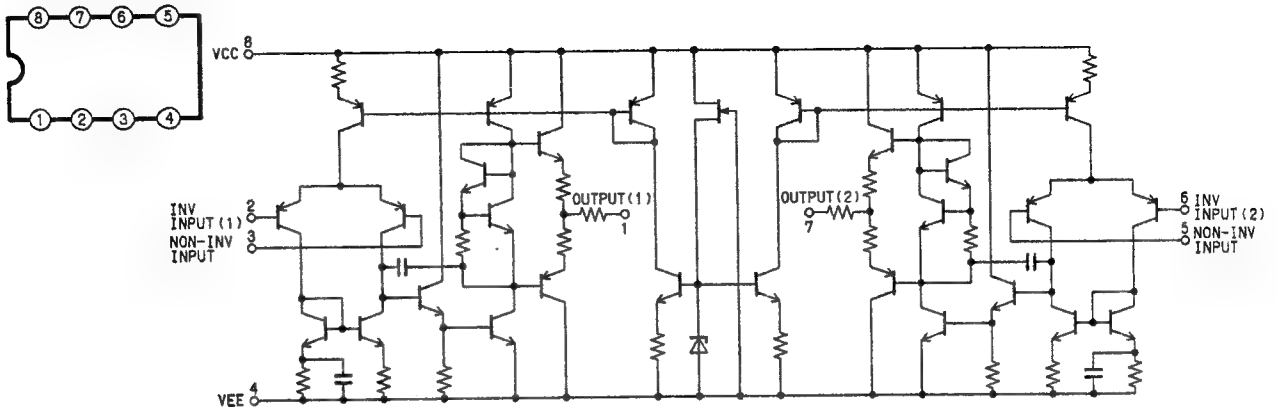
NJM319M
(DUAL VOLTAGE COMPARATOR)
(TOP VIEW)



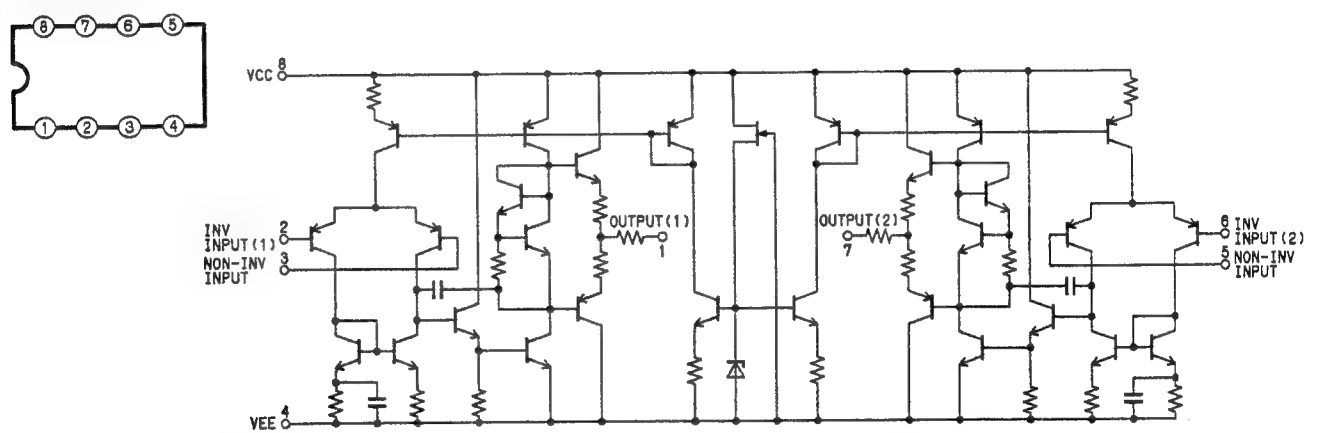
NJM386
(LOW FREQUENCY POWER AMPLIFIER)
(TOP VIEW)



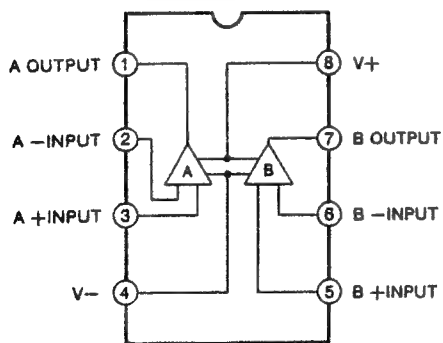
NJM4556MB
(OPERATIONAL AMPLIFIER)



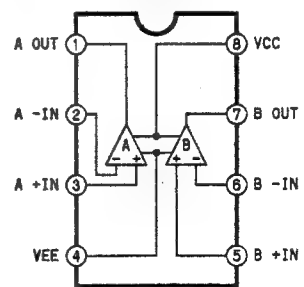
NJM4580
(OPERATIONAL AMPLIFIER)



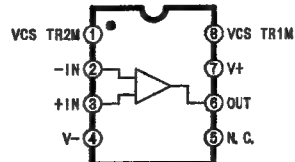
NJM4580ED
(DUAL OP AMP)



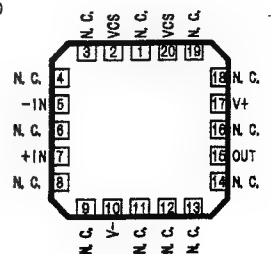
NJM4558
(OPERATIONAL AMPLIFIER)
(TOP VIEW)



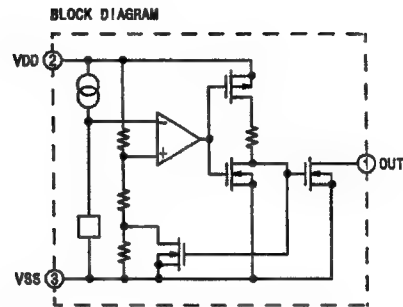
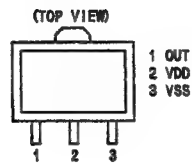
OP177GS
(OP AMP)



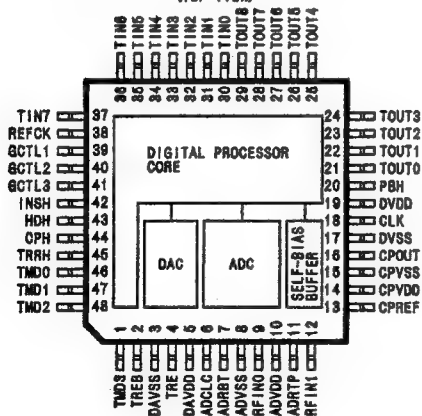
(TOP VIEW)



S80700AN



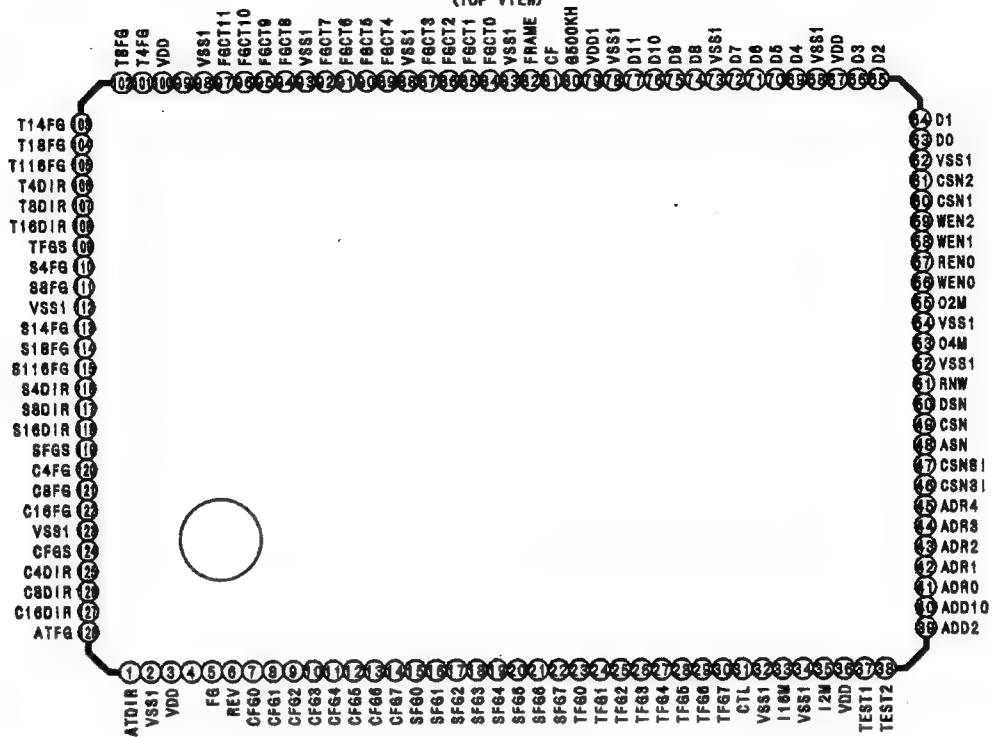
SC371025VFU (FULL DIGITAL VTR SERVO INTERFACE) (TOP VIEW)



- (1) TMD3 : TEST MODE SELECT INPUT
- (2) TBEB : DA CONV. BUFFER OUTPUT
- (4) TRE : DA CONV. OUTPUT
- (7) ADRBT : AD CONV. BOTTOM REFERENCE
- (9) RFINO : AD CONV. INPUT
- (11) ADRTP : AD CONV. TOP REFERENCE
- (12) RFINI : SELF BIAS BUFFER INPUT
- (13) CPREF : SELF BIAS BUFFER INVERTED OUTPUT (FEEDBACK)
- (16) CP OUT : SELF BIAS BUFFER OUT
- (18) CLK : CLOCK INPUT (41.85MHz)
- (20) PBH : POWER DOWN CONTROL L: POWER DOWN
- (38) REFCK : 72 COUNT DOWN CLOCK OUT
- (39) GCTL 1 : GAIN SELECT 1
- (40) GCTL 2 : GAIN SELECT 2
- (41) GCTL 3 : GAIN SELECT 3
- (42) INSH : FILTER RESPONSE TIME SELECT 1
- (43) HDH : FILTER RESPONSE TIME SELECT 2
- (44) GPH : ADC/SELF BIAS BUFFER SELECT SETTING INPUT
- (46) TRRH : DA OUTPUT CODE SELECT

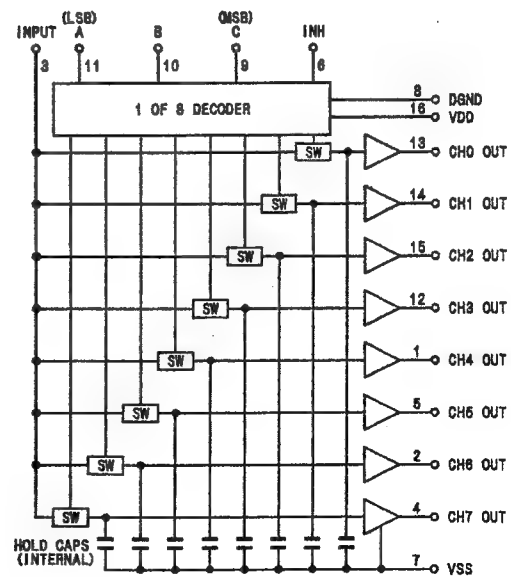
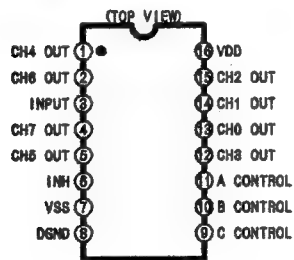
SLA909SF1G
(MOTOR CONTROL GATE ARRAY)

(TOP VIEW)

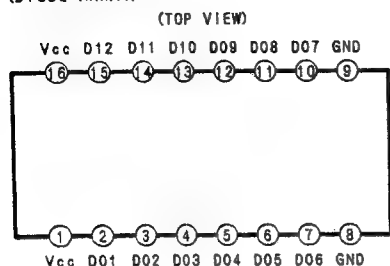


SMPO8FS
(SAMPLE/HOLD AMP)

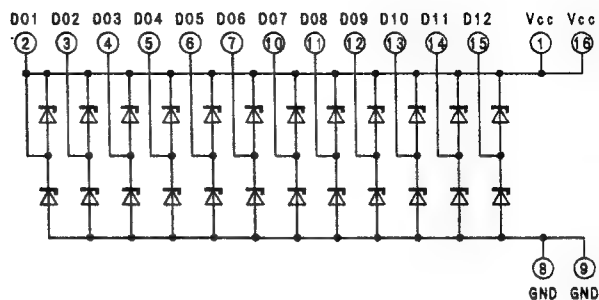
BLOCK DIAGRAM



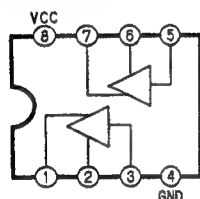
SN74S1051NS
(DIODE ARRAY)



(BLOCK DIAGRAM)

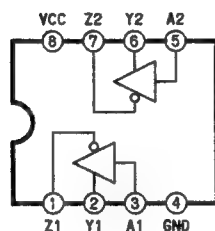


SN75158PS
(40 MA, RS422)

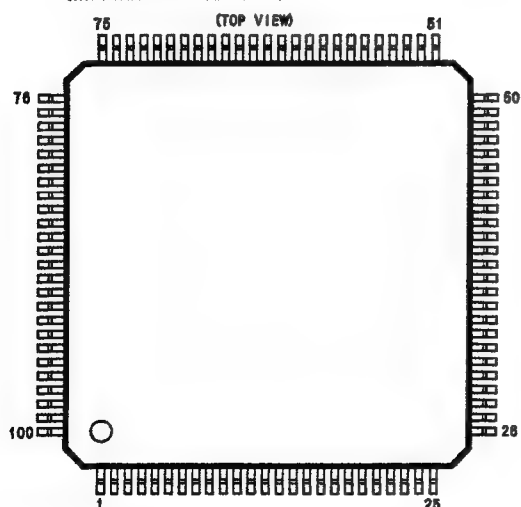


SN75158

(TOP VIEW)

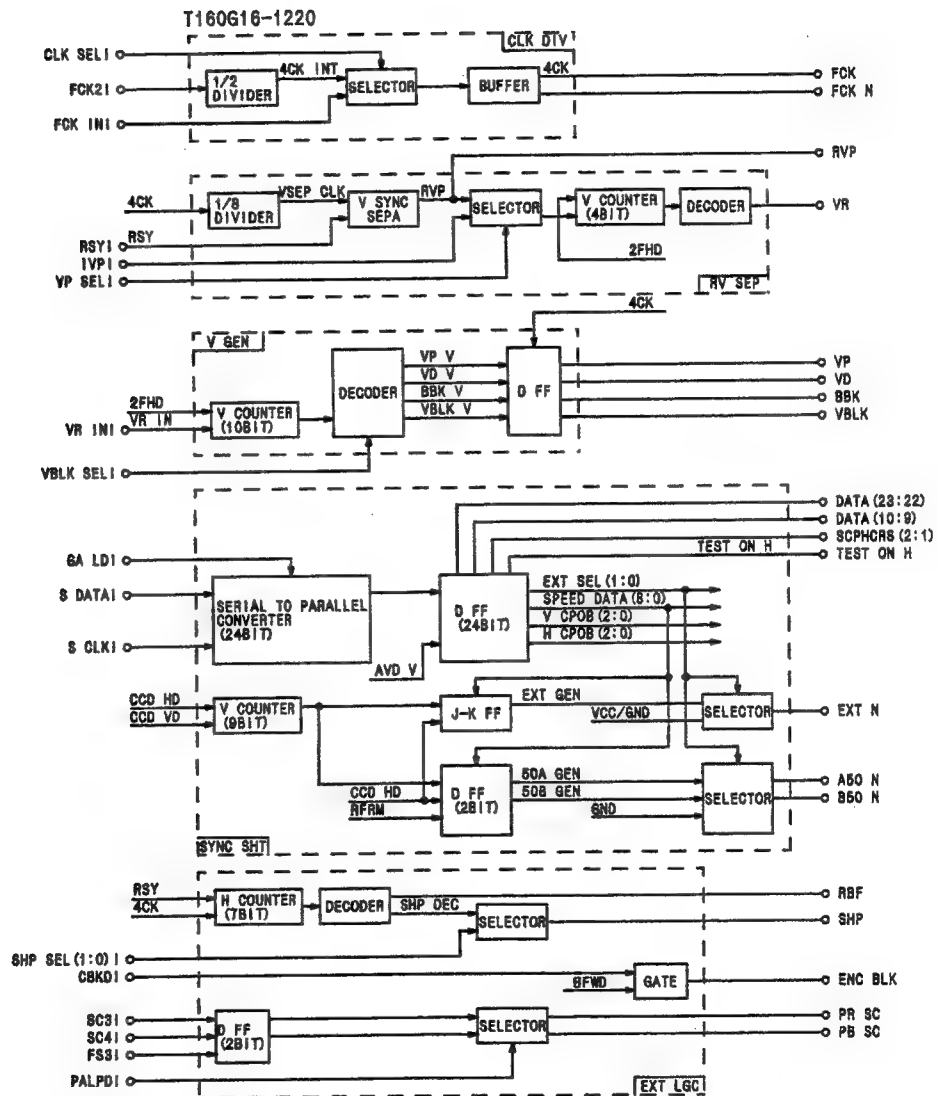


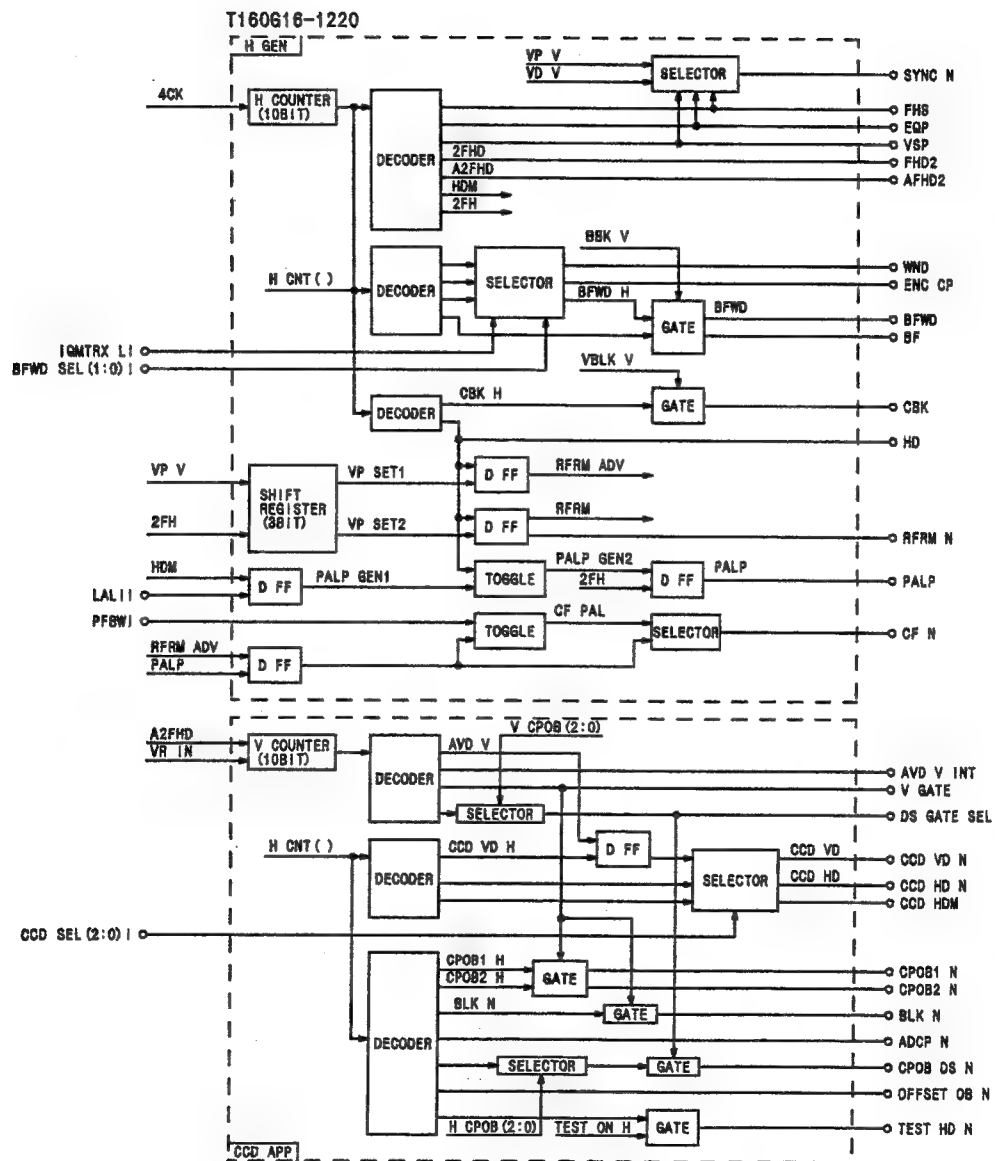
T180G16-1220
(GATE ARRAY-SYNC GENERATOR)



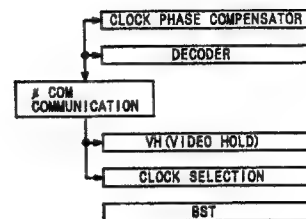
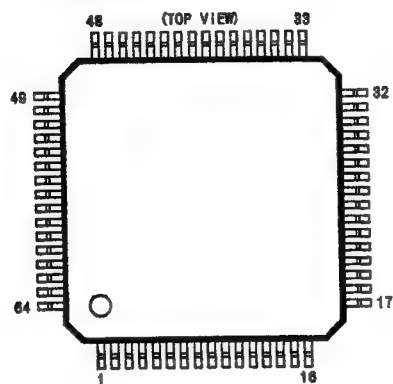
PIN ASSIGNMENT

PIN NO.	PIN NAME	I/O	PIN NO.	PIN NAME	I/O
1	DATA0	OUT	51	DATA22	OUT
2	VSS	—	52	CPOB DS N	OUT
3	VDD	—	53	VDD	—
4	FHS	OUT	54	ADCP N	OUT
5	EDP	OUT	55	CPOB2 N	OUT
6	VSP	OUT	56	CPOB1 N	OUT
7	VR IN1	IN	57	BLK N	OUT
8	VR	OUT	58	VSS	—
9	RVP	OUT	59	ENC BLK	OUT
10	DS GATE SEL	OUT	60	ENC CP	OUT
11	V GATE	OUT	61	SA L01	IN
12	AVD V INT	OUT	62	S CLK1	IN
13	CCD HDM	OUT	63	S DATA1	IN
14	RBF	OUT	64	PR SC	OUT
15	VSS	—	65	VSS	—
16	SHP SEL01	IN	66	PB SC	OUT
17	SHP SEL1	IN	67	EXT N	OUT
18	SHP	OUT	68	BBO N	OUT
19	FCK IN1	IN	69	A60 N	OUT
20	FCK21	IN	70	RFRM N	OUT
21	CLK SEL1	IN	71	PALPD1	IN
22	WND	OUT	72	PALP	OUT
23	TESTON H	OUT	73	CBK01	IN
24	TEST HD N	OUT	74	VD	OUT
25	OFFSET OB N	OUT	75	HD	OUT
26	DATA10	OUT	76	DATA23	OUT
27	BFWD	OUT	77	FCK N	OUT
28	VDD	—	78	VDD	—
29	BFWD SEL01	IN	79	FCK	OUT
30	BFWD SEL1	IN	80	CBK	OUT
31	FHD2	OUT	81	BF	OUT
32	AFHD2	OUT	82	SYNC N	OUT
33	BBK	OUT	83	CCD VD N	OUT
34	VBLK	OUT	84	CCD HD N	OUT
35	VP	OUT	85	RSY1	IN
36	CF N	OUT	86	LAL11	IN
37	TEST IN81	IN	87	PFBW1	IN
38	TEST IN71	IN	88	SCPHCRS1	OUT
39	TEST IN61	IN	89	SCPHCRS2	OUT
40	VSS	—	90	VSS	—
41	TEST IN51	IN	91	IVP1	IN
42	TEST IN41	IN	92	VP SEL1	IN
43	TEST IN31	IN	93	CCD SEL01	IN
44	TEST IN21	IN	94	CCD SEL11	IN
45	TEST IN11	IN	95	CCD SEL21	IN
46	TEST31	IN	96	VBLK SEL1	IN
47	TEST21	IN	97	QMTRX L1	IN
48	TEST11	IN	98	SC41	IN
49	NTSC L1	IN	99	SC31	IN
50	NRST L1	IN	100	FS31	IN





T160G22-1225
(GATE ARRAY)

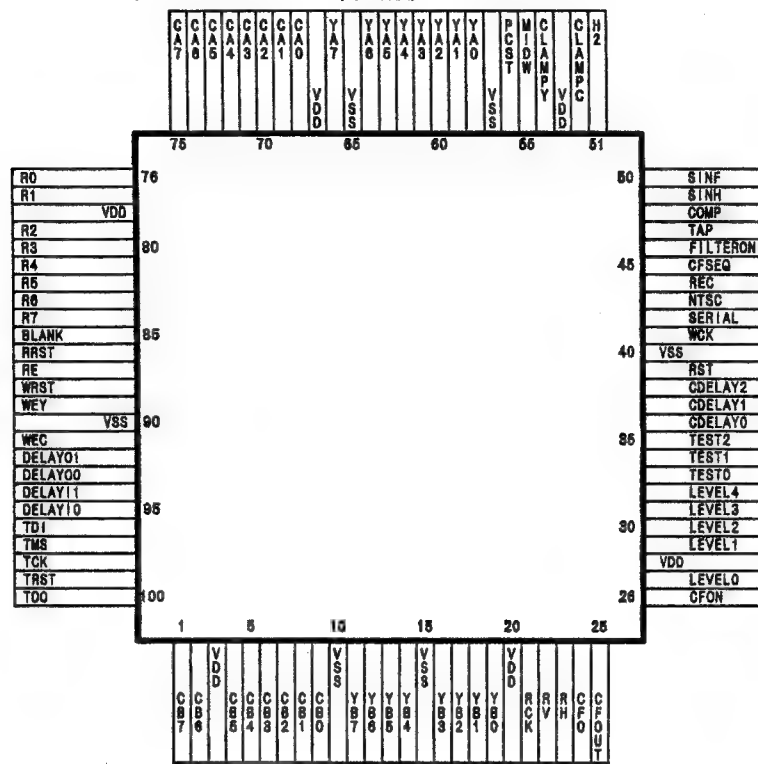


PIN ASSAINGMENT

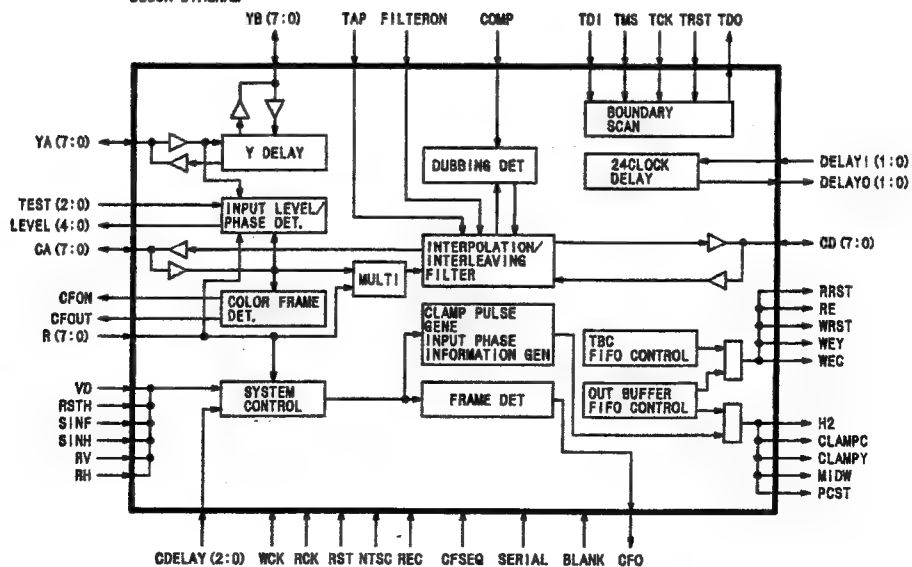
PIN NO.	PIN NAME	I/O	PIN NO.	PIN NAME	I/O
1	VDD	—	33	VSS	—
2	ADD	IN	34	MON 00	OUT
3	AD1	IN	35	MON 01	OUT
4	AD2	IN	36	MON 02	OUT
5	AD3	IN	37	MON 03	OUT
6	AD4	IN	38	MON 04	OUT
7	AD5	IN	39	MON 05	OUT
8	AD6	IN	40	MON 06	OUT
9	CLKTST	IN	41	MON 07	OUT
10	VSS	—	42	VSS	—
11	M CLK	IN	43	TMS	IN
12	SEL CLK AD	OUT	44	TCK	IN
13	SEL CLK DCI	OUT	45	TDI	IN
14	VDD	—	46	TRST	IN
15	VSS	—	47	TDO	OUT
16	PBCLK	IN	48	RECSTR	IN
17	PBDAT 1	IN	49	SBSTR	IN
18	PBDAT 0	OUT	50	DEDR 10	IN
19	VSS	—	51	DEDR 11	IN
20	RST	IN	52	DEDR 12	IN
21	TEST	IN	53	DEDR 13	IN
22	RCA	IN	54	DEDR 00	OUT
23	RCB	IN	55	DEDR 01	OUT
24	HID	IN	56	DEDR 02	OUT
25	FRP	IN	57	DEDR 03	OUT
26	VDD	—	58	VDD	—
27	PBH	IN	59	S CS	IN
28	PWM	OUT	60	S CLK	IN
29	MON MD0	IN	61	S DATA	I/O
30	MON MD1	IN	62	CLK18	IN
31	MON MD2	IN	63	DREC	IN
32	MON MD3	IN	64	VSS	—

T160641-1437
(GATE ARRAY (TBC))

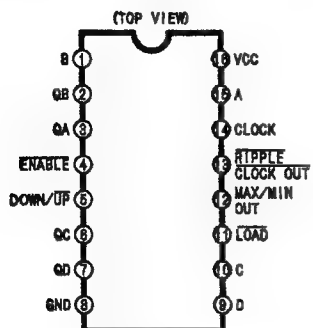
(TOP VIEW)



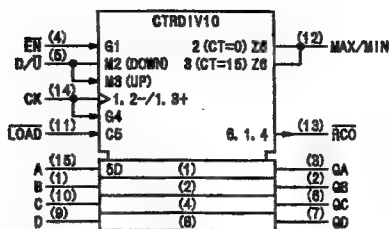
BLOCK DIAGRAM



T74HCT191A
16 BIT BINARY UP/DOWN COUNTER



LOGIC DIAGRAM

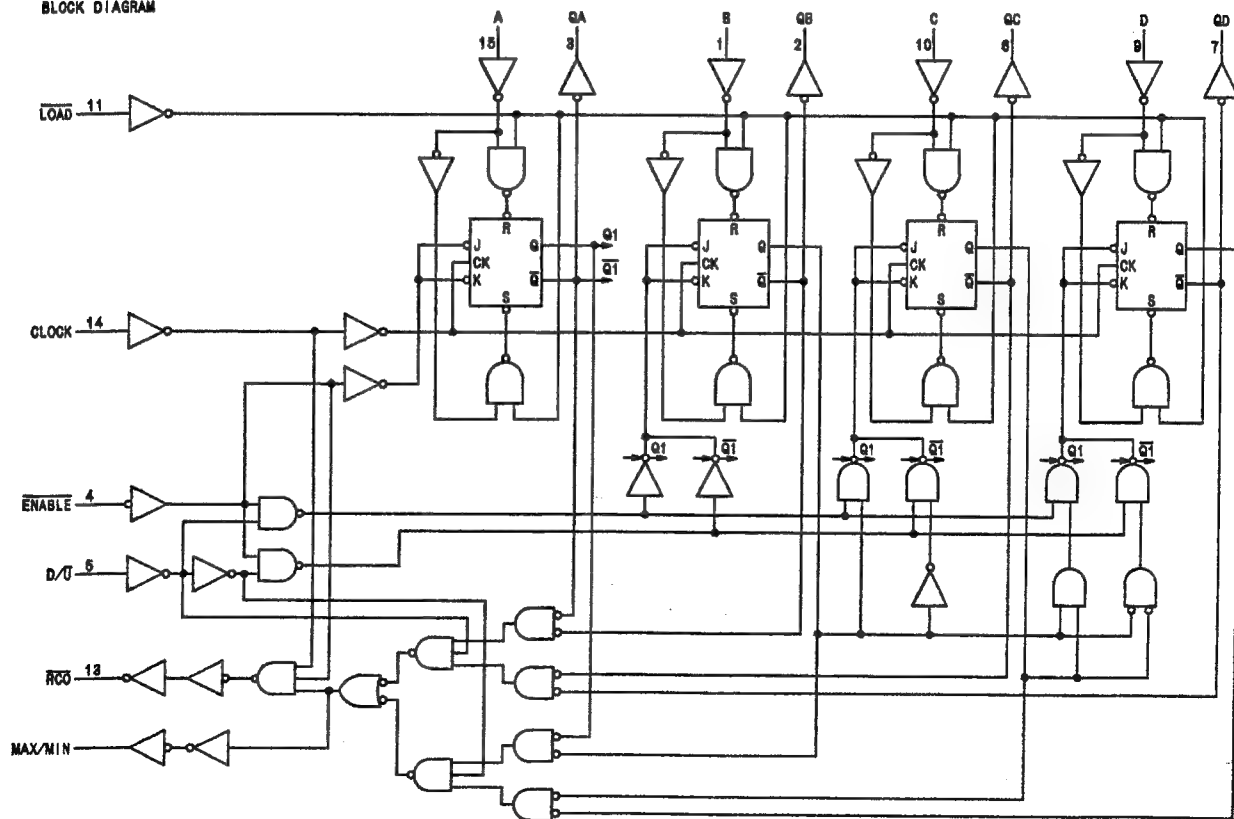


TRUTH TABLE

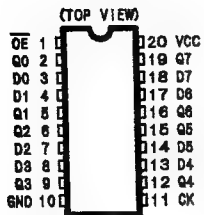
INPUTS				OUTPUTS				FUNCTION
LOAD	ENABLE	D/U	CLOCK	QA	QB	QC	QD	
L	X	X	X	a	b	c	d	PRESET DATA
H	L	L	X					UP COUNT
H	L	H	X					DOWN COUNT
H	H	X	X					NO CHANGE
H	X	X	X					NO CHANGE

NOTE: X: DON'T CARE
a~d: INPUT LEVEL INTO A~D

BLOCK DIAGRAM



T74HCT374A
(OCTAL D-TYPE FLIP FLOP WITH 3 STATE OUTPUT)

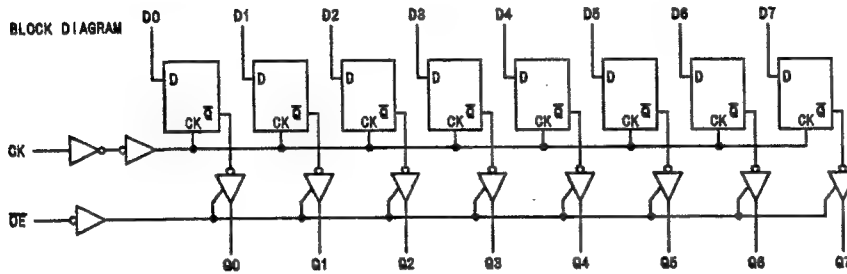
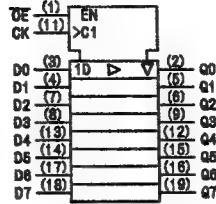


TRUTH TABLE

INPUTS			OUTPUTS	
OE	CK	D	Q (T374A)	Q (T534A)
H	X	X	Z	Z
L	X	X	Qn	Qn
L	L	L	L	H
L	L	H	H	L

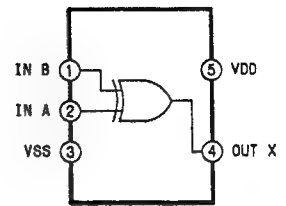
X: DON'T CARE
Z: HIGH IMPEDANCE
Qn (Qn): NOT VARIABLE

LOGIC DIAGRAM



TC4830F
(EXCLUSIVE-OR GATE)

(TOP VIEW)

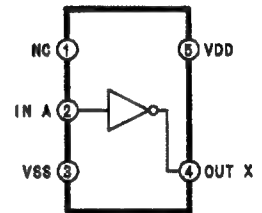


TRUTH TABLE

INPUT	OUTPUT
A B X	
L L L	
L H H	
H L H	
H H L	

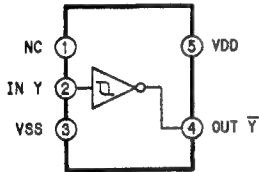
TC4889F
(INVERTER GATE)

(TOP VIEW)

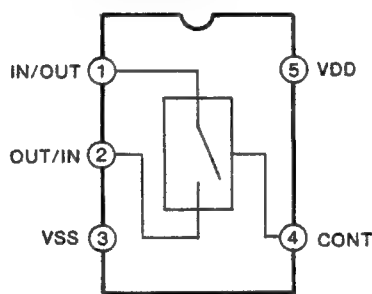


TC48584F
(SCHMITT TRIGGER)

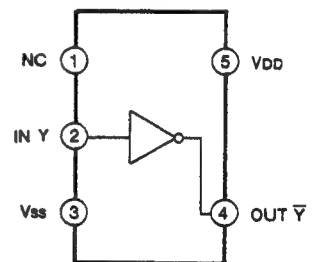
(TOP VIEW)



TC4S66F
(BILATERAL SWITCH)

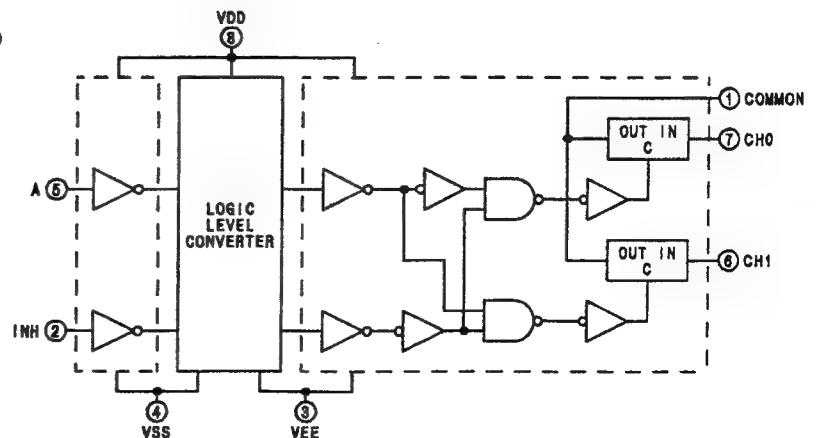
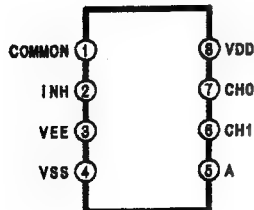


TC7S04F
(C-MOS INVERTER)

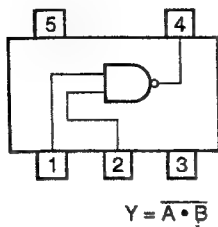


TC4W53FU
(2-CHANNEL MULTIPLEXER/DEMULTIPLEXER)

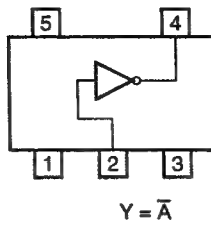
(TOP VIEW)



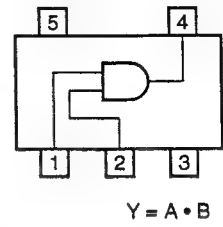
TC7S00F(2 INPUT NAND GATE)



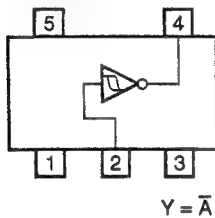
TC7S04F(INVERTER)



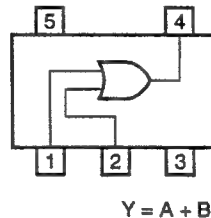
TC7S08F(2 INPUT AND GATE)



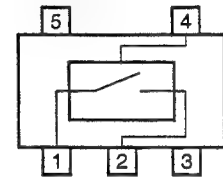
TC7S14F(SCHMITT INVERTER)



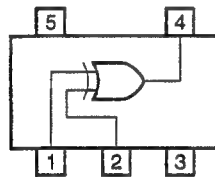
TC7S32F(2 INPUT OR GATE)



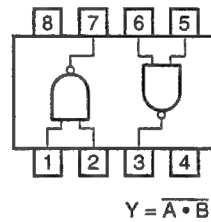
TC7S66F(ANALOG SWITCH)



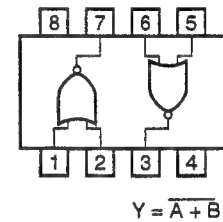
TC7S86F(2 INPUT EXCLUSIVE OR GATE)



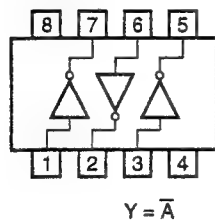
TC7W00F(DUAL 2 INPUT NAND GATE)



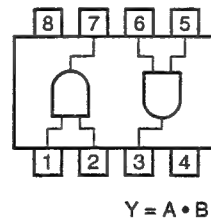
TC7W02F(DUAL 2 INPUT NOR GATE)



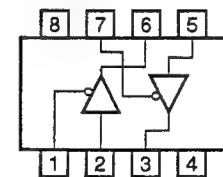
TC7W04F(TRIPLE INVERTER)



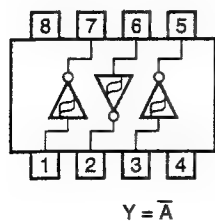
TC7W08F(DUAL 2 INPUT AND GATE)



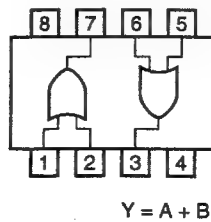
TC7W125FU(DUAL 3-STATE BUFFER)



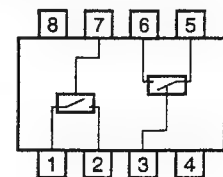
TC7W14F(TRIPLE SCHMITT INVERTER)



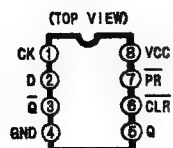
TC7W32F(DUAL 2 INPUT OR GATE)



TC4W66F(DUAL ANALOG SWITCH)



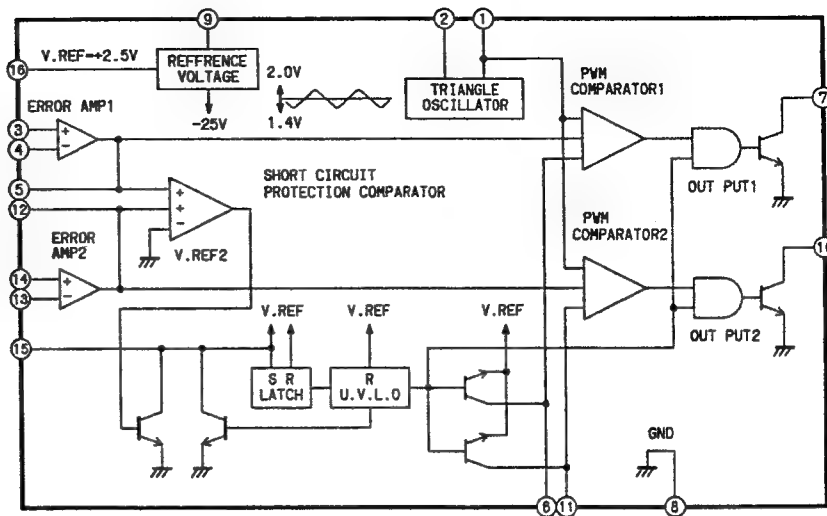
TC7W74F
(D TYPE FLIP FLOP WITH PRESET AND CLEAR)



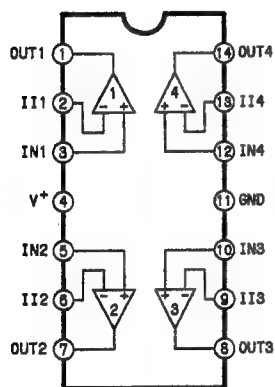
LOGIC BLOCK DIAGRAM



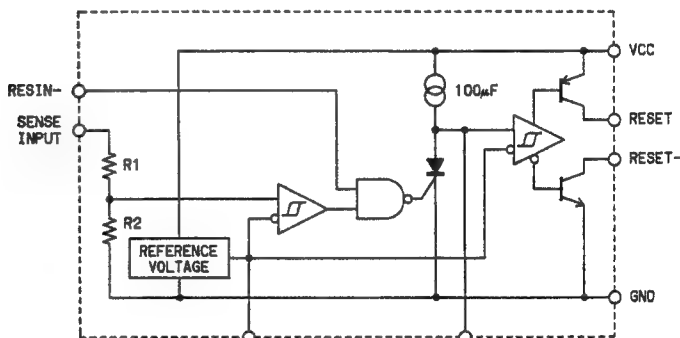
TL1451CNS
(DUAL SWITCHING REGULATOR CONTROLLER)



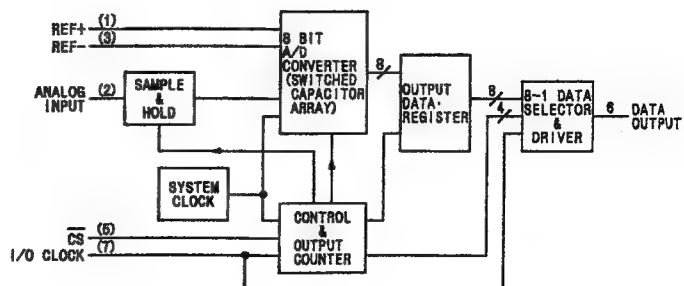
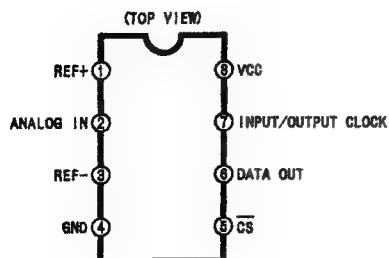
TL084
(OPERATIONAL AMPLIFIER)
(TOP VIEW)



TL7705
(SUPPLY VOLTAGE SUPERVISOR CIRCUIT)

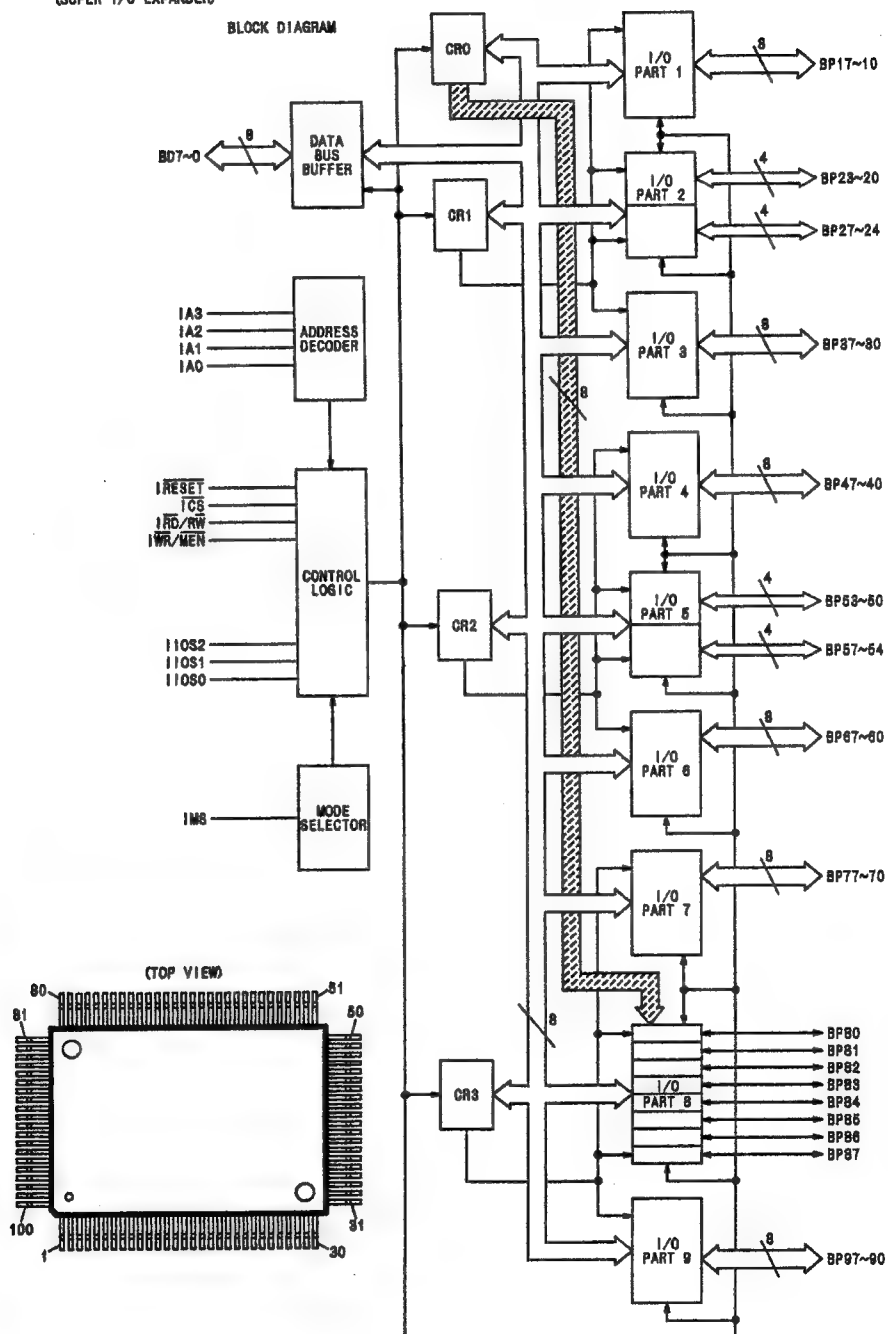


TLC548C/549C
(8 BIT BINARY COMPATIBLE A/D CONVERTER)

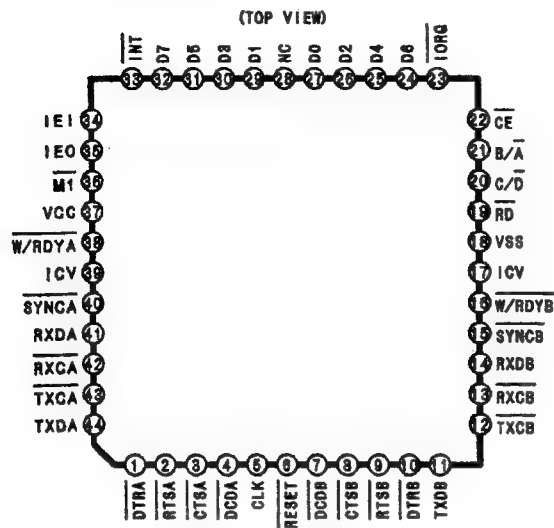


TE7751
(SUPER I/O EXPANDER)

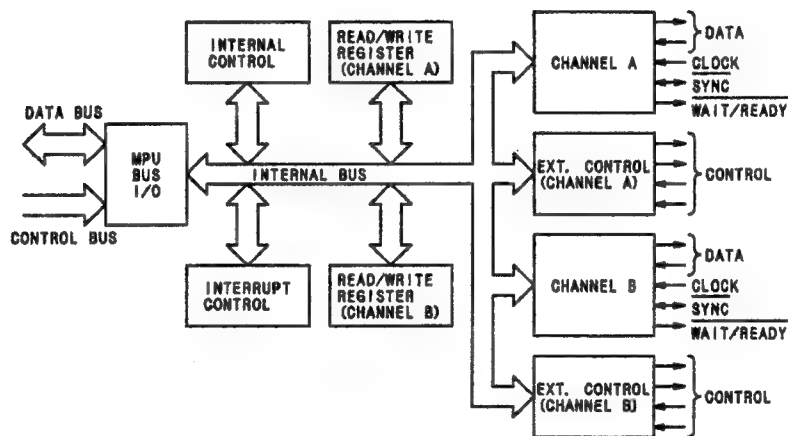
BLOCK DIAGRAM



TMP284C43AF-8
(SERIAL INPUT/OUTPUT CONTROLLER)



FUNCTION BLOCK DIAGRAM

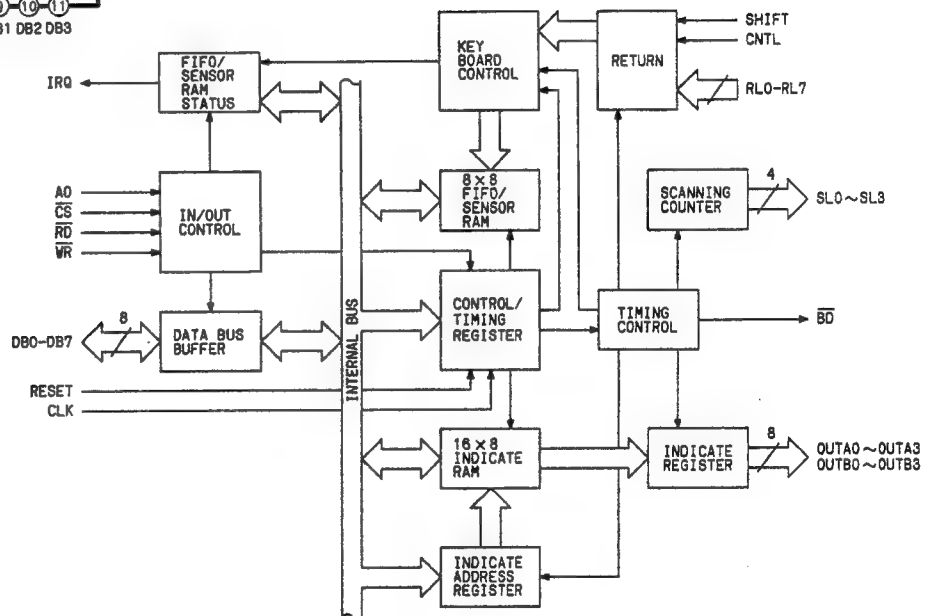
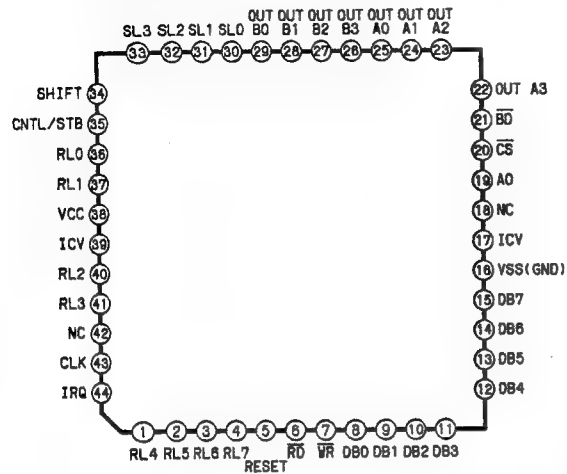


I/O CHART

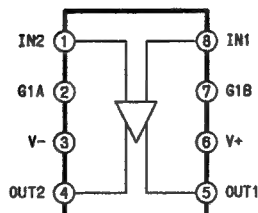
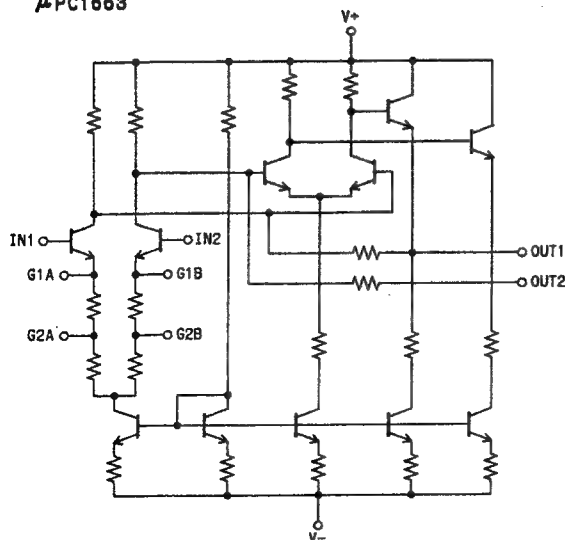
PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	DTRA	O	DATA TERMINAL READY	40	SYNCA	I/O	SYNC
10	DTRB	O	DATA TERMINAL READY	15	SYNCB	I/O	SYNC
2	RTSA	O	TRANSMIT REQUEST	38	W/RDYA	O	WAIT/READY A, B
9	RTSB	O	TRANSMIT REQUEST	16	W/RDYB	O	WAIT/READY A, B
3	CTSA	I	TRANSMIT ABLE	17	ICV	-	VCC OR OPEN
8	CTSB	I	TRANSMIT ABLE	18	VSS	POWER	OV
4	DCDA	I	DATA CARRIER DETECT	19	RD	I	READ SIGNAL
7	DCDB	I	DATA CARRIER DETECT	20	C/D	I	COMMAND/DATA SELECT
5	CLK	I	SINGLE PHASE CLOCK	21	B/A	I	CHANNEL SELECT
6	RESET	I	RESET	22	CE	I	CHIP ENABLE
44	TXDA	O	SERIAL TRANSMIT DATA	23	TORQ	I	I/O REQUEST
11	TXDB	O	SERIAL TRANSMIT DATA	24~27	D0~D7	I/O	8 BIT BUS
43	TXCA	I	TRANSMIT CLOCK	28~32	D0~D7	I/O	8 BIT BUS
12	TXCB	I	TRANSMIT CLOCK	33	INT	O	INTERRUPT REQUEST
42	RXCA	I	RECEIVE CLOCK	34	IEI	I	INTERRUPT INABLE INPUT
13	RXCB	I	RECEIVE CLOCK	35	IEO	O	INTERRUPT INABLE OUTPUT
41	RXDA	I	SERIAL RECEIVE DATA	36	M1	I	MACHINE CYCLE 1
14	RXDB	I	SERIAL RECEIVE DATA	37	VCC	POWER	+5V

TMP82C79F2

(CMOS PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE)

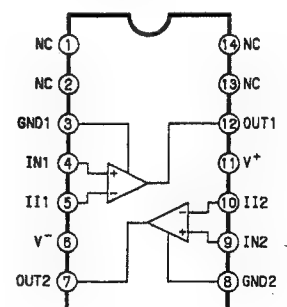


μPC1663

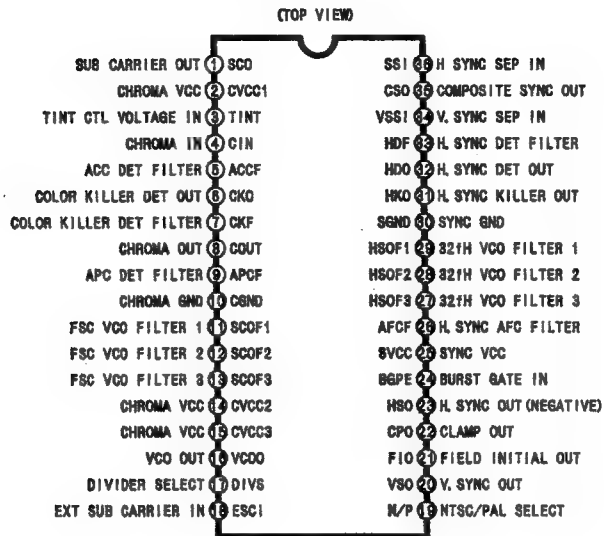


UPC319

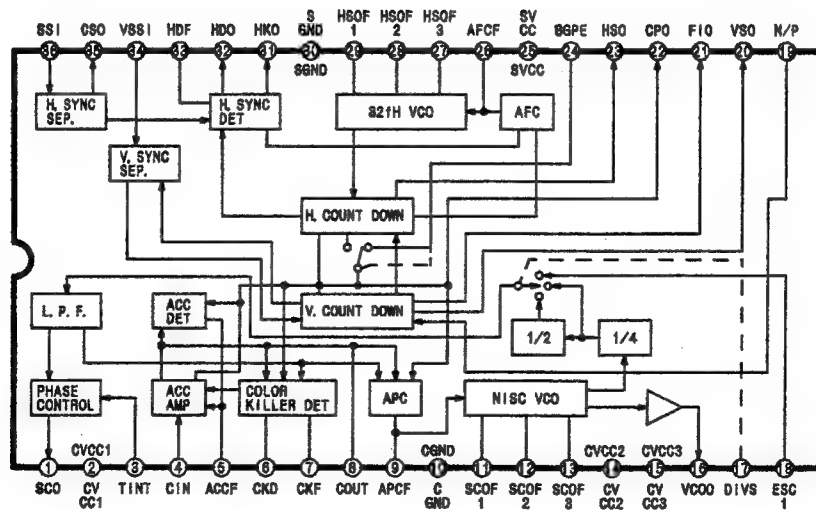
(DUAL COMPARATOR)
(TOP VIEW)



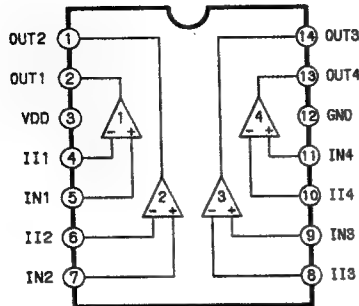
UPC1862GS
VIDEO SIGNAL PROCESSOR CLOCK GENERATOR



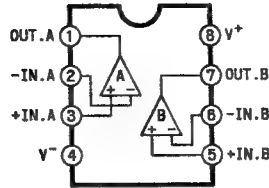
BLOCK DIAGRAM



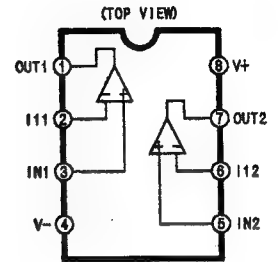
UPC339
(OPERATIONAL AMPLIFIER)
(TOP VIEW)



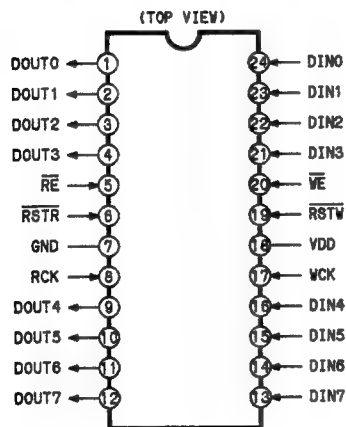
UPC4082
(OPERATIONAL AMPLIFIER)
(TOP VIEW)



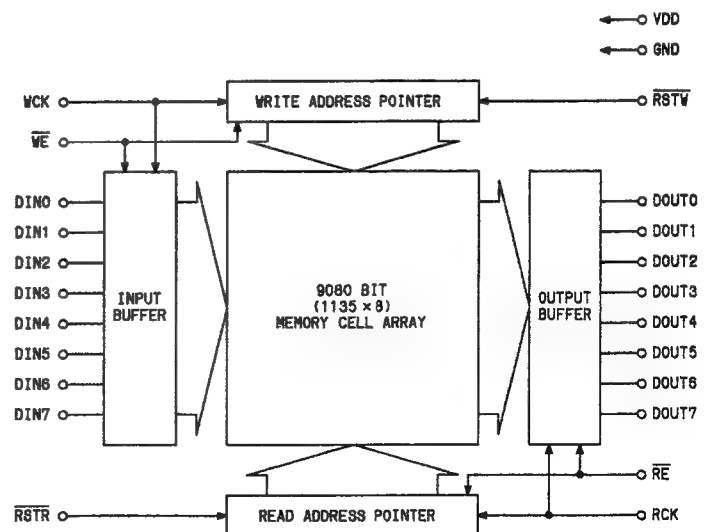
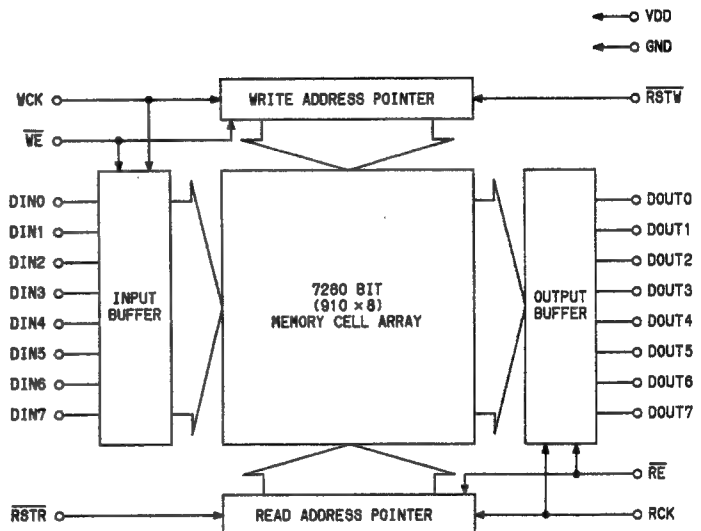
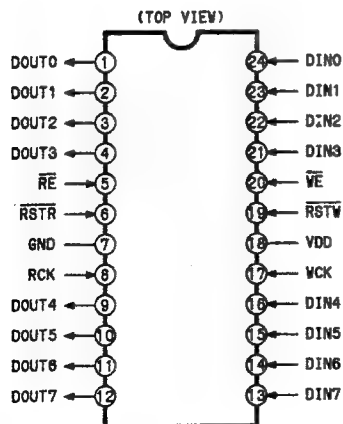
UPC4556
(OP AMP, WIDE BAND)
(TOP VIEW)



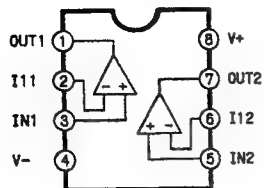
μPD421016 (FIFO 1H DELAY)



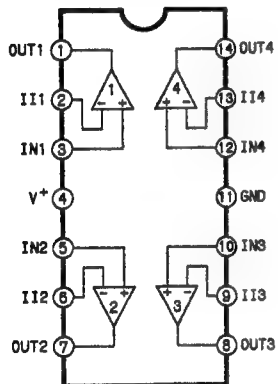
μPD421026 (FIFO 1H DELAY)



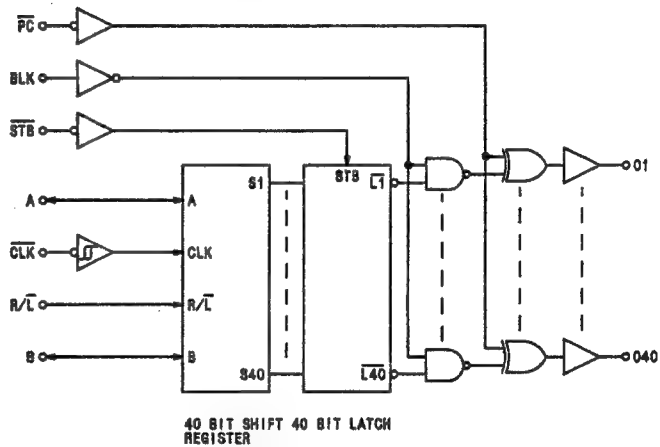
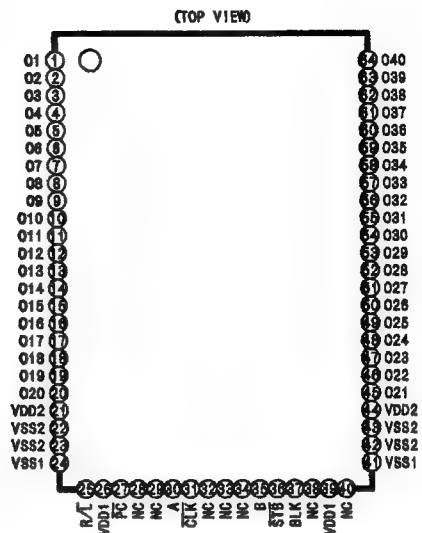
UPC4558
(OPERATIONAL AMPLIFIER)
(TOP VIEW)



UPC4741
(OPERATIONAL AMPLIFIER)
(TOP VIEW)

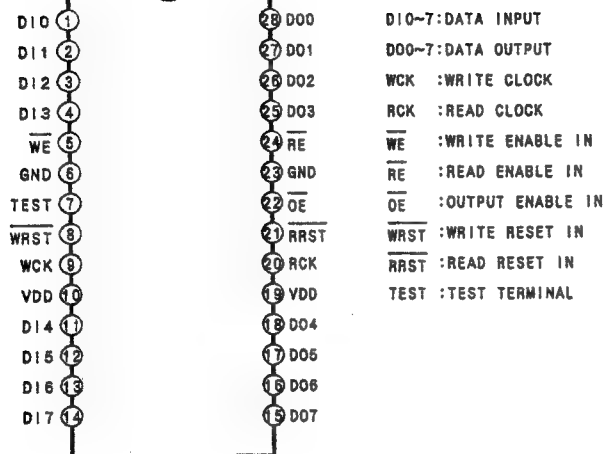


APD163106F
(DISPLAY TUBE DRIVER)

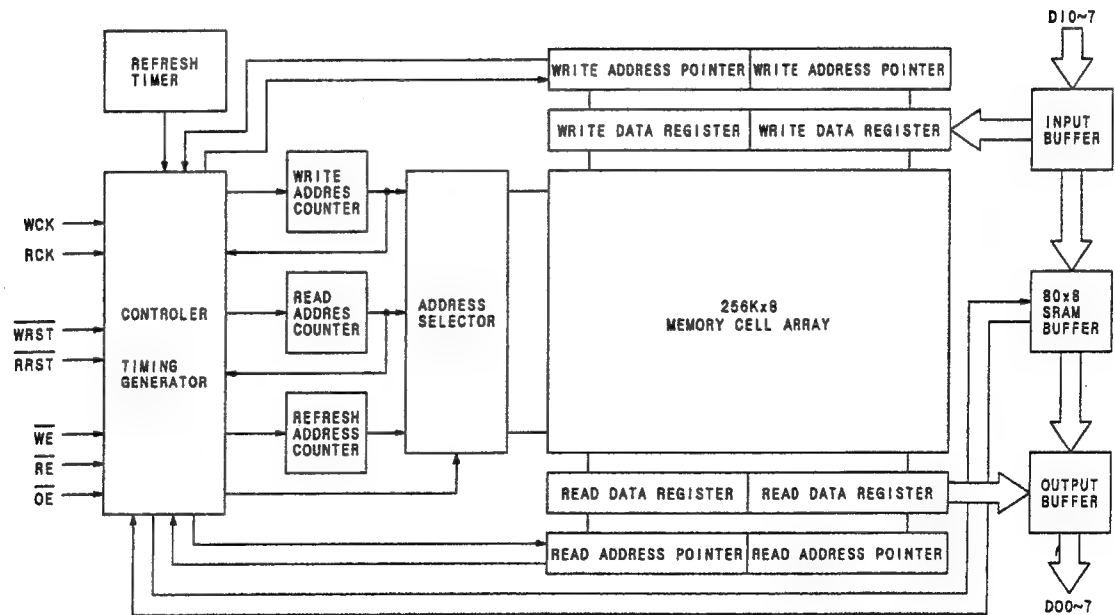


UPD42280
(2M BIT FIELD BUFFER)

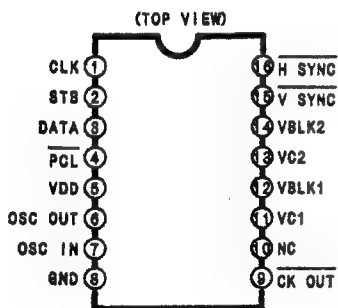
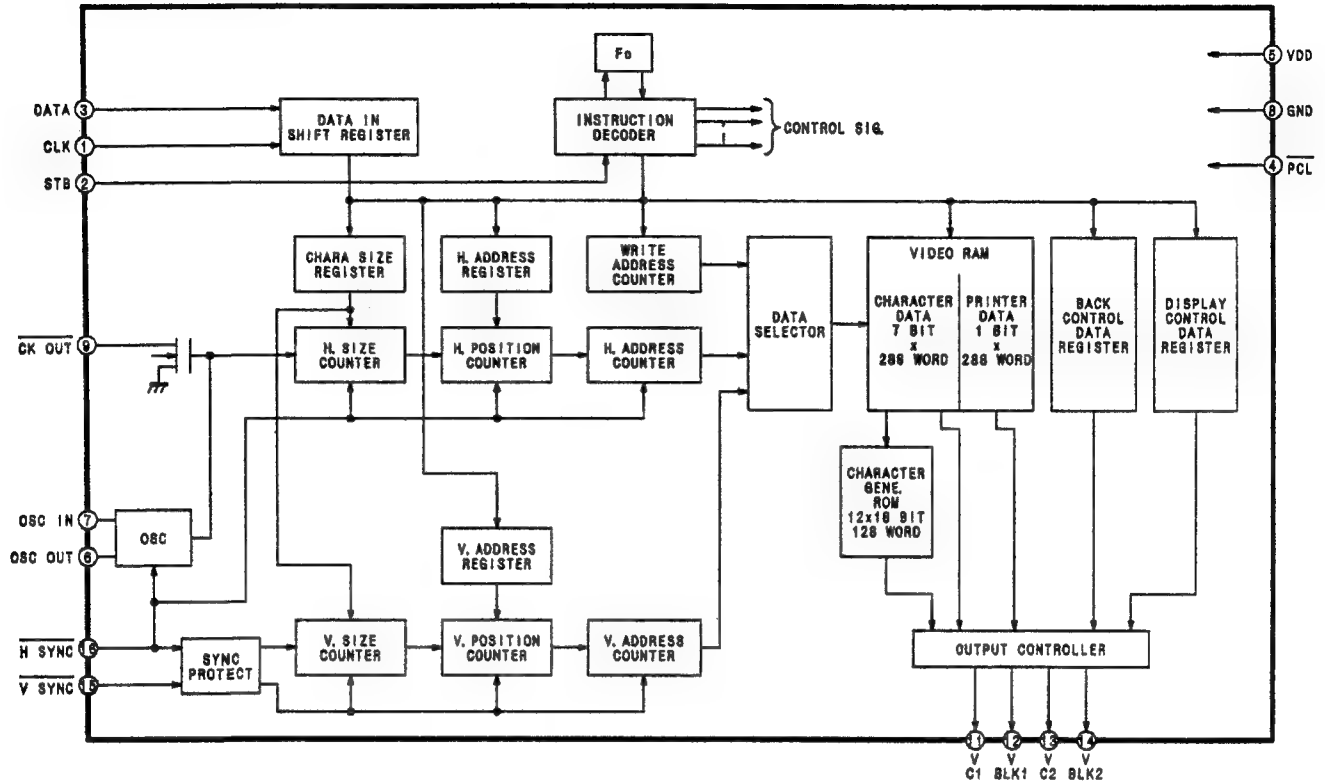
(TOP VIEW)



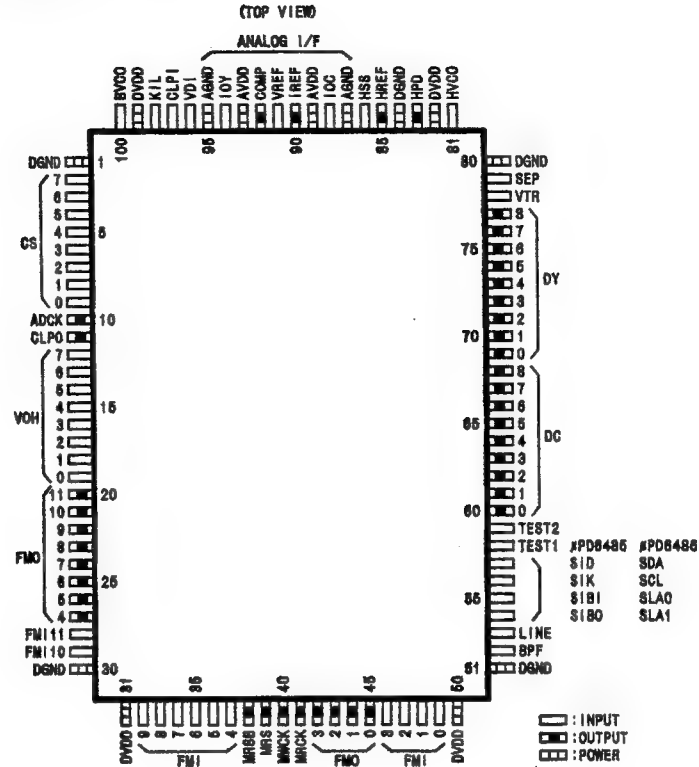
BLOCK DIAGRAM



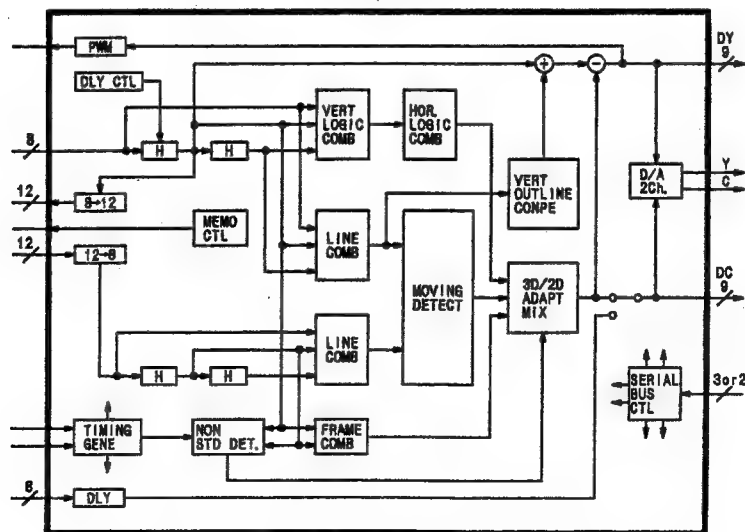
UPD6456
(ON-SCREEN CHARACTER DISPLAY)



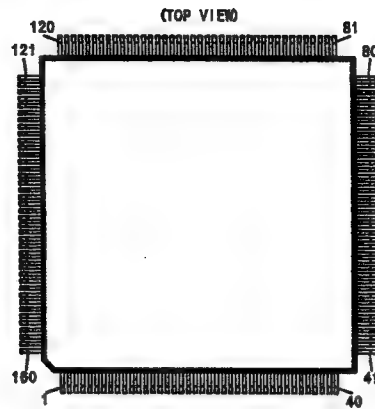
#PD6486GF
NTSC Y/C SEPARATION



BLOCK DIAGRAM



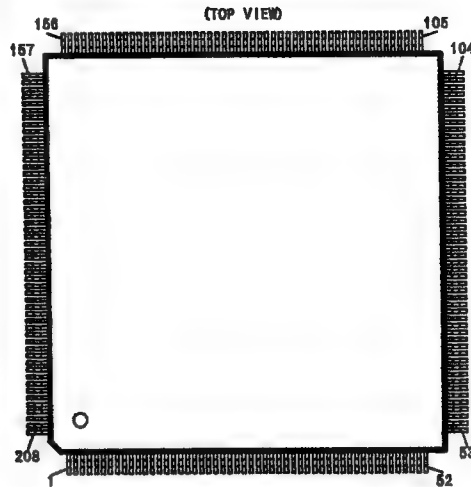
#PD658456039



PIN ALIGNMENT

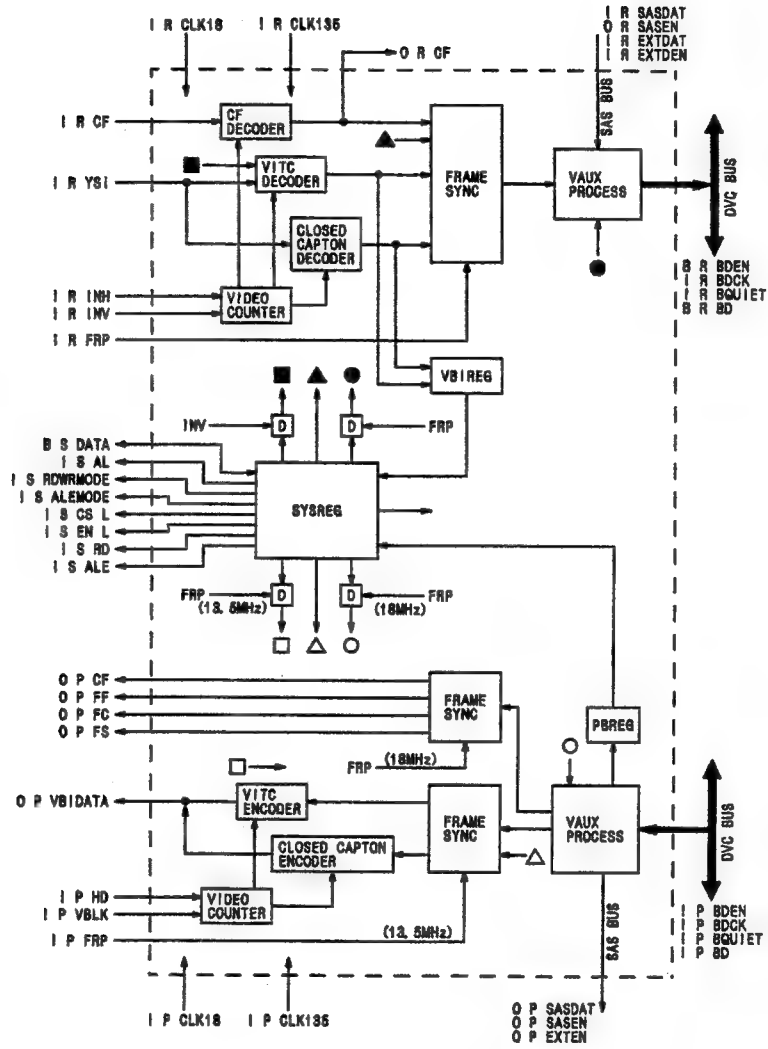
PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	VDD	41	GND	81	VDD	121	GND
2	FRP R	42	GND	82	I EEDAT	122	GND
3	SEQN0	43	CF0	83	HSE	123	FE CTRL0
4	SEQN1	44	CF1	84	CTLA	124	FE CTRL1
5	SEQN2	45	CF2	85	CTLB	125	CLK837
6	SEQN3	46	DLYDAT0	86	FRP P	126	AL0
7	GND	47	DLYDAT1	87	FIFORST	127	AL1
8	FRMSTRY	48	DLYDAT2	88	VDD	128	AL2
9	CFLOAD	49	DLYDAT3	89	FIFOCCLK	129	AL3
10	FEFRMST	50	DLYDAT4	90	O EEDAT	130	AL4
11	GND	51	CLK18	91	O EDAT70	131	AL5
12	RECSTRT	52	TRANSIT	92	O EDAT71	132	GND
13	SBSTR	53	GND	93	O EDAT72	133	DATA0
14	TST SEQ0	54	RRST	94	GND	134	DATA1
15	TST SEQ1	55	WRST	95	GND	135	DATA2
16	TST SEQ2	56	SBSTP	96	O EDAT73	136	DATA3
17	TST SEQ3	57	DEDP0	97	O EDAT74	137	DATA4
18	SEQNEN	58	DEDP1	98	O EDAT75	138	DATA5
19	SEQNEN2	59	DEDP2	99	O EDAT76	139	DATA6
20	VDD	60	DEDP3	100	VDD	140	DATA7
21	GND	61	GND	101	GND	141	GND
22	OUT SEQ0	62	CLK8	102	PBCLK	142	CS N
23	OUT SEQ1	63	PBDAT18	103	PBDATA	143	READ
24	OUT SEQ2	64	PBDAT880	104	PBDATA80	144	WRITE
25	OUT SEQ3	65	PBDAT881	105	PBDATA81	145	U ALMODE
26	GND	66	PBDAT882	106	PBDATA82	146	U RWMODE
27	SBSTP R	67	PBDAT883	107	VDD	147	ALE
28	DEDP R0	68	PBDAT884	108	PBDATA83	148	VDD
29	DEDP R1	69	PBDAT885	109	PBDATA84	149	TEST SW
30	DEDP R2	70	PBDAT886	110	PBDATA85	150	RST SW
31	DEDP R3	71	PBDAT887	111	PBDATA86	151	SBE
32	HIO R	72	I EDAT70	112	PBDATA87	152	HIZ
33	GND	73	I EDAT71	113	GND	153	TCK
34	SBSTP P	74	I EDAT72	114	ATFCLK	154	TR3
35	DEDP P0	75	I EDAT73	115	I REC L	155	TMS
36	DEDP P1	76	I EDAT74	116	I SPA	156	TDI
37	DEDP P2	77	I EDAT75	117	TST DFRP	157	TDO
38	DEDP P3	78	I EDAT76	118	ATFCLK5	158	VDD
39	HIO P	79	GND	119	GND	159	GND
40	VDD	80	GND	120	VDD	160	GND

#PD65868D022
(GATE ARRAY)

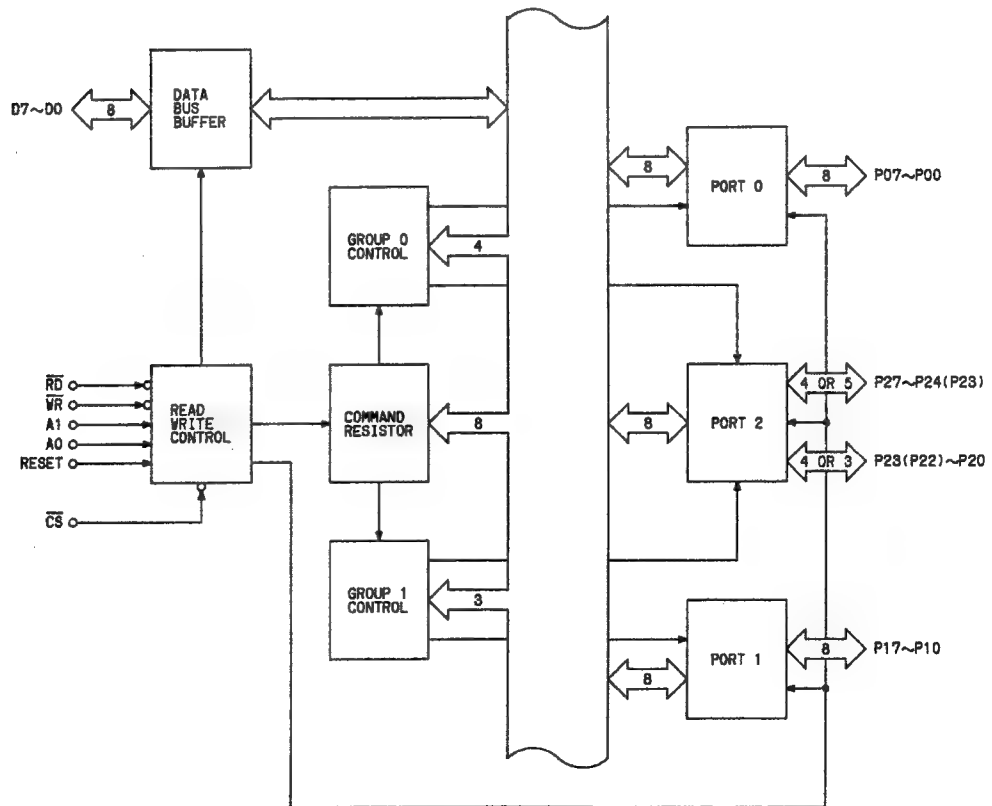
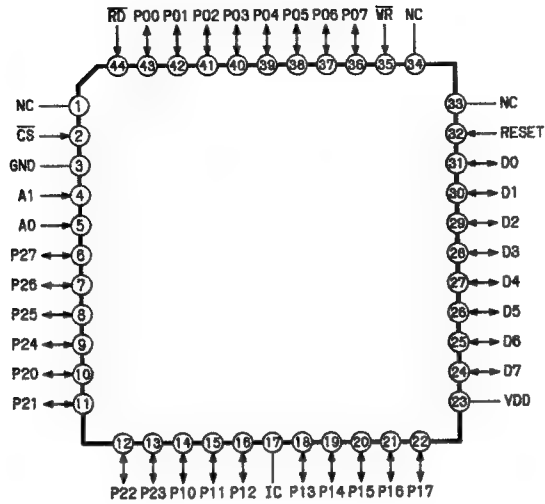


PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	GND	53	VDD	105	GND	157	VDD
2	GND	54	BTLO	106	GND	158	RVO
3	RCF0	55	BTL1	107	PSD0	159	RVZ
4	RCF1	56	BTL2	108	PSD1	160	RVW
5	RCV	57	GND	109	PSD2	161	RA1Z
6	INH	58	BTL3	110	PSD3	162	RA1W
7	INV	59	BTL4	111	PSE	163	RA2Z
8	RFP	60	BTL5	112	PEE	164	RA2W
9	N.C.	61	BTL6	113	VDD	165	GND
10	N.C.	62	GND	114	GND	166	VDD
11	SRW	63	GND	115	PBD0	167	RSD0
12	SAM	64	BTL7	116	PBD1	168	RSD1
13	SCS	65	BTL8	117	PBD2	169	RSD2
14	SRD	66	BTL9	118	PBD3	170	RSD3
15	SEN	67	VDD	119	PBD4	171	RSE
16	SAE	68	BFRM	120	PBD5	172	N.C.
17	SD0	69	APF	121	PBD6	173	TCF0
18	SD1	70	ALP	122	PBD7	174	TCF1
19	SD2	71	ASE	123	PBE	175	TCV
20	GND	72	ALV	124	PBC	176	VARE
21	SD3	73	ATE	125	PBQ	177	VBRE
22	SD4	74	AAD0	126	PFP	178	N.C.
23	SD5	75	AAD1	127	TCK	179	N.C.
24	SD6	76	AAD2	128	TRS	180	GND
25	SD7	77	PIC	129	TMS	181	RSC
26	GND	78	VDD	130	VDD	182	GND
27	VDD	79	GND	131	GND	183	VDD
28	SAL0	80	PSC	132	TDI	184	RIC
29	SAL1	81	GND	133	TDO	185	GND
30	SAL2	82	N.C.	134	HIZ	186	BCD0
31	SAL3	83	AAD3	135	RST	187	BCD1
32	SAL4	84	AAD4	136	GND	188	BCD2
33	SAL5	85	AAD5	137	RBE	189	BCD3
34	PVDO	86	AAD6	138	RBC	190	BCD4
35	PVD1	87	AAD7	139	RBQ	191	BCD5
36	PVD2	88	AAD8	140	RBD0	192	BCD6
37	PVD3	89	AAD9	141	RBD1	193	BCD7
38	PVD4	90	AAD10	142	RBD2	194	VDD
39	PVD5	91	AAD11	143	RBD3	195	GND
40	PVD6	92	AAD12	144	RBD4	196	BTCE
41	PVD7	93	AAD13	145	RBD5	197	BCDR
42	N.C.	94	PCF0	146	RBD6	198	BTDR
43	N.C.	95	PCF1	147	RBD7	199	RY10
44	N.C.	96	PCN	148	GND	200	RY11
45	PVE	97	PCE	149	TST1	201	RY12
46	PDE	98	PFF	150	RXD0	202	RY13
47	PHD	99	PFS	151	RXD1	203	RY14
48	PVB	100	PFC	152	RXD2	204	RY15
49	VAPE	101	PFV	153	RXD3	205	RY16
50	VBPE	102	TST2	154	RXE	206	RY17
51	GND	103	TST3	155	GND	207	N.C.
52	GND	104	VDD	156	GND	208	VDD

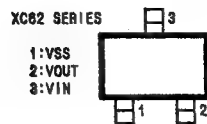
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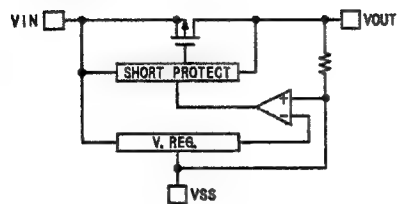
UPD710556
(PARALLEL INTERFACE UNIT)



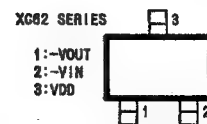
XC62APXX02M
(VOLTAGE REGULATOR)



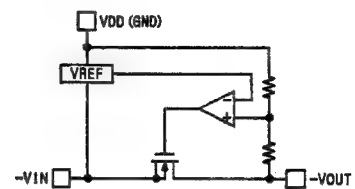
BLOCK DIAGRAM



XC62DNXX02M
(VOLTAGE REGULATOR)

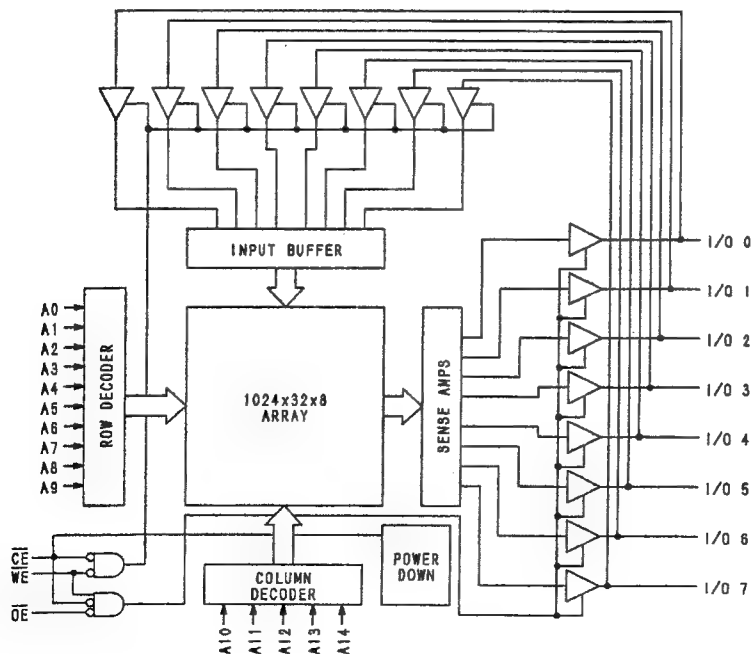


BLOCK DAIGRAM



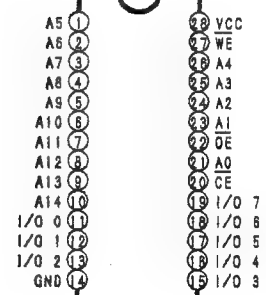
Y7C19935VC
(32Kx8 STATIC RAM)

LOGIC BLOCK DIAGRAM

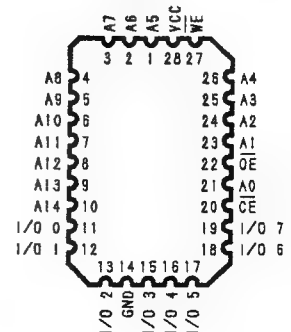


PIN CONFIGURATIONS

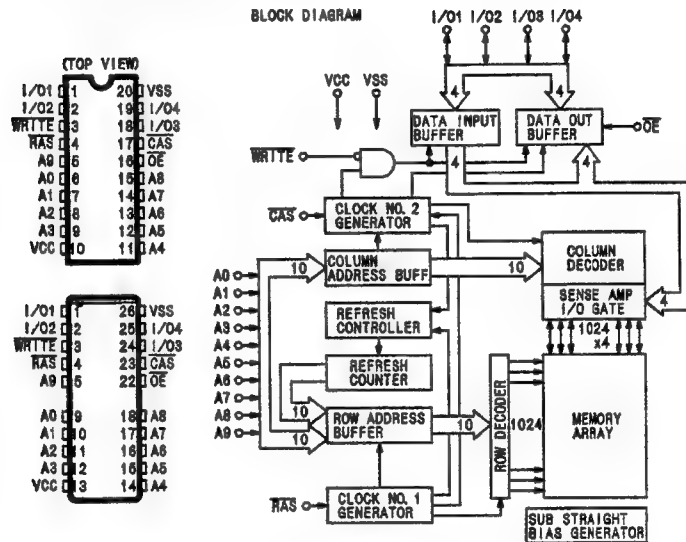
**DIP/SOJ
(TOP VIEW)**



**LCC
(TOP VIEW)**



T51440ASJ7EL
(4M 1,048,576 WORDSx48ITS D RAM)



17727

Order No. VSD9610SA613

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Improvement of Pr and Pb Frequency Response

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D750E/EN	13	VSD9606M502A/B	G6TRA0001

Board : V OUT (F4:VEP83221B)

Symptom : Pr and Pb frequency response of Analog Component OUT may be out of specification.

Cause : Noise may appear on the Component Y/C timing adjustment volume due to the wiring procedures.

Remedy : To improve it, capacitors C8735 and C8754 are changed from 50V/120pF to 50V/150pF on the foil side.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
C8735	ECUX1H121JCV	ECUX1H151JCV	C. CAPACITOR CH 50V 150P	1	
C8754	ECUX1H121JCV	ECUX1H151JCV	C. CAPACITOR CH 50V 150P	1	

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
C8735	2-80	E-8 (26/30)	3-6	H-3 (F)
C8754	2-80	E-8 (26/30)	3-6	I-3 (F)

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Order No. VSD9610SA614

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Reduction of Vertical and Horizontal Sags at Video OUT

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D750E/EN	14	VSD9606M502A/B	I6TRA0001

Board : V OUT (F4:VEP83221B)

Symptom : Vertical sag and horizontal sag may be appeared at the V blanking period.

Cause : Due to the tolerance of leak current of sample hold circuit.

Remedy : To reduce the vertical and horizontal sags, capacitors C8716, C8738, C8757 and C8909 are changed from 50V/100pF to 50V/1000pF on the foil side.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
C8716	ECUX1H101JCV	ECUX1H102JV	C. CAPACITOR CH 50V 1000P	1	
C8738	ECUX1H101JCV	ECUX1H102JV	C. CAPACITOR CH 50V 1000P	1	
C8757	ECUX1H101JCV	ECUX1H102JV	C. CAPACITOR CH 50V 1000P	1	
C8909	ECUX1H101JCV	ECUX1H102JV	C. CAPACITOR CH 50V 1000P	1	

Ref. No.	Schematic Diagram		P.C. Board	
	Page	Area No.	Page	Area No.
C8716	2-80	B-10 (26/30)	3-6	H-3 (F)
C8738	2-80	D-10 (26/30)	3-6	I-3 (F)
C8757	2-80	G-10 (26/30)	3-6	J-3 (F)
C8909	2-83	B-4 (28/30)	3-6	I-3 (F)

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Order No. VSD9610SA616

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Improvement of Picture Under High Temperature

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D750E/EN	16	VSD9606M502A/B	J6TRA0001

Board : REC PB (F5:VEP83223B)

Symptom : Picture may be disturbed under high temperature.

Cause : Noise may jump into the ECC output signal of playback side due to the temperature characteristics of ECC.

Remedy : To reduce the picture disturbance, the following modification is performed.

- 1). Add a resistor R3741 (1/4W, 27K Ω) between pins #2 and #10 of IC3241 on the foil side as shown in figures 1 and 2.
- 2). Add a resistor R3742 (1/4W, 27K Ω) between C3264 and land (A portion) on the component side as shown in figures 3 and 4.
- 3). Add a resistor R3743 (1/4W, 27K Ω) between pins #6 and #10 of IC3241 on the foil side as shown in figures 1 and 2.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
R3741 ~ 43	—	ERDS2TJ273	C. RESISTOR 1/4W 27K	0→3	

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REC PB (F5 20/23) Schematic Diagram

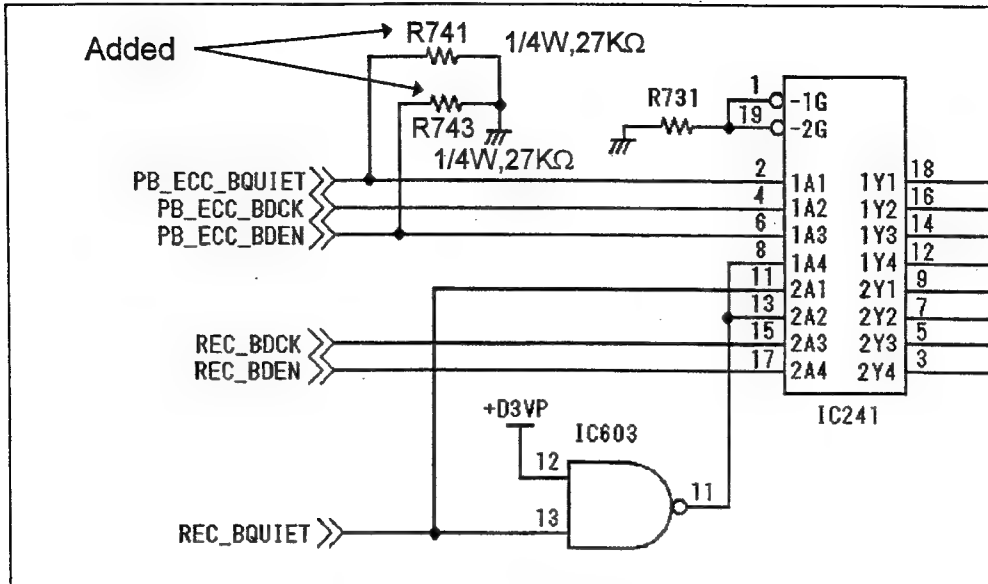


Fig. 1 Page 2-105 (B-2)

F5 REC PB P.C.Board (VEP83223B)

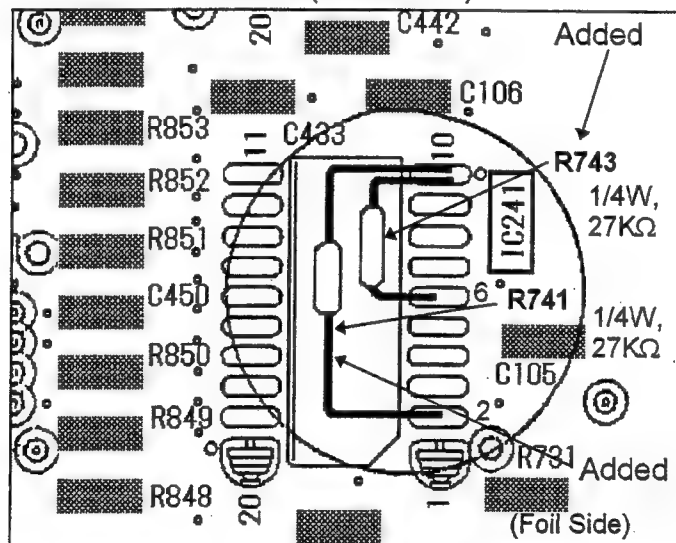


Fig. 2 Page 3-7 (E-2)

REC PB (F5 20/23) Schematic Diagram

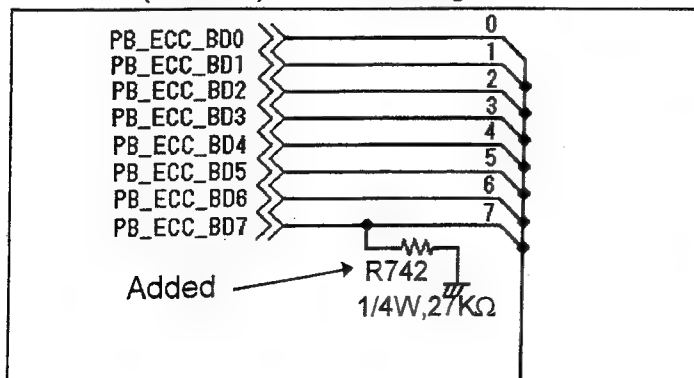


Fig. 3 Page 2-105 (F-2)

F5 REC PB P.C.Board (VEP83223B)

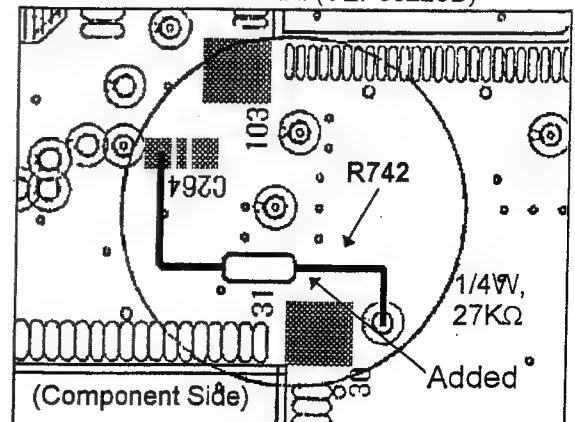


Fig. 4 Page 3-7 (E-2)

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Order No. VSD9610SA618

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Software Version Up Grades

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D750E/EN	18	VSD9606M502A	J6TRA0001

Board : REC PB (F5:VEP83223B)

The following software has been up-dated to improve the functioning of the VTR.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
IC501	VSI2282	VSI2159D	F5 SBC1 PROM Ver. 1.04	1	CHECK SUM : D5CA
IC601	VSI2282	VSI2159D	F5 SBC2 PROM Ver. 1.04	1	CHECK SUM : D5CA

< Improvement of Performance >

1. RECDATE and RECTIME data is written in spite of write inhibit method. It is improved.

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Order No. VSD9610SA619

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Improvement of Tape End/Beginning Detection

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D750E/EN	19	VSD9606M502A/B	J6TRA0001

Board : System Control (F2:VEP86146B)

Symptom : When the Consumer DV tape is inserted, the tape end/beginning may be mis-detected.

Cause : Black portion of the tape may be detected as white portion of the tape.

Remedy : To prevent it, resistor R11 is changed from 3.3K Ω to 1K Ω on the foil side.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
R11	ERJ6GEYJ332	ERJ6GEYJ102	M. RESISTOR CH 1/10W 1K	1	

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
R11	2-31	B-8 (1/14)	3-4	C-2 (F)

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Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Improvement of Crystal Oscillator Circuit

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D750E/EN	20	VSD9606M502A/B	K6TRB0001

Board : System Control (F2:VEP86146B)
Front CPU (VEP86147A)

To have an oscillation margin for the microcomputer oscillator circuit, the following modification is performed.

< System Control >

- 1). Change capacitors C10 and C11 from 50V/27pF to 50V/15pF on the component side.
- 2). Change capacitors C500 and C501 from 50V/22pF to 50V/12pF on the component side.
- 3). Change resistor R57 from 12Ω to 1KΩ on the component side.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
C10, 11	ECUM1H270JCN	ECUM1H150JCN	C. CAPACITOR CH 50V 15P	2	
C500, 501	ECUM1H220JCN	ECUM1H120JCN	C. CAPACITOR CH 50V 12P	2	
R57	ERJ6GEYJ120	ERJ6GEYJ102	M. RESISTOR CH 1/10W 1K	1	

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
C10	2-31	G-9 (1/14)	3-4	C-3 (C)
C11	2-31	G-9 (1/14)	3-4	C-3 (C)
C500	2-36	B-4 (6/14)	3-4	E-2 (C)
C501	2-36	C-4 (6/14)	3-4	E-2 (C)
R57	2-31	G-9 (1/14)	3-4	C-3 (C)

< Front CPU >

- 1). Change capacitors C4 and C5 from 50V/22pF to 50V/10pF on the component side.
- 2). Change resistor R17 from 0Ω to 180Ω on the component side.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
C4, 5	ECUM1H220JCN	ECUM1H100DCN	C. CAPACITOR CH 50V 10P	2	
R17	ERJ6GEY0R00	ERJ6GEYJ181	M. RESISTOR CH 1/10W 180	1	

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Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
C4	2-196	C-3 (1/4)	3-21	D-3 (C)
C5	2-196	C-3 (1/4)	3-21	D-3 (C)
R17	2-196	C-3 (1/4)	3-21	D-2 (C)

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Order No. VSD9611SA621

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Software Version Up Grade

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D750E/EN	21	VSD9606M502A/B	K6TRB0001

Board : Front CPU (VEP86147A)

The following software has been up-dated to improve the functioning of the VTR.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
IC2	VSI2166C	VSI2166D	FRONT PROM Ver. N1.04	1	

< TEST MENU >

SERVO IC235	:	F1-P1.06	5BED	SYSTEM IC2	:	F2-P1.03	341D
I/F IC503	:	F2-P1.02	7C36	AV IC702	:	F2-P1.07	65CF
FRONT IC2	:	FP-N1.04	299F				

< Improvement of Performance >

1. When the Search Dial is rotated to the maximum direction of REV during Service Menu, it is rotated to FWD direction. It is improved.

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Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Introduction of New MECHA I/F Board

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D750E/EN	22	VSD9606M502A/B	J6TRB0163

Board : MECHA I/F (VEP82214A)

Pin arrangement of connector P17 for the MIC Sensor on the MECHA I/F Board is changed. According to this change, the following change is performed.

- 1). P.C.Board number is changed from VEP82106A to VEP82214A.
- 2). Serial Number version is advanced from A version to B version as shown below.

J6TRA**** → J6TRB****

- 3). There is no interchangeability between old MECHA I/F Board and new one. So, when the old MECHA I/F Board (VEP82106A) is replaced to new one (VEP82214A), please mark on the Serial Number Plate as you can discriminate between old Board and new Board.
- 4). After this modification, 5-7. Tension Arm Adjustment Procedures are required.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
	VEP82106A	VEP82214A	MECH I/F P.C.BOARD	1	

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Order No. VSD9611SA623

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Reduction of Noise from Cylinder Circuit

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D750E/EN	23	VSD9606M502A/B	J6TRB0163
AJ-D650E/EN	1	VSD9612MJ01A/B	K6TRA0001
AJ-D640E/EN	1	VSD9612MJ01A/B	K6TRA0001

Board : MECHA I/F (VEP82214A)

Symptom : High Error Rate may occur.

Cause : Noise from the Cylinder circuit may jump into the RF circuit. It results in High Error Rate.

Remedy : To improve the Error Rate, the following modification is performed.

- 1). Add a capacitor C200 (50V/100pF) between pins #2 and #26 of P1 on the foil side as shown in figures 1 and 2.
- 2). Add a capacitor C201 (50V/100pF) between pins #1 and #27 of P1 on the foil side as shown in figures 1 and 2.
- 3). Add a capacitor C202 (50V/100pF) between pin #28 of P1 and land of GND on the foil side as shown in figures 1 and 2.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
C200 ~ 02	—	ECCF1H101JC	C. CAPACITOR 50V 100P	0→3	

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MECHA I/F (3/4) Schematic Diagram

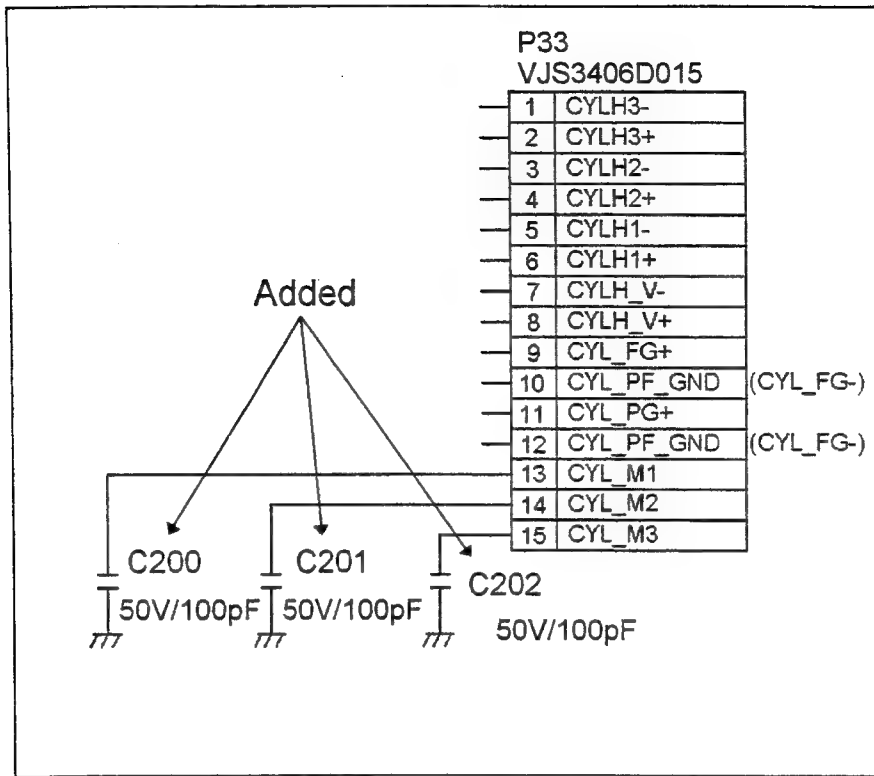


Fig. 1 Page 2-190 (C-7)

MECHA I/F P.C. Board (VEP82214A)

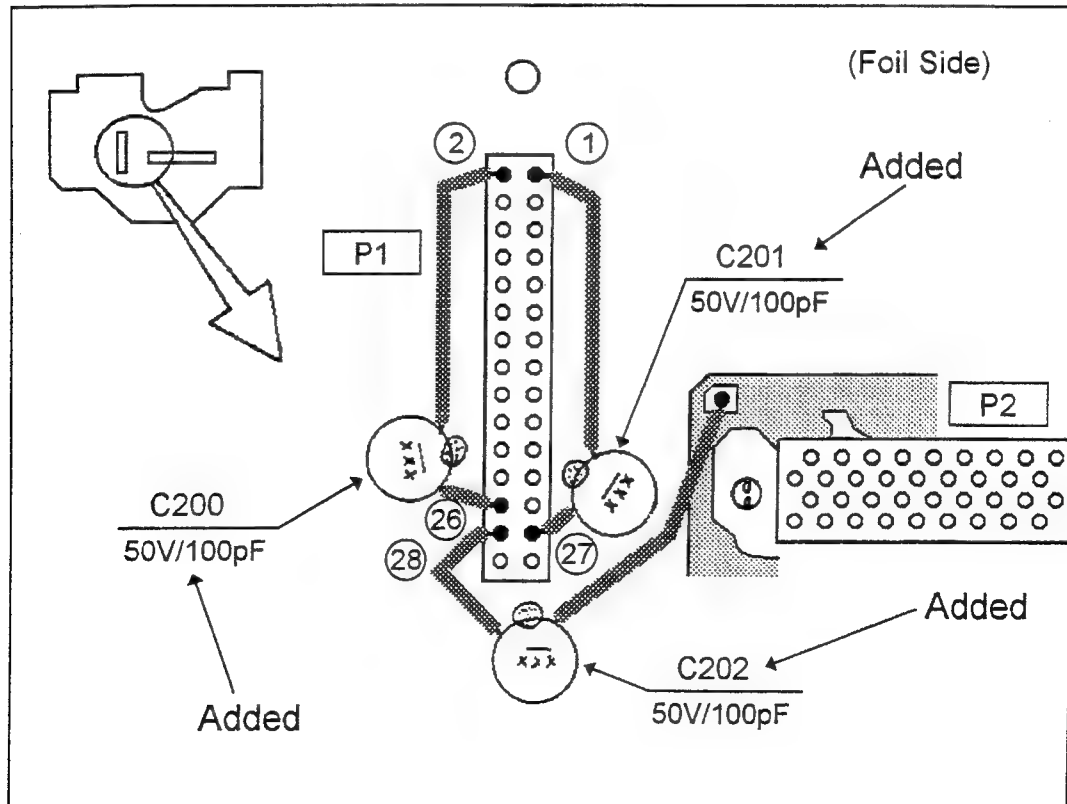


Fig. 2 Page 3-18 (D-2~3)

V17727

Order No. VSD9612SA624

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Change of IC

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-YA750P	24	VSD9606M502A/B	L6TRB0001

Board : SIF (F3:VEP83220A)

Reason for Change

- ☐ The following part(s) has(have) been changed for serviceability improvement.
- ☐ The following part(s) has(have) been changed for productivity improvement.
- ☒ The following part(s) has(have) been changed for standardization.
- ☐ The following part(s) has (have) been changed for the safety regulation.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
IC3301	CG31633-2109	CG31633-2131	IC	1	

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
IC3301	2-52	G-8 (8/9)	3-5	I-4 (C)

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Order No. VSD9612SA625

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Improvement of CUE Audio Monitor Output Level

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D750E/EN	25	VSD9606M502A/B	L6TRB0001

Board : CUE (H2:VEP84182B)

Symptom : Monitor Output level is decreased about -2dB against CH1 or CH2 when select CUE on the Monitor OUT.

Cause : Cue Audio output level for the Channel Select circuit of the Monitor is set lower than CH1 or CH2 output level.

Remedy : To improve Monitor Output level, the following modification is performed.

- 1). Change resistor R4057 from 2.2K Ω to 1.5K Ω on the foil side.
- 2). Change resistor R4105 from 2.7K Ω to 36K Ω on the foil side.
- 3). Change resistor R4112 from 12K Ω to 8.2K Ω on the foil side.
- 4). Change resistor R4166 from 1.5K Ω to 4.7K Ω on the foil side.
- 5). Change resistor R4211 from 15K Ω to 11K Ω on the component side.
- 6). After this modification, the following adjustment procedures are required.
 - 3-4. CUE PB Level Adjustment
 - 3-8. CUE REC/PB Level Adjustment

*** Note *** When this modification is performed, the System Control and I/F PROM software must be up-graded at the same time. Please refer to the Technical Bulletin No. VSD9609SA608.

System Control (IC2) : VSI2277B F2-P1.02 1CD7
I/F (IC503) : VSI2279A F2-P1.01 DC03

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
	VEP84182A	VEP84182B	CUE P.C.BOARD	1	
R4057	ERJ6GEYJ222	VRE0034E152	M. RESISTOR CH 1/10W 1.5K	1	
R4105	VRE0034E272	VRE0034E363	M. RESISTOR CH 1/10W 36K	1	
R4112	ERJ6GEYJ123	VRE0034E822	M. RESISTOR CH 1/10W 8.2K	1	
R4166	VRE0034E152	VRE0034E472	M. RESISTOR CH 1/10W 4.7K	1	
R4211	VRE0034E153	VRE0034E113	M. RESISTOR CH 1/10W 11K	1	

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
R4057	2-159	G-16 (1/6)	3-11	C-2 (F)

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Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
R4105	2-160	B-6 (2/6)	3-11	E-3 (F)
R4112	2-160	E-5 (2/6)	3-11	E-4 (F)
R4166	2-160	E-6 (2/6)	3-11	D-3 (F)
R4211	2-161	D-6 (3/6)	3-11	C-3 (F)

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Order No. VSD9612SA626

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Change of IC

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D750E/EN	26	VSD9606M502A/B	L6TRB0001

Board : V OUT (F4:VEP83221B)

Reason for Change

- ☐ The following part(s) has(have) been changed for serviceability improvement.
- ☐ The following part(s) has(have) been changed for productivity improvement.
- ☒ The following part(s) has(have) been changed for standardization.
- ☐ The following part(s) has (have) been changed for the safety regulation.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
IC8170	SN74AS244NS	SN74AS244AN	IC	1	
IC8264, 65	SN74AS244NS	SN74AS244AN	IC	2	
IC8330, 31	SN74AS244NS	SN74AS244AN	IC	2	

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
IC8170	2-64	C-18 (10/30)	3-6	C-2 (F)
IC8264	2-67	B~C-8 (13/30)	3-6	A-2 (F)
IC8265	2-67	D~E-9 (13/30)	3-6	A-3 (F)
IC8330	2-70	A-3 (16/30)	3-6	D-3 (F)
IC8331	2-70	D-3 (16/30)	3-6	C-3 (F)

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Order No. VSD9701SA627

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Improvement of PLL Unlock under Low Temperature (-10°C)

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D750E/EN	27	VSD9606M502A/B	A7TRB0001
AJ-D650E/EN	2	VSD9612MJ01A/B	A7TRA0001
AJ-D640E/EN	2	VSD9612MJ01A/B	A7TRA0001

Board : EQ (H3:VEP85048A)

Symptom : PLL may not be locked under low temperature. (-10°C)

Cause : Output voltage may oscillate due to the lack of input capacity of 3 terminals regulator.

Remedy : To prevent the PLL unlock, the following modification is performed.

- 1). Add a capacitor C5995 (16V/47 μ F) between terminals I (plus side) and G (minus side) of IC5956 on the component side as shown in figures 1 and 2.
- 2). Add a capacitor C5996 (16V/47 μ F) between terminals G (plus side) and I (minus side) of IC5958 on the component side as shown in figures 3 and 4.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
C5995, 56	—	ECEA1CGE470	E. CAPACITOR 16V 47U	0→2	

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EQ (H3 9/9) Schematic Diagram

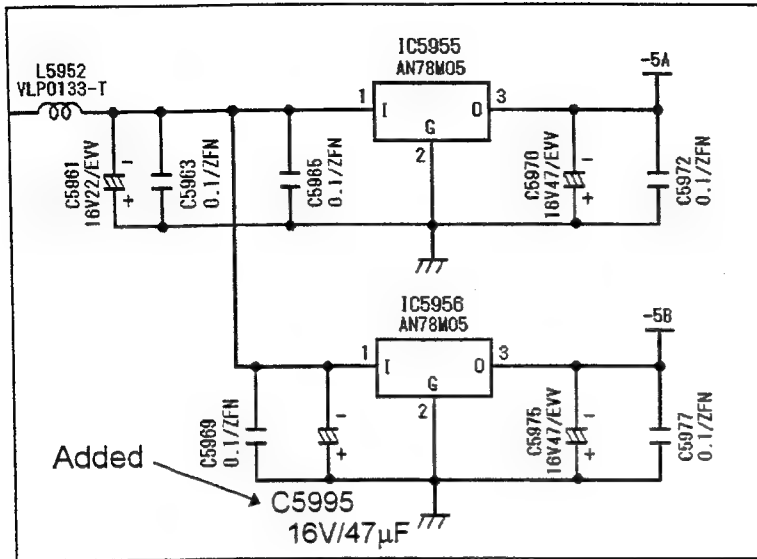


Fig. 1 Page 2-173 (E-5) - AJ-D750
Page 2-135 (B-5) - AJ-D640/D650

EQ P.C.Board (VEP85048A)

(Component Side)

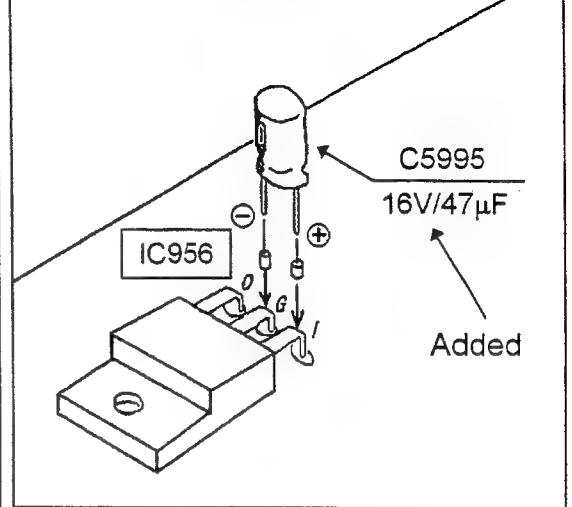


Fig. 2 Page 3-12 (A-2) - AJ-D750
Page 3-10 (A-2) - AJ-D640/D650

EQ (H3 9/9) Schematic Diagram

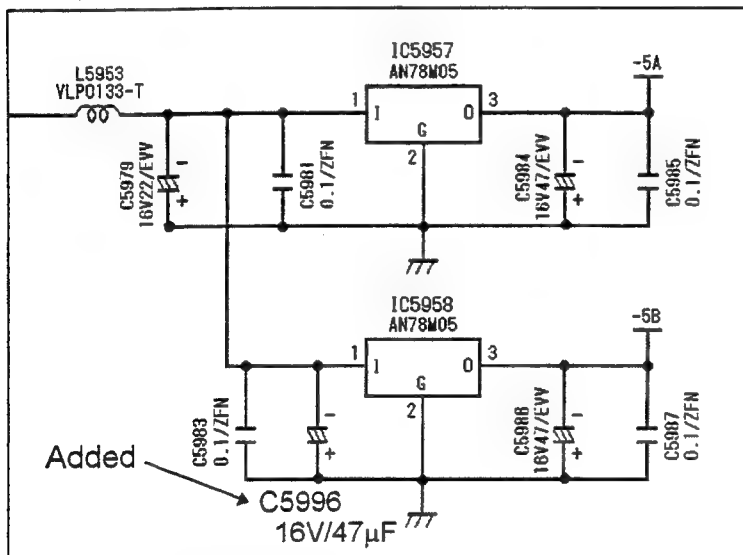


Fig. 3 Page 2-173 (E-7) - AJ-D750
Page 2-135 (B-7) - AJ-D640/D650

EQ P.C.Board (VEP85048A)

(Component Side)

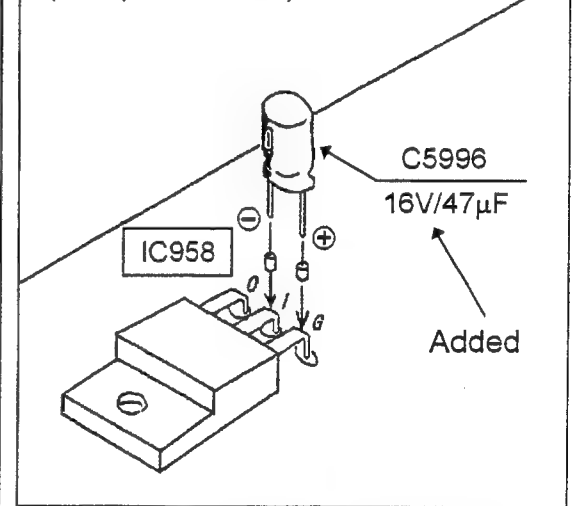


Fig. 4 Page 3-12 (A-3) - AJ-D750
Page 3-10 (A-3) - AJ-D640/D650

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Order No. VSD9701SA628

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Change of ROM Type

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D750E/EN	28	VSD9606M502A/B	A7TRB0001

Board : REC PB (F5:VEP83223B)

To improve manufacturing productivity, IC501 and IC601 are changed from one time memory type PROM to masking type PROM as follows.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
IC501	VSI2159D	M37709M4L162	F5 SBC1 PROM Ver. 1.04	1	CHECK SUM : D5CA
IC601	VSI2159D	M37709M4L162	F5 SBC2 PROM Ver. 1.04	1	CHECK SUM : D5CA

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V17727

Order No. VSD9701SA629

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Change of IC (SRAM)

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D750E/EN	29	VSD9606M502A/B	A7TRB0001

Board : Servo (F1:VEP82105B)

Reason for Change

- ☐ The following part(s) has(have) been changed for serviceability improvement.
☒ The following part(s) has(have) been changed for productivity improvement.
☒ The following part(s) has(have) been changed for standardization.
☐ The following part(s) has (have) been changed for the safety regulation.

Part Number				
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs
IC260, 261	MB81C78A35PF	Y7C18525SC	IC	2

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
IC260	2-20	B~C-4 (9/19)	3-3	H-3 (C)
IC261	2-20	E~F-4 (9/19)	3-3	J-3 (C)

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Technical Bulletin

Supplement to the Service Manual

Broadcast Product

**Subject : Countermeasure for Electric Power Capability of 3 Terminals
Regulator IC under High Temperature (60°C)**

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D750E/EN	30	VSD9606M502A/B	A7TRB0001
AJ-D650E/EN	3	VSD9612MJ01A/B	A7TRA0001
AJ-D640E/EN	3	VSD9612MJ01A/B	A7TRA0001

Board : REC PB (F5:VEP83223B) - AJ-D750
REC PB (F5:VEP83353B) - AJ-D640/D650

Symptom : Electric power capability of 3 terminals regulator IC may be over under high temperature environment (60°C).

Remedy : To prevent it, the input voltage is decreased. The following modification is performed.

*** P.C.Board version is VEP83223B (AJ-D750)**

- 1). Cut the foil between terminal I of IC256 and terminal O of D112 on the foil side as shown in figures 1 and 2.
- 2). Add a diode D113 (11ES1) between terminal I of IC254 (anode side) and terminal I of IC256 (cathode side) on the foil side as shown in figures 1 and 3.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
D113	—	11ES1	DIODE	0→1	

*** P.C.Board version is VEP83353B (AJ-D640/D650)**

- 1). Cut the foil between terminal I of IC3206 and terminal O of D3112 on the foil side as shown in figures 3 and 4.
- 2). Add a diode D3113 (11ES1) between terminal I of IC3204 (anode side) and terminal I of IC3206 (cathode side) on the foil side as shown in figures 2 and 3.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
D3113	—	11ES1	DIODE	0→1	

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REC PB (F5 22/23) Schematic Diagram

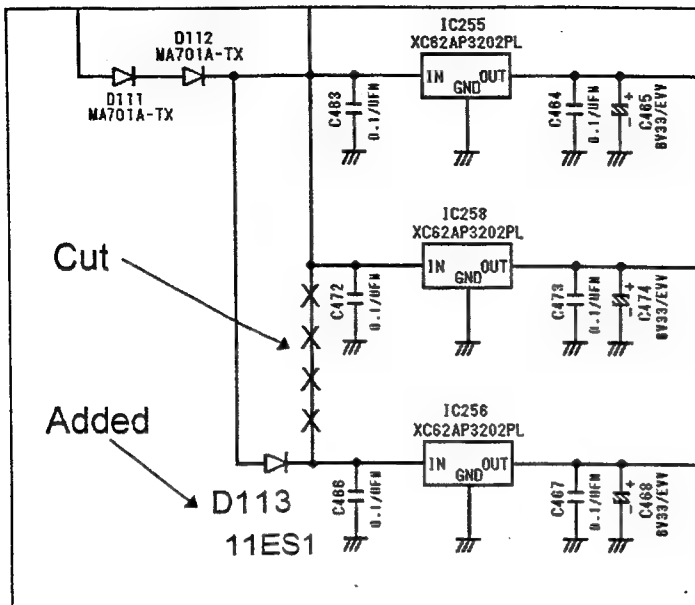


Fig. 1 Page 2-107 (E-3) - AJ-D750

REC PB (F5 22/23) Schematic Diagram

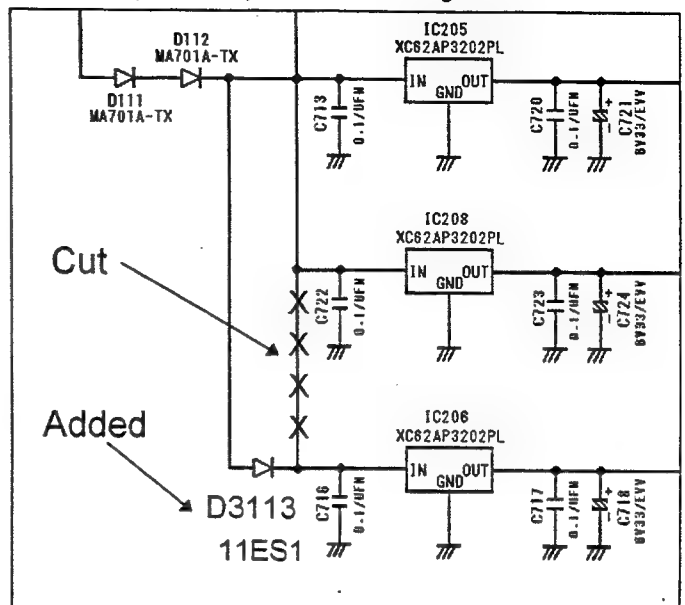


Fig. 2 Page 2-82 (B-4) - AJ-D640/D650

F5 REC PB P.C.Board (VEP83223B / VEP83353B)

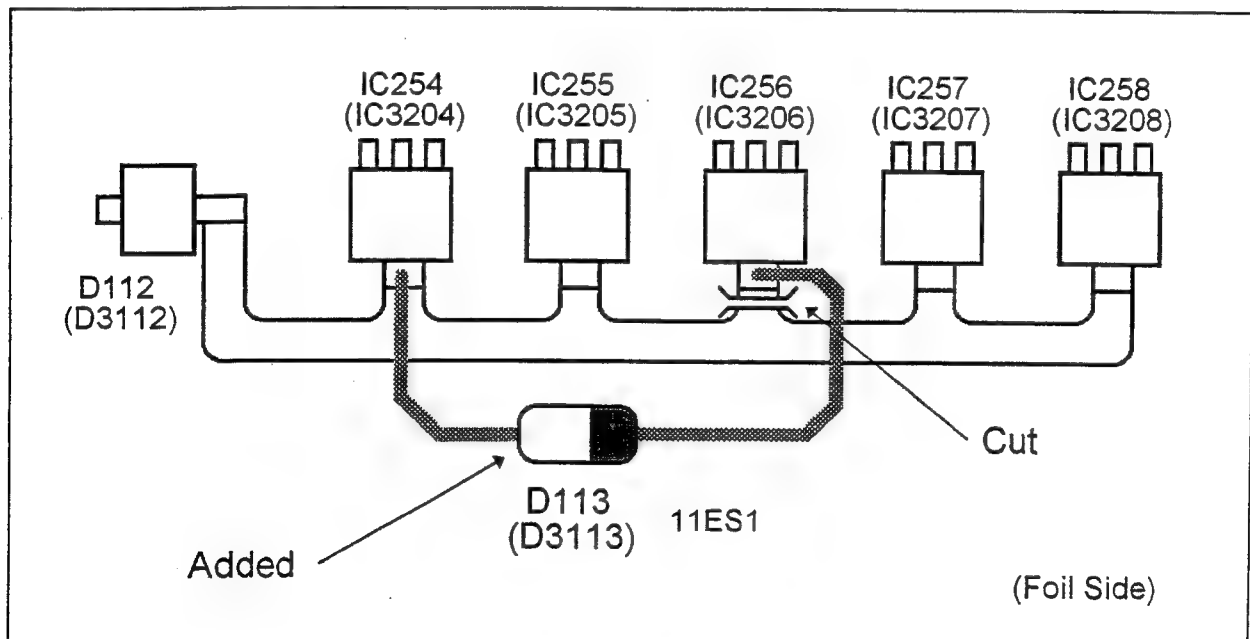


Fig. 3 Page 3-7 (E-4) - AJ-D750
Page 3-6 (E-4) - AJ-D640/D650

V17727

Order No. VSD9702SA632

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Improvement of System H Phase Shift

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D750E/EN	32	VSD9606M502A/B	B7TRB0001

Board : V OUT (F4:VEP83221B)

Symptom : 1). System H phase may shift 1 cycle of sub-carrier when the System Sub-carrier phase is varied.
 2). System H phase may shift and be easy to lock when the power supply is turned ON/OFF.

Remedy : To prevent it, the following modification is performed.

- 1). Change resistor R8130 from 56K Ω to 2.2K Ω on the component side.
- 2). Delete resistor R8229 (1/16W, 56K Ω) from the foil side.
- 3). Cut the foil of pin #5 of IC8164 on the component side as shown in figures 1 and 2.
- 4). Connect a jumper wire between pin #12 and land of pin #5 of IC8164 on the component side as shown in figures 1 and 2.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
R8130	ERJ3GEYJ563	ERJ3GEYJ222	M. RESISTOR CH 1/16W 2.2K	1	
R8229	ERJ3GEYJ563	—	M. RESISTOR CH 1/16W 56K	1→0	

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
R8130	2-62	C-3 (8/30)	3-6	F-1 (C)
R8229	2-65	D-4 (11/30)	3-6	C-1 (F)

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V OUT (F4 10/30) Schematic Diagram

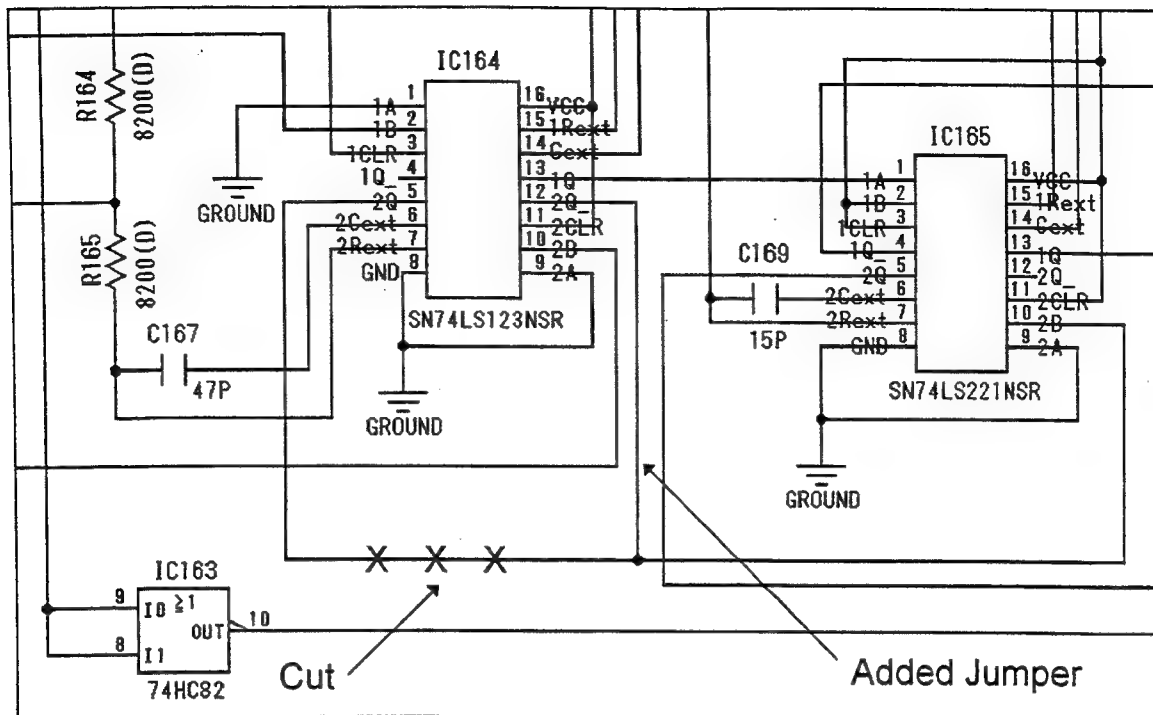


Fig. 1 Page 2-64 (D~E-8~9)

F4 V OUT P.C.Board (VEP83221B)

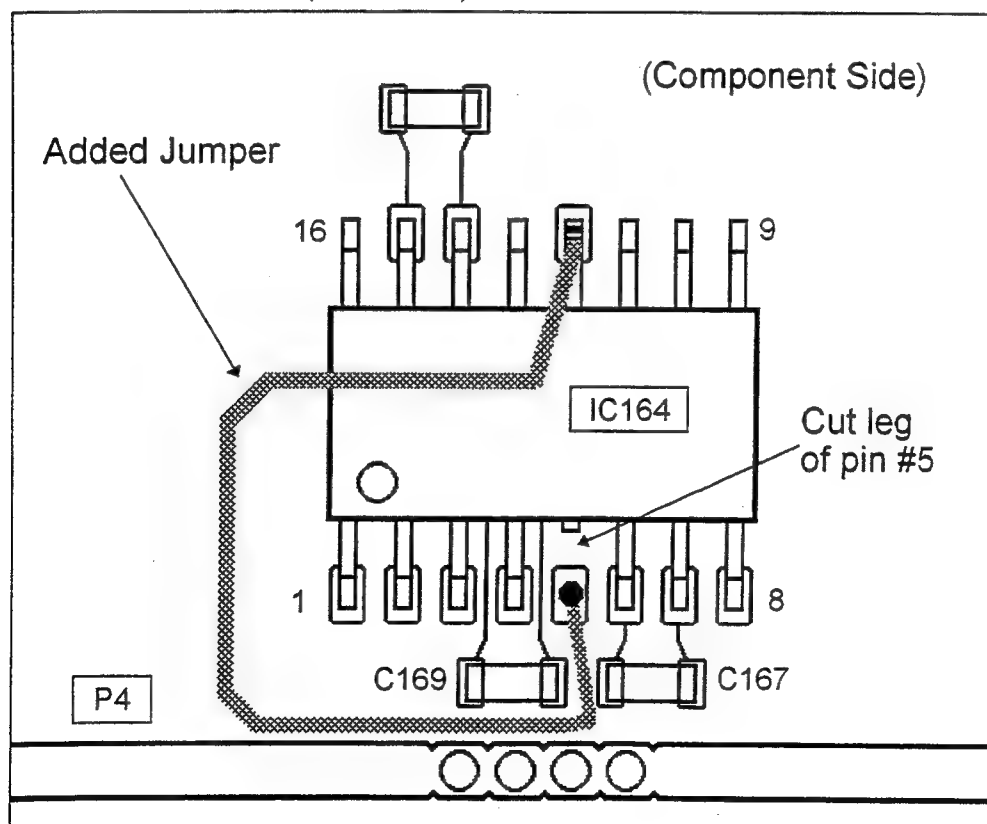


Fig. 2 Page 3-6 (C-2)

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

**Subject : Improvement of Data Communication Error between AV Micon
and SBC Micon under High Temperature (60°C)**

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D750E/EN	33	VSD9606M502A/B	B7TRB0001
AJ-D650E/EN	4	VSD9612MJ01A/B	B7TRA0001
AJ-D640E/EN	4	VSD9612MJ01A/B	B7TRA0001

Board : System Control (F2:VEP86146B) - AJ-D750
System Control (F2:VEP86146E) - AJ-D650
System Control (F2:VEP86146F) - AJ-D640

Symptom : Data communication error between AV microcomputer and SBC microcomputer may occur under high temperature environment (60°C).

Cause : Data input/output timing is delayed due to the temperature characteristics of Transistor-Resistor. It results in data communication error.

Remedy : To prevent it, the following transistor-resistors QR701, QR702 and QR703 are changed from UN2214 to UN221L on the foil side.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
QR701 ~ 3	UN2214	UN221L	TRANSISTOR-RESISTOR	3	

AJ-D750

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
QR701	2-40	B-5 (10/14)	3-4	H-4 (F)
QR702	2-40	A-10 (10/14)	3-4	H-3 (F)
QR703	2-40	A-11 (10/14)	3-4	H-3 (F)

AJ-D640/D650

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
QR701	2-40	F-3 (10/14)	3-4	H-4 (F)
QR702	2-40	F-6 (10/14)	3-4	H-3 (F)
QR703	2-40	F-7 (10/14)	3-4	H-3 (F)

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Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Common Use of ICs (CPU)

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D750E/EN	34	VSD9606M502A/B	B7TRB0001
AJ-D650E/EN	5	VSD9612MJ01A/B	B7TRA0001
AJ-D640E/EN	5	VSD9612MJ01A/B	B7TRA0001

Board : System Control (F2:VEP86146B) - AJ-D750
 System Control (F2:VEP86146E) - AJ-D650
 System Control (F2:VEP86146F) - AJ-D640
 Front CPU (VEP86147A) - AJ-D750
 Front CPU (VEP86256A) - AJ-D640/D650

Reason for Change

- ☐ The following part(s) has(have) been changed for serviceability improvement.
☐ The following part(s) has(have) been changed for productivity improvement.
☒ The following part(s) has(have) been changed for standardization.
☐ The following part(s) has (have) been changed for the safety regulation.

F2 System Control Board (VEP86146B / AJ-D750)

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
IC500	HD64180ZRP8	HD64180ZRP8 or HD64180ZRP10	IC	1	

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
IC500	2-36	B~F-5 (6/14)	3-3	F-2 (C)

F2 System Control Board (VEP86146E / AJ-D650, VEP86146F / AJ-D640)

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
IC500	HD64180ZRP8	HD64180ZRP8 or HD64180ZRP10	IC	1	

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
IC500	2-36	E~C-3 (6/14)	3-4	F-2 (C)

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Front CPU (VEP86147A / AJ-D750)

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
IC1	HD64180ZRP8	HD64180ZRP8 or HD64180ZRP10	IC	1	

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
IC1	2-196	C~G-4 (1/4)	3-21	E-2 (C)

Front CPU (VEP86256A / AJ-D640/D650)

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
IC1	HD64180ZRP8	HD64180ZRP8 or HD64180ZRP10	IC	1	

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
IC1	2-154	E~C-3 (1/3)	3-12	K-3 (C)

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Improvement of Clamp Pulse of Color Signal

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D750E/EN	35	VSD9606M502A/B	B7TRB0001
AJ-D650E/EN	6	VSD9612MJ01A/B	B7TRA0001
AJ-D640E/EN	6	VSD9612MJ01A/B	B7TRA0001

Board : V IN (F6:VEP83341A) - AJ-D750
 V IN (F6:VEP83355B) - AJ-D640/D650

Symptom : Clamp pulse of the color signal is not good.

Remedy : To improve the clamp pulse of color signal, the following modification is performed.

- 1). Change transistors Q303, Q656, Q706 and Q756 from 2SK374 to 2SK198 on the foil side.
- 2). Change resistors R713 and R763 from 270K Ω to 220K Ω on the foil side.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
Q303	2SK374	2SK198	TRANSISTOR	1	
Q656	2SK374	2SK198	TRANSISTOR	1	
Q706	2SK374	2SK198	TRANSISTOR	1	
Q756	2SK374	2SK198	TRANSISTOR	1	
R713	ERJ6GEYJ274	ERJ6GEYJ224	M. RESISTOR CH 1/10W 220K	1	
R763	ERJ6GEYJ274	ERJ6GEYJ224	M. RESISTOR CH 1/10W 220K	1	

AJ-D750

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
Q303	2-116	F-6 (7/18)	3-8	I-3 (F)
Q656	2-123	F-7 (14/18)	3-8	E-3 (F)
Q706	2-124	F-7 (15/18)	3-8	C-2 (F)
Q756	2-125	F-7 (16/18)	3-8	C-1 (F)
R713	2-124	G-5 (15/18)	3-8	C-2 (F)
R763	2-125	G-5 (16/18)	3-8	C-1 (F)

AJ-D640/D650

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
Q303	2-90	C-5 (7/18)	3-7	I-3 (F)
Q656	2-97	B-6 (14/18)	3-7	E-3 (F)
Q706	2-98	B-6 (15/18)	3-7	C-2 (F)
Q756	2-99	B-6 (16/18)	3-7	C-1 (F)
R713	2-98	B-4 (15/18)	3-7	C-2 (F)
R763	2-99	B-4 (16/18)	3-7	C-1 (F)

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Improvement of LTC Output Waveform

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D750E/EN	36	VSD9606M502A/B	B7TRB0001
AJ-D650E/EN	7	VSD9612MJ01A/B	B7TRA0001
AJ-D640E/EN	7	VSD9612MJ01A/B	B7TRA0001

Board : System Control (F2:VEP86146B) - AJ-D750
 System Control (F2:VEP86146E) - AJ-D650
 System Control (F2:VEP86146F) - AJ-D640

Symptom : LTC Output waveform may not meet the specification. (SMPTE)

Remedy : To improve the LTC output waveform, the following modification is performed.
 1). Change capacitor C771 from 50V/2200pF to 50V/820pF on the component side.
 2). Change resistor R790 from 22K Ω to 12K Ω on the foil side.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
C771	ECUM1H222KBN	ECUM1H821JCN	C. CAPACITOR CH 50V 820P	1	
R790	VRE0034E223	VRE0034E123	M. RESISTOR CH 1/10W 12K	1	

AJ-D750

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
C771	2-41	D-13 (11/14)	3-4	I-4 (C)
R790	2-41	D-13 (11/14)	3-4	I-4 (F)

AJ-D640/D650

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
C771	2-41	D-8 (11/14)	3-4	I-4 (C)
R790	2-41	D-8 (11/14)	3-4	I-4 (F)

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Improvement of Crystal Oscillator

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D750E/ENV1206+V17227	95	VSD9606M502A/B	G7TRB0001
AJ-D650E/V1845+V1846	69	VSD9612MJ01A/B	G7TRA0001
AJ-D640E -12 + -16	69	VSD9612MJ01A/B	G7TRA0001

Board : System Control (F2:VEP86146B) - AJ-D750
 System Control (F2:VEP86146E) - AJ-D650
 System Control (F2:VEP86146F) - AJ-D640

Symptom : Crystal Oscillator for Time Code Gate Array may be malfunctioned.

Cause : Due to a little margin of the Crystal Oscillator.

Remedy : To prevent it, capacitor C727 is changed from 50V/18pF to 50V/5pF on the component side as shown below.

Part Number						
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks	
C727	ECUM1H180JCN	ECUM1H050CCN	C. CAPACITOR CH 50V 5P	1		

AJ-D750

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
C727	2-41	C-9 (11/14)	3-4	I-2 (C)

AJ-D650/D640

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
C727	2-41	E-5 (11/14)	3-4	I-2 (C)

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Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Deletion of Parts

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D750E/EN <i>VAF926 + VAF927</i>	96	VSD9606M502A/B	G7TRB0001
AJ-D650E <i>VAB415 + VAB416</i>	70	VSD9612MJ01A/B	G7TRA0001
AJ-D640E <i>-12 + -12</i>	70	VSD9612MJ01A/B	G7TRA0001

Board : RF AMP (H4:VEP85049A)

To improve the manufacturing productivity, the following parts are deleted.

- 1). Delete capacitors (25V/0.1 μ F) C5095, C5096, C5097, C5102, C5112, C5114 and C5115 from the component side.
- 2). Delete capacitors (25V/0.1 μ F) C5098, C5101, C5103, C5104 and C5113 from the foil side.
- 3). Delete IC5001 and IC5018 (TL084CNS) and IC5019 (NJM082BM) from the component side.
- 4). Delete IC5012 (NJM082BM) from the foil side.
- 5). Delete variable resistors (5K Ω) VR5001, VR5002, VR5003, VR5004, VR5005, VR5006, VR5007, VR5008, VR5009, VR5010, VR5011 and VR5012 from the component side.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
C5095 - 98	ECUM1E104ZFN	---	C. CAPACITOR CH 25V 0.1U	4 \rightarrow 0	
C5101 - 04	ECUM1E104ZFN	---	C. CAPACITOR CH 25V 0.1U	4 \rightarrow 0	
C5112 - 15	ECUM1E104ZFN	---	C. CAPACITOR CH 25V 0.1U	4 \rightarrow 0	
IC5001	TL084CNS	---	IC	1 \rightarrow 0	
IC5012	NJM082BM	---	IC	1 \rightarrow 0	
IC5018	TL084CNS	---	IC	1 \rightarrow 0	
IC5019	NJM082BM	---	IC	1 \rightarrow 0	
VR5001-12	VRV0112B502	---	V. RESISTOR 5K	12 \rightarrow 0	

AJ-D750

Ref. No.	Schematic Diagram		P.C.Board	
	Page	Area No.	Page	Area No.
C5095	2-175	D-4 (2/5)	3-13	C~D-1 (C)
C5096	2-175	D-4 (2/5)	3-13	C-1 (C)
C5097	2-175	E-4 (2/5)	3-13	C-1 (C)
C5098	2-175	E-4 (2/5)	3-13	C-1 (F)
C5101	2-175	E-4 (2/5)	3-13	A-1 (F)
C5102	2-175	F-4 (2/5)	3-13	A-1 (C)
C5103	2-175	F-4 (2/5)	3-13	A-1 (F)
C5104	2-175	G-4 (2/5)	3-13	A-1 (F)

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Ref. No.	Schematic Diagram		P.C. Board	
	Page	Area No.	Page	Area No.
C5112	2-175	G-4 (2/5)	3-13	C~D-1 (C)
C5113	2-175	H-4 (2/5)	3-13	B-1 (F)
C5114	2-175	H-4 (2/5)	3-13	B-1 (C)
IC5001	2-175	G-3 (2/5)	3-13	B-1 (C)
IC5012	2-175	F-2 (2/5)	3-13	A-1 (F)
IC5018	2-175	D-2 (2/5)	3-13	C-1 (C)
IC5019	2-175	E-3 (2/5)	3-13	A-1 (C)
VR5001	2-175	D-2 (2/5)	3-13	D-1 (C)
VR5002	2-175	D-2 (2/5)	3-13	D-1 (C)
VR5003	2-175	D-2 (2/5)	3-13	D-1 (C)
VR5004	2-175	E-2 (2/5)	3-13	D-1 (C)
VR5005	2-175	E-2 (2/5)	3-13	A-1 (C)
VR5006	2-175	F-2 (2/5)	3-13	A-1 (C)
VR5007	2-175	F-2 (2/5)	3-13	B-1 (C)
VR5008	2-175	F-2 (2/5)	3-13	B-1 (C)
VR5009	2-175	G-2 (2/5)	3-13	C-1 (C)
VR5010	2-175	G-2 (2/5)	3-13	B-1 (C)
VR5011	2-175	H-2 (2/5)	3-13	C-1 (C)
VR5012	2-175	H-2 (2/5)	3-13	C-1 (C)

AJ-D650/D640

Ref. No.	Schematic Diagram		P.C. Board	
	Page	Area No.	Page	Area No.
C5095	2-137	D-3 (2/5)	3-11	C~D-1 (C)
C5096	2-137	D-3 (2/5)	3-11	C-1 (C)
C5097	2-137	D-3 (2/5)	3-11	C-1 (C)
C5098	2-137	D-3 (2/5)	3-11	C-1 (F)
C5101	2-137	C-3 (2/5)	3-11	A-1 (F)
C5102	2-137	C-3 (2/5)	3-11	A-1 (C)
C5103	2-137	C-3 (2/5)	3-11	A-1 (F)
C5104	2-137	C-3 (2/5)	3-11	A-1 (F)
C5112	2-137	B-3 (2/5)	3-11	C~D-1 (C)
C5113	2-137	B-3 (2/5)	3-11	B-1 (F)
C5114	2-137	B-3 (2/5)	3-11	B-1 (C)
IC5001	2-137	B-3 (2/5)	3-11	B-1 (C)
IC5012	2-137	C-2 (2/5)	3-11	A-1 (F)
IC5018	2-137	D-2 (2/5)	3-11	C-1 (C)
IC5019	2-137	C-3 (2/5)	3-11	A-1 (C)
VR5001	2-137	D-2 (2/5)	3-11	D-1 (C)
VR5002	2-137	D-2 (2/5)	3-11	D-1 (C)
VR5003	2-137	D-2 (2/5)	3-11	D-1 (C)
VR5004	2-137	D-2 (2/5)	3-11	D-1 (C)
VR5005	2-137	C-2 (2/5)	3-11	A-1 (C)
VR5006	2-137	C-2 (2/5)	3-11	A-1 (C)
VR5007	2-137	C-2 (2/5)	3-11	B-1 (C)
VR5008	2-137	C-2 (2/5)	3-11	B-1 (C)
VR5009	2-137	B-2 (2/5)	3-11	C-1 (C)
VR5010	2-137	B-2 (2/5)	3-11	B-1 (C)
VR5011	2-137	B-2 (2/5)	3-11	C-1 (C)
VR5012	2-137	B-2 (2/5)	3-11	C-1 (C)

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Change of Factory Default Setting of DIP SW 501-8

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D750E/EN	106	VSD9606M502A/B	H7TRB0001

Board : System Control (F2:VEP86146B)

Factory default setting of DIP SW 501-8 on F2 System Control P.C. Board is set to ON from the August 1997 production. According to this, the following function can be available.

- 1). RS-232C Control function
- 2). DVCPRO/DV/DVCAM Playback select function

Regarding to the details information, please refer to the Technical Bulletin No. VSD9705SA658.

Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Software Version Up Grade

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D750E/EN	112	VSD9606M502A/B	I7TRB0001

Board : System Control (F2:VEP86146B)

The following software has been up-dated to improve the functioning of the VTR.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
IC2	VSI2277E	VSI2277F	F2 SYSTEM PROM Ver. P1.06	1	

< TEST MENU >

SERVO	IC235	:	F1-P1.08	1416	*	SYSTEM	IC2	:	F2-P1.06	025B
I/F	IC503	:	F2-P1.05	D6CE		AV	IC702	:	F2-P1.09	CAE1
FRONT	IC2	:	FP-1.05	5521						

* Note *

The hardware modification must be required since the following software version. (Servo/P1.08, System Control/P1.05, Interface/P1.05, AV/P1.09, Front/1.05). When the software is up-graded this time, please confirm the P.C. Board version. If the P.C. Board is not modified, the following modification must be performed.

[H3 EQ Board]

Please refer to the Technical Bulletin No. VSD9705SA658.

Symptom : AUTO OFF "S REEL TORQUE ERROR" may be occurred when the L cassette tape which is wound to tape beginning is inserted.

Cause : Supply Reel torque over may occur when the tape rushes into the tape beginning by Short FF function due to the mis-detection of tape end/beginning.

Remedy : System Control software version is up-graded to P1.06. At the same time, the following software version must be up-graded to the following version. Please refer to the Technical Bulletin No. VSD9705SA658.

Servo	VSI2280J	P1.08	1416
I/F	VSI2279E	P1.05	D6CE
AV	VSI2278J	P1.09	CAE1
FRONT	VSI2166E	1.05	5521

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Technical Bulletin

Supplement to the Service Manual

Broadcast Product

Subject : Software Version Up Grades

Please use this supplement together with the Service Manual as follows :

Model No.	Bulletin No.	Order No.	Effective from
AJ-D750E/EN	114	VSD9606M502A/B	J7TRB0001

Board : Servo (F1:VEP82105B)
System Control (F2:VEP86146B)
Front CPU (VEP86147A)

The following software have been up-dated to improve the functioning of the VTR.

Part Number					
Ref. No.	Original Part No.	New Part No.	Part Name & Descriptions	Pcs	Remarks
IC235	VSI2280J	VSI2280K	F1 SERVO PROM Ver. P1.09	1	
IC2	VSI2277F	VSI2277G	F2 SYSTEM PROM Ver. P1.07	1	
IC503	VSI2279E	VSI2279F	F2 I/F PROM Ver. P1.06	1	
IC702	VSI2278J	VSI2278L	F2 AV PROM Ver. P1.11	1	
IC2	VSI2166E	VSI2166F	FRONT PROM Ver. 1.06	1	

< TEST MENU >

* SERVO IC235 : F1-P1.09 D9E5	* SYSTEM IC2 : F2-P1.07 9626
* I/F IC503 : F2-P1.06 69C9	* AV IC702 : F2-P1.11 F173
* FRONT IC2 : FP-1.06 D4B5	

*** Note ***

The hardware modification must be required since the following software version. (Servo/P1.08, System Control/P1.05, Interface/P1.05, AV/P1.09, Front/1.05). When the software is up-graded this time, please confirm the P.C. Board version. If the P.C.Board is not modified, the following modification must be performed.

[H3 EQ Board]

Please refer to the Technical Bulletin No. VSD9705SA658.

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< Additional Function >

< System Control / AV >

1. System H Range select function is introduced on the System SETUP Menu as follows.
When the power is turned OFF connecting with Encoder Remote, System H setting value may be shifted.
To prevent it, the setting value on the Encoder Remote is always backed up.
This function is added on the System SETUP Menu as follows.

Item		Setting		Description
No.	Superimposed Display	No.	Superimposed Display	
20	SYS H RANGE	0000 0001	FULL FINE	This adjusts the adjustable range for SYSTEM H during when the Encoder Remote is connected. 0 : $\pm 8 \mu\text{sec}$ (± 30 steps) 1 : -1.9 to $+2.7 \mu\text{sec}$ (-7 to $+10$ steps) < Note > If setting operation is performed, the setting value does not return to factory (default) setting.

< Note >

The System Control and AV PROM must be up-graded at the same time as follows.
System Control : more than P1.07, AV : more than P1.10

< System Control / Interface / Front >

1. Channel condition is displayed on the Superimpose.
2. INT BB is displayed.
3. Warning Message is displayed on the Superimpose.

< System Control / Interface >

1. VAR/JOG speed select function is introduced on the SETUP Menu connecting with Remote (9P, RS-232C) as follows.

Item		Setting		Description
No.	Superimposed Display	No.	Superimposed Display	
314	JOG RANGE	0000 0001	-0.43 ~ 1 -4 ~ +4	This sets the range of the JOG speed during Remote operation. 0 : Plays at -0.43 to $+1$ speed range (In DV or DVCAM format, -0.5 to $+1$ speed range) 1 : Plays at ± 4.1 speed range (In DV or DVCAM format, ± 3.1 speed range) < Notes > 1. Phase synchronization from the editing controller is no longer possible once this item has been set to "0". 2. During the dial-up operation at the front, the unit normally plays at the -0.43 to $+1$ speed range regardless of the setting in the SETUP Menu. (In DV or DVCAM format, the unit plays at the -0.5 to $+1$ speed range)

The Playback speed range is as follows.

SETUP Menu Setting		Playback Speed			
		Front Dial		Remote (9P, RS-232C)	
		JOG	VAR	JOG	VAR
300 : VAR RANGE	0 : -.43 ~ 1		-0.43 ~ +1 (-0.5 ~ +1)		-0.43 ~ +1 (-0.5 ~ +1)
	1 : -4 ~ +4		-4.1 ~ +4.1 (-0.5 ~ +1)		-4.1 ~ +4.1 (-3.1 ~ +3.1)
314 : JOG RANGE	0 : -.43 ~ 1	-0.43 ~ +1 (-0.5 ~ +1)		-0.43 ~ +1 (-0.5 ~ +1)	
	1 : -4 ~ +4			-4.1 ~ +4.1 (-3.1 ~ +3.1)	

() DV/DVCAM Playback speed

< Improvement of Performance >

< Servo >

1. Time code may be frozen during RF AUTO Adjustment mode. It is improved.
2. When the SHTL mode is reversed, its response is too late. It is improved.
3. When the mode is changed from STOP to PLAY, Quick Start is not performed. It is improved.
4. Capstan may overshoot during JOG mode. It is improved.
5. Capstan Motor may not rotate when the mode is changed from X0.5 to FF and then X0.5. It is improved.
6. Tape damage may occur when the cassette tape lid is not opened and the unit goes to Loading mode. It is improved. AUTO OFF "FRONT_LOAD_ERROR" will be displayed.
6. Reel Motor may be rushed when the unit goes to Loading mode by Emergency with no cassette tape. It is improved.
7. When the mode is changed from STOP to REW and then STOP at the tape end, the tape is over-tension. It is improved. (M and L cassette)

< AV >

1. LTC read error may occur during DV Playback mode with BVW-75. It is improved.
2. Audio 4 CH output can be available on the PLAY mode only during DV Playback mode. All mode can be available for Audio 4 CH output.
3. Audio may be muted when the Error Rate is high. It is not muted.
4. TC OUT (LTC/VITC) is advanced 1 frame to the Video output during EE mode. It is improved.
5. L channel is not output when the Monitor is selected. It is improved.

< Interface >

1. Dip SW4-1 on the Front is not turned OFF during RF Auto Adjustment mode. It is improved.
2. When the Edit point is registered 2 points on the Recorder side and 1 point on the Player side, one Recorder side point which is not registered on the Player side is trimmed. This time, another registered point of the Recorder side is deleted and the its registered point of the Player side is deleted too. It is improved.
3. Communication error between Interface and Front may occur during DV/DVCAM Playback mode. It is improved.
4. Preview mode is not accepted with AG-A350 during IN GOTO mode. It is improved.
5. Warning Message LED is always displayed the Recorder side Warning.
6. When the deck to deck editing mode is performed with AU-650/660 (Player side), AUDIO SPLIT Editing can not be performed. AIN; AOUT of the Player status is memorized on the Recorder side.
7. When the PREVIEW/AUTO EDIT is performed which Player side setting of [301:IN/OUT DEL] on the User SETUP Menu is AUTO with deck to deck Editing mode, editing is finished after passing the IN point instead of OPEN END. It is improved.
8. When the RESET button is pressed during PLAY mode with CTL or INS mode, key function is not efficient. It is improved.

9. When the RESET button is pressed on STOP mode during CTL mode on the Recorder side with deck to deck editing mode, the unit does not go to deck to deck editing mode. It is improved.

< Front >

1. When the DIAL position is JOG while [100:SEARCH ENA] on Operation SETUP Menu is set to DIAL (direct search). It is improved,

< Servo / System Control >

1. When the cassette tape is inserted and the unit goes to Loading mode right after it is ejected, tape position may shift. It is improved.

< System Control / Interface / AV >

1. When the MONI CH SEL on the Audio SETUP Menu is selected AUTO mode, L/R display on the Front Panel is not same at the Monitor selection. It is improved. Then, the display will change according to the monitor output.

*** Note ***

System Control / Interface /AV PROM must be up-graded at the same time.